International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 07 Issue: 06 | June - 2023 SJIF Rating: 8.176 ISSN: 2582-3930

Comparative analysis of 1:1:1 and 1:2:2 bitcell and implementing write assist

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***Abstract*—This paper presents a comprehensive comparison between two distinct bitcell designs: the 1:1:1 bitcell and the 1:2:2 bitcell. Bitcell analysis is a critical aspect of memory design, influencing system performance, power consumption, area efficiency, and reliability.The paper begins by introducing the two bitcell designs and their fundamental principles. The 1:1:1 bitcell represents a conventional single-ended bitcell architecture, widely used in various memory technologies. On the other hand, the 1:2:2 bitcell is a modified version featuring a differential read path, enabling improved read stability and enhanced noise immunity.A comprehensive performance evaluation is conducted, comparing the key metrics of the two bitcell designs. The analysis encompasses parameters such as read and write stability, read and write margins, power consumption, access time, and area efficiency. The impact of process variations, temperature variations, and supply voltage fluctuations on the performance of both bitcell designs is also investigated.In conclusion, this paper offers a comparative analysis of 1:1:1 and 1:2:2 bitcell designs, assessing their performance, reliability, and system-level implications. The findings serve as valuable insights for memory designers, researchers, and engineers, aiding in the selection and optimization of bitcell designs for next-generation memory architectures.**

***Index Terms*—bitcell, process variations,temperature vari-ations, supply voltage fluctuations,read stability,write stabil-ity,noise immunity.**

I. INTRODUCTION

Memory compilers are essential tools in the design and implementation of integrated circuits, enabling efficient and systematic generation of memory structures with specific characteristics. With the increasing demand for high-density and high-performance memories in various applications, memory compilers have become instrumental in streamlining the memory design process.

The primary objective of a memory compiler is to generate memory structures that meet specific requirements and constraints, such as area, power consumption, access time, and performance. These requirements are typically specified by the system designer based on the application's needs and the target technology node. Memory compilers use sophisticated algorithms and optimization techniques to generate optimal memory configurations that balance these requirements while ensuring proper functionality and manufacturability.Moreover, memory compilers offer a level of customization and flexibility, allowing designers to modify various parameters and trade-offs to tailor the memory structure to their specific needs. Designers can adjust aspects such as word size, bit width, aspect ratio, sense amplifier design, and other critical circuit characteristics. This flexibility enables designers to optimize the memory structure for specific application requirements, such as high-speed operation, low-power consumption, or compact area utilization.

Another key advantage of memory compilers is their ability to adapt to different technology nodes and process variations. As semiconductor technology evolves, memory compilers can be updated and optimized to support new process technologies, ensuring compatibility and maximizing the benefits offered by advanced manufacturing nodes.

In summary, memory compilers have emerged as indis-pensable tools in the design and implementation of mem-ory structures. By providing a standardized and automated approach, they enable efficient generation of memory arrays with specific characteristics, while offering flexibility and customization options. With their ability to adapt to new technology nodes and address reliability and manufacturability challenges, memory compilers empower designers to meet the ever-increasing demands for high-performance and high-density memories in various applications.

Bitcell analysis is a critical aspect of memory design, playing a pivotal role in the development of efficient and reliable memory architectures. Bitcells are the fundamental building blocks of memories, responsible for storing and retrieving binary data in integrated circuits. Analyzing and optimizing the performance, power consumption, reliability, and area efficiency of bitcells are crucial for meeting the growing demands of modern memory systems.

The objective of bitcell analysis is to evaluate various performance metrics and trade-offs associated with different bitcell designs. These metrics include read stability, write abil-ity, read and write margins, access time, power consumption, area utilization, and reliability. Through rigorous analysis and optimization, memory designers can select the most suitable bitcell design for specific applications and technology nodes.

In conclusion, this paper presents a detailed comparison analysis of the 1,1,1 and 1,2,2 bitcell designs. By evaluat-ing their performance metrics, reliability considerations, and system-level implications, the paper aims to provide valuable

insights into the strengths, weaknesses, and trade-offs associ-ated with each bitcell design. This analysis serves as a valuable resource for memory designers, researchers, and engineers, aiding in the selection and optimization of bitcell designs for next-generation memory architectures.

II. BITCELL FUNDAMENTALS

A. Overview of Bitcell

Bitcells are fundamental components of memory systems that store and retrieve binary data. They consist of transistors and capacitors and enable the operation of different memory technologies. Bitcells undergo read, write, and hold operations to retrieve, update, and maintain stored data. Performance met-rics such as read stability, write ability, and access time assess their efficiency. Reliability considerations include factors like soft errors and aging effects, which can impact long-term stability. Optimizing bitcell design is crucial for developing efficient and reliable memory architectures.

The performance of bitcells is evaluated based on various metrics, including read stability, write ability, read and write margins, access time, power consumption, and area efficiency. Read stability refers to the ability of the bitcell to main-tain its stored value during the read operation. Write ability measures the ease and reliability of writing new data into the bitcell. Read and write margins represent the voltage or current levels required for proper operation. Optimizing the design and characteristics of bitcells is essential for achiev-ing efficient and reliable memory systems. Researchers and designers continuously explore innovative bitcell architectures and optimization techniques to meet the increasing demands of high-performance, low-power, and high-density memory applications.

B. Design of 1:1:1 and 1:2:2 FinFet bitcell

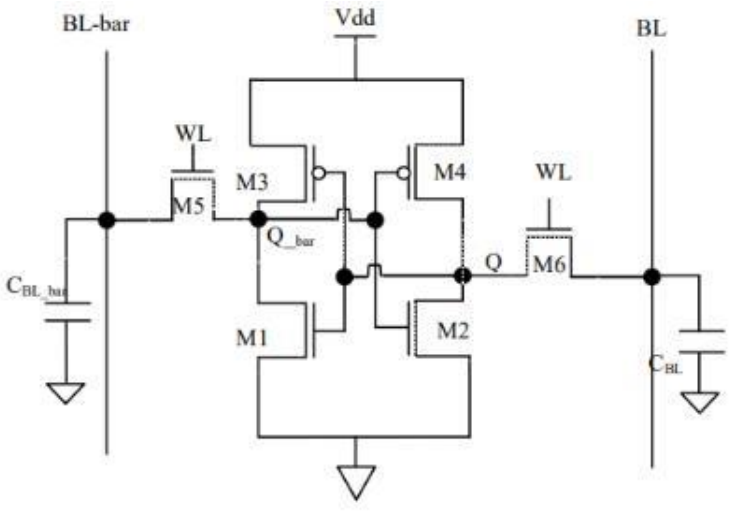

Fig. 1. SRAM Bitcell Schematic

Both the 1:1:1 and 1:2:2 bitcell differ in the Fin size of the mosfets used in the bitcell. As seen in figure 1 when the access transistors(PG) denoted by M5 and M6 , the pull up(PU) transistor denoted by M3 and M4 and the pull down(PD) transistor denoted by M1 and M2 have the same fin size ratio then they represent 1:1:1 bitcell.

On the other hand when the Fin ratio of the PD ,PU and PD is such that the sizing of PU is half the size of PG and PD then it is known as a 1:2:2 bitcell.

As it is known for the write operation to take place the $(W/L)_{PG} > (W/L)_{PU}$ denotes the stability condition but in 1:1:1 bitcell as all the three transistors are of the similar size the writability comes out to be lesser as compared to 1:2:2 bitcell. Thus, to improve this a negative BL technique is used in 1:1:1 bitcell to improve the writability.

C. Performance metrics for a Bitcell

In this paper comparing the performance of the 1:1:1 Fin-FET bitcell and the 1:2:2 FinFET bitcell, several performance metrics can be evaluated. These metrics provide insights into the efficiency and speed of the bitcells. Here are few of the metrics which are considered:

1) Read and Write Time: This metric measures the time required to access and manipulate data in the bitcells. It encompasses various delays, including address decod-ing, signal propagation, and data retrieval or storage. A shorter read and write time indicates faster data transfer, allowing for quicker access to information stored in the memory. This metric is crucial for applications that require high-speed data processing, such as real-time systems or high-performance computing.
2) Cell Stability: Cell stability refers to the ability of the bitcells to retain stored data accurately over time and under different operating conditions. Factors such as leakage current, charge loss, and sensitivity to noise can impact stability. A more stable memory operations and data integrity in applications where data retention is essential, such as cache memories or non-volatile memories.
3) Noise Immunity: Noise immunity assesses the ability of the bitcells to withstand external noise sources without compromising data integrity. External noise can arise from various sources, including power supply fluctu-ations, electromagnetic interference, or crosstalk from neighboring circuits. A bitcell design with high noise immunity can mitigate the impact of such noise sources and maintain accurate data storage or retrieval. Eval-uating noise immunity helps ensure reliable memory operation in noisy environments or applications where noise sources are prevalent.
4) Read and Write Margins: Read and write margins rep-resent the voltage levels required for reliable read and write operations. They indicate the voltage range within which the bitcells can correctly interpret and store data. Large read and write margins imply greater tolerance to voltage variations, noise, or process variations, ensuring

robust operation across different operating conditions. Analyzing read and write margins helps identify the bitcells sensitivity to voltage fluctuations and ensures reliable memory operation in practical scenarios.

5) Power Consumption: Power consumption quantifies the amount of electrical power needed to operate the bit-cells. It includes both dynamic power and static power. Dynamic power is consumed during switching activi-ties when reading or writing data, while static power represents the power dissipated when the bitcells are idle. Lower power consumption is desirable as it reduces energy costs, extends battery life in portable devices, and minimizes heat generation, which can affect system reliability. Analyzing power consumption helps identify energy-efficient bitcell designs. The power consumption The power is calculated on the basis of the current thus analysis of leakage current, standby current and read current as important performance parameters to be analyzed.

III. METHODOLOGY

We mainly focus on the analysis of the following parameters for different processes, voltages and temperature.

1) Read current analysis - This analysis examines the current passing through the access transistor ie, PG when the read operation takes place. This read current is useful in finding out the amount of power dissipated through the bitcell while read operation takes place. Thus, read current helps in deciding which bitcell out of 1:1:1 and 1:2:2 has higher read current.
2) Leakage current analysis - Leakage is a major issue that leads to wastage of a lot of power of the bitcell. Leakage current is the current that passes through PG when the worldline of the bitcell is at VSS. This means that the current through PG is found when the bitcell is off.
3) Standby current analysis - Standby current analysis refers to leakage current through either PU or PD transistor when the bitcell is off ie, when the worldline is zero.
4) Static noise margin - SNM is one of the most important parameters to be analyzed for a bitcell. SNM helps in providing the noise stability for the bitcell. In SNM analysis the potential at one of the critical nodes at which the cell flips is from 0 to VDD and the voltage at which the cell flips is determined. The more the SNM the better the data retention of the cell and better noise stability of the cell.
5) DC Write Margin - DC Write margin analysis is done to find the minimum voltage at the bitline for the write operation to take place. For the same reason let's assume that Q bar is at 1 and Q is at 0. For the write operation to take place WL is turned on.For the analysis of DCWM Bl bar is given a DC pulse that goes from Vdd to 0 for the write operation to take place and the voltage at which the cell flips is noted. This gives us the minimum voltage required on the bitline for the write to take place. Higher the write margin the better is the readability of the cell. This writability can also be improved by using the write assist technique if required.
6) AC write margin - The AC write margin is used in determining the flip time of the bitcell. Flip time as the name suggests is the amount of time required for the cell to flip the data stored in it.Assuming the internal node Q bar is at 0 and Q is at 1.Thus for write to take place Bl bar is given 1 and Bl is given 0 based on this assumption flip time can be determined by 2 different analysis-
   - BL driven write margin - In this a pulse of very short duration in nanoseconds is given on the bit-line(Bl bar) to transverse from Vdd toward 0. The critical nodes are monitored to check when the data flips. The time required for the data to flip is the maximum of the time required for Q bar to rise to 0.95*Vdd when Bl bar drops by 50% or Q to fall to 0.05*Vdd when Bl bar falls by 50%
   - WL driven write margin - As the name suggests a pulse of very short duration is given on the WL and the critical notes are monitored to check when the data flips.Here, the flip time is the maximum of Q bar reaching 0.95*Vdd when WL rises by 50% or Q reaching 0.05 *Vdd when WL rises by 50%.

IV. EFFECT OF DIFFERENT PVT'S ON A BITCELL

A. Effect of change in process

For the comparison of 1:1:1 and 1:2:2 the NMOS and PMOS have mainly three different processes i.e., slow, fast and typical. The slow process denotes that the Vt of the mosfet is higher than the typical value whereas the fast process denotes that the Vt of the mosfet is lower than the typical value. If the parameter of flip time is compared it is noticed that for ss ie, when both pmos and nmos are slow is most and for ff ie, when both the pmos and nmos are fast is the least provided the voltage and temperature is fixed.

B. Effect of voltage

The voltage here refers to the supply voltage which is very important in the functioning of the bitcell. Again comparing the 1:1:1 and 1:2:2 bitcell for flip time, keeping the process and temperature constant it can be noticed that as the voltage increases the flip time reduces as the readability becomes better but this reduction in flip is more in 1:2:2 bitcell as compared to the 1:1:1 showing that the writability in he 1:1:1 bitcell is better.

C. Effect of Temperature

Here the analysis is done for mainly two temperatures - 40°C and 150°C. Analyzing the flip time it is observed that as the temperature increases the flip time reduces provided the process and voltage are kept constant. Here, also as the temperature increases the flip time reduces mire for the 1:2:2 bitcell as compared to 1:1:1 bitcell.

V. IMPLEMENTATION OF WRITE ASSIST

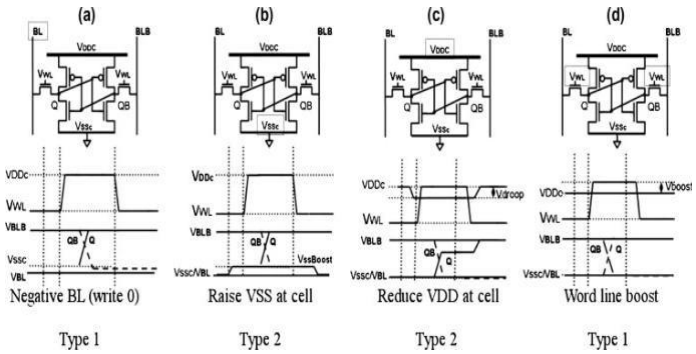

Fig. 2. Different Write assist techniques

After the running the bitcell analysis it became evident that in terms of the writability the 1:1:1 bitcell is weaker as compared to 1:2:2 bitcell ie, the flip time in 1:2:2 bitcell is less asd compared to 1:1:1 bitcell. The reason behind this being that in 1:1:1 bitcell the $(W/L)_{PG} = (W/L)_{PU}$ but for the write operation to take place in a bitcell the write stability condition is $(W/L)_{PG} > (W/L)_{PU}$ making the write operation weak in 1:1:1 bitcell. For the same reason the implementation of write assist becomes important Figure 2 shows the different write assist techniques that can be applied :

- The Negative Bitline Write Assist technique : It is used to improve the write ability of the SRAM cell. In this technique, an additional negative bitline (NBL) is used during the write operation to boost the voltage at the cell nodes. This reduces the voltage difference between the bitlines, which in turn reduces the possibility of write failures.During the write operation, the data to be written is applied to the bitlines and the wordline is activated. The voltage at the cell nodes is pulled down to ground through the activated access transistor. At the same time, the NBL is activated and precharged to a negative voltage. When the voltage at the cell nodes drops below the precharged voltage on the NBL, the NBL is discharged through the cell, which results in a higher voltage at the cell nodes.The NBL technique improves the write margin of the SRAM cell by increasing the voltage at the cell nodes during the write operation. This reduces the voltage difference between the bitlines and improves the stability of the stored data.
- The ”raise Vss at cell” technique : It is a write assist technique used in SRAM bitcells to improve write ability. In this technique, the voltage of the Vss line, which is the ground reference voltage for the SRAM bitcell, is increased only at the cell being written. This is done by using a local charge pump or level shifter circuit that generates a higher voltage than the global Vss level.During a write operation, when a logic ’1’ needs to be written into the bitcell, the access transistor that connects the bitline to the bitcell is turned on, and the bitline voltage is pulled high. At the same time, the wordline voltage is raised to activate the write driver in the bitcell, which in turn pulls the internal node of the bitcell high. However, due to the threshold voltage of the access transistor, the voltage at the internal node may not rise to the full logic ’1’ level, especially at low supply voltages.By raising the Vss voltage at the bitcell, the threshold voltage of the access transistor is reduced, allowing a higher voltage to be written into the cell. This improves the write margin and reduces the probability of write failures. However, the increased voltage at the Vss line can also increase leakage current and power dissipation, which are important factors to consider in the overall design.
- Reducing Vdd at the SRAM cell : This is a commonly used technique to improve the write ability of the SRAM cell. By reducing the Vdd voltage level, the cell becomes less susceptible to write failures caused by process vari-ations and other noise sources. The reduced Vdd voltage level also reduces the voltage stress on the SRAM cell transistors, resulting in lower leakage current and power dissipation. However, reducing the Vdd voltage level too much can lead to read instability and increased read ac-cess time. Therefore, an optimal trade-off between write margin improvement and read stability must be achieved when using this technique. This technique is often used in conjunction with other write assist techniques to further improve the write ability of the SRAM cell.
- Wordline boost technique : The wordline boost technique is a type of write assist technique used in SRAM bitcells to improve their write-ability. In this technique, the volt-age level of the wordline during the write operation is increased beyond the nominal voltage level. This helps in reducing the threshold voltage of the access transistor and increasing its conductance. As a result, the access tran-sistor allows a larger current to flow through it, thereby improving the write-ability of the SRAM cell.During the write operation, a large voltage is applied to the selected wordline, which is typically higher than the nominal voltage level of the wordline. This high voltage level causes an increase in the electric field across the gate oxide of the access transistor, resulting in a reduction in the threshold voltage. This makes it easier for the bitline to pull the voltage on the storage node to the desired level, leading to a more reliable write operation.One of the advantages of the wordline boost technique is that it can be easily implemented using simple circuitry. Addi-tionally, it does not require any additional power or area overhead. However, this technique may result in increased leakage current and power dissipation in the SRAM array due to the higher voltage level applied to the wordlines during the write operation. Hence, careful optimization is required to balance the write-ability improvement with the power and leakage overhead.

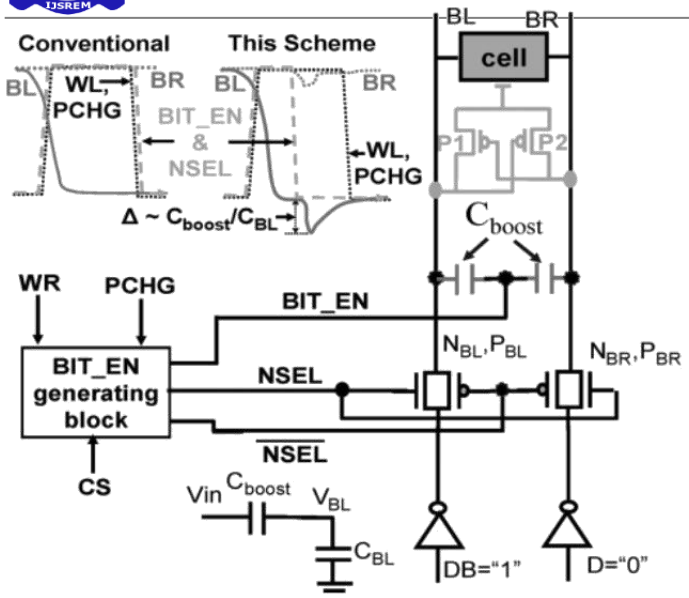

Fig. 3. Negitive bitline technique

Out of all these techniques the one which is used is the negitve bitline technique. The reason for using is technique is that it is the most optimized technique and it the easiest to scale out of all the other techniques. By changing the capacitance of the capacitors the negitve voltage to be given to bitlines can be changed. In this method two Cboost capacitors are used to reduce the bitline voltage. For this the BIT EN transitions from high to low. When this goes low the other end of the capacitor falls below zero making the BL negative . As the BL becomes negative as seen in figure 1 the the source of the pass transistor M6 or M5 goes below 0 increasing the Vgs and making the pass transistor stronger than the Pull up and improving the writability. This is applied in the 1:1:1 bitcell where by increasing the Vgs the write stability condition is met and the writability is improved.

VI. RESULTS

The analysis between 1:1:1 and 1:2:2 shows that 1:2:2 gives better read current , leakage current and standby current because of the fin sizes being more.

TABLE I
READ , LEAKAGE , STANDBY CURRENT ANALYSIS

parameters	1:1:1	1:2:2
Read current	1.66E-05	2.89E-05
Leakage current	2.18E-13	5.09E-13
Standby current	8.25E-13	1.39E-12

These values in Table I are for both the mosfets being in typical process and operating at the lowest Vdd and lowest temperature. When the process goes from typical to slow the current reduces whereas when the process goes from typical to fast the current increases. Similarly when the voltage or the temperature increases the current also increases.

It is clear in Table II that the static noise margin in the case of 1:1:1 bitcell is higher as the passsgate in this case is weaker, reducing the current. This reduces the voltage bump at any one of the voltage node when the read operation takes place requiring more voltage for the cell to flip , thus higher SNM

TABLE II
SNM AND DCWM ANALYSIS

parameters	1:1:1	1:2:2
SNM	0.067912	0.06378
DCWM	0.256628	0.272572

In case of DCWM it can be seen that the write margin value is better in 1:2:2 bitcell making its writabilty better as the size of the pass gate is more than the size of the pull up making the passgate stronger.

As the prcoess goes from both the mosfets being typical to slow the current reduces and thus in turn the static noise margin increases , also if both the mosfets have become of fast process then the current increases and SNM decreases. On the other hand the more the current the more the write margin thus , as the process goes from typical to slow the write margin reduces whereas when it goes from typical to fast the write margin increases.

TABLE III
AC DRIVEN WRITE MARGIN ANALYSIS

parameters	1:1:1	1:2:2
AC BL driven write margin	1.38E-10	1.23E-10
AC WL driven write margin	1.46E-10	1.27E-10

TABLE IV
WRITE MARGIN AFTER WRITE ASSIST

parameters	1:1:1 before write assist	1:1:1 after write assist
Flip time	1.38E-10	1.20541E-10

The flip time as seen in TABLE III is more for 1:1:1 bitcell showing that the writability of the bitcell is less as compared to 1:2:2 bitcell. This writability can be improved with the help of the write assist technique. being applied. The flip time increases as the current reduces making the writability weaker. Thus, as the process goes from typical to slow the flip time increases whereas as it goes from typical to fast the flip time reduces. Similarly as temperature and supply voltage increase current increases reducing the flip time.

It can be seen in Table IV that after applying the write assist technique of making the bitline negative the flip time of the 1:1:1 bitcell improves and becomes close to the flip time of the 1:2:2 bitcell as seen in TABLE III.

VII. CONCLUSION

The complete comparison of 1:1:1 and 1:2:2 bitcells for various PVT's gives a clear picture that the 1:2:2 bitcell has better writability as compared to 1:1:1. Also , the writability of the 1:1:1 bitcell can be improved and match the 1:2:2 bitcell but this leads

to more power dissipation involved due to the write assist circuit that is used.

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