International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 08 Issue: 05 | May - 2024 SJIF Rating: 8.448 ISSN: 2582-3930

Comparative Analysis of 8-Bit Test Pattern Generator for LBIST

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Abstract - In order to guarantee their dependability, modern integrated circuits require efficient testing techniques. One of the greatest DFT methods [2] for logic design when an IC must be tested on a regular basis is LBIST. The DUT, a comparator, an analyzer, a test pattern generator, and memory for storing golden values are all part of the LBIST architecture. DUT affects the circuit's power because it dwells with the test circuitry. The use of area- and power-efficient TPG can lower this overhead. The project's primary goal is to put several TPGs that have been presented in a lifetime into practice and conduct a comparative analysis of them.

Key Words: DFT, CUT, ORA, MC-LFSR, BSMCS,

BS-LFSR, LP-TPG.

1. INTRODUCTION

Quality and dependability are essential in the design and manufacture of integrated circuits. BIST techniques assist in achieving these objectives for intricate semiconductor devices. An essential part of BIST systems is the 8-bit pattern generator, which generates test patterns for assessing logic blocks. In order to enhance Logic BIST applications, this study compares 8-bit pattern generator designs[1].

One of the pillars of the Design-for-Testability (DFT)[2] in integrated circuits is LBIST. By creating on-chip test patterns, it lessens the requirement for external testing apparatus and streamlines chip testing for use in in-field and production processes. The pattern generator generates a series of test vectors that are applied to logic blocks in order to identify possible errors that could affect the circuit's performance, such as aging-related problems and manufacturing defects.

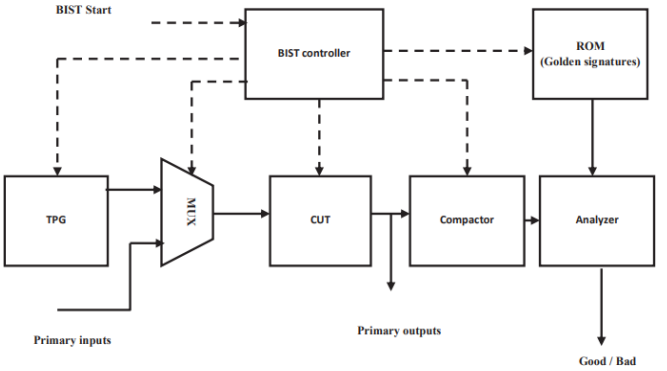

Fig-1: Detailed logic of BIST system

2. Methodology

1. Verilog HDL will be used to implement all TPGs covered literature.
2. Using simulation results and a test bench with cadence NCsim, the functional verifications of the RTL code will be carried out.
3. A 45 nm technologically sluggish library will be used to create the designs with a significant effort with Cadence Genus.
4. For the implemented design, power will be estimated and compared.

3. Literature Review

1. Conventional LFSR:

Shift registers known as LFSRs[3] have linear functions as their input. The XORed output of particular shift register nodes is used by the shift register as feedback. Without repeating any of the patterns, the LFSR generates every feasible pattern. A pattern that exhibits strong correlation between them must be produced by the feedback system selected for the LFSR. The random pattern is generated by the primitive polynomial x^8+x^4+x^3+x^2+1, and the feedback system determines the TAP sites. The clock is triggered in order to enable the values from the input to the output.

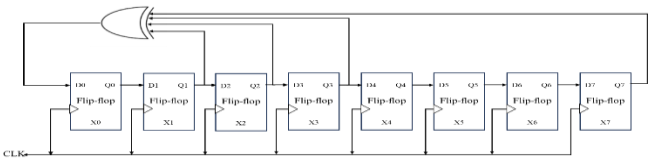

Fig-2: Conventional LFSR

Advantages:

1) Its application in mineral and hydrocarbon exploration is extensive.
2) It can be applied to evaluate soil qualities and map subsurface water resources.

2. LFSR with Modified Clock Scheme:

By keeping undesirable flops dormant, clock gating lowers digital power dissipation. This method lowers switching activity, and Fig-3's MC-LFSR[4] architecture increases area while lowering power. When the input and output are equal, the clock is turned off, and the pattern transition is the same as with a traditional LFSR. This method lessens switching to decreasing power consumption, but it is not very successful in reducing testing power.

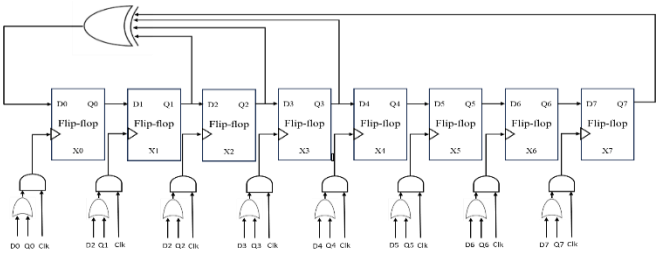

Fig-3: MC LFSR

Advantages:

1) It strengthens the system's security.
2) It is sturdy

3.BS-LFSR(Bit-Swapping technique):

By using multiplexers in conjunction with the traditional LFSR, the BS-LFSR technique[6] lowers the switching activity in the LFSR. Fig-3 shows the layout of the multiplexer and LFSR. The output of the nth flip-flop in this architecture determines the chosen line for the multiplexers. The flip-flops' output is switched, and the bits that are adjacent to it are multiplexed together. The second bit with the first bit, the fourth bit with the fifth bit, and so on, all the way up to the (N-1)th bit of the LFSR, are examples. The bits will be swapped until the (N-2)th flip-flop if the LFSR's length is even. On the other hand, multiplexing continues until the (N-1)th flip-flop if the LFSR's length is odd.

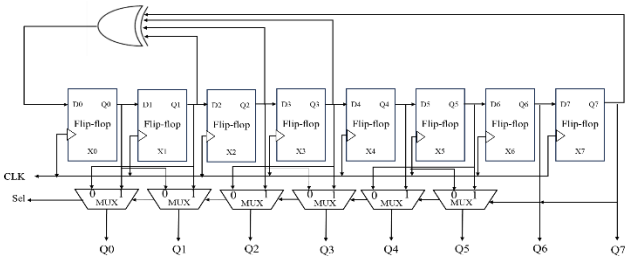

Fig-4:BS-LFSR

Advantages:

1) They are relatively simple to implement in hardware and software.

4. Bit Swapping technique with Modified Clock Scheme:

By utilizing two distinct architectures, a new LFSR has been presented that lowers power usage in two dimensions. While the second architecture cuts power by switching the bits next to flops, the first architecture employs clock gating. The BSMCS LFSR[5] is the outcome of this. A novel technique has been presented to cut down on power usage, which involves disabling logic circuits that are unable to conduct functional activities within a specified timescale. The "gated clock" method, which only activates the FF when the input signal differs from the actual output value, can be used to accomplish this. Every pair of adjacent bits in the modified LFSR is multiplexed, with the exception of the nth bit, which serves as the multiplexers' selection line.

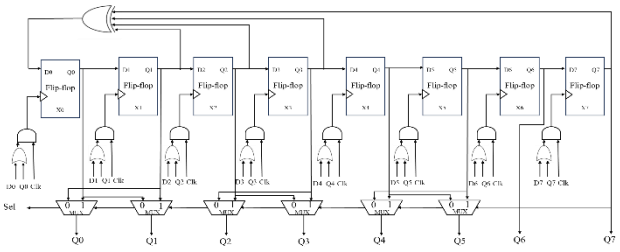

Fig-5: BSMCS LFSR

Advantages:

1)It allows flexibility in adjusting the timing of bit-swapping operations.

5. Low Power Transition test pattern generator:

As seen in Fig-6, the new architecture is composed of an LP-TPG, an m-bit counter, an n-bit gray code generator, a NOR-gate structure, and an XOR array. The m-bit counter is first filled with zeros, producing two million test pattern sequences. A single clock signal governs both the m-bit counter and the gray code generator. The gray code generator and the NOR-gate structure are coupled to the m-bit counter's output. The NOR-gate output is 1 when every bit in the counter output is 0. Using the supplied clock signal, the LP-TPG generates the subsequent sequence upon activation of this 1 output. Next, the sequence produced by the gray code generator and the LP-TPG[7] sequence are XORed. This XOR array generates the final output patterns.

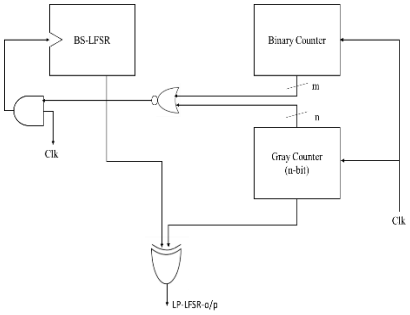

Fig-6:LP-TPG

Advantages:
1) It uses less energy when creating test patterns.
2) It saves money.

3. Experimental Results

1 . Conventional LFSR:

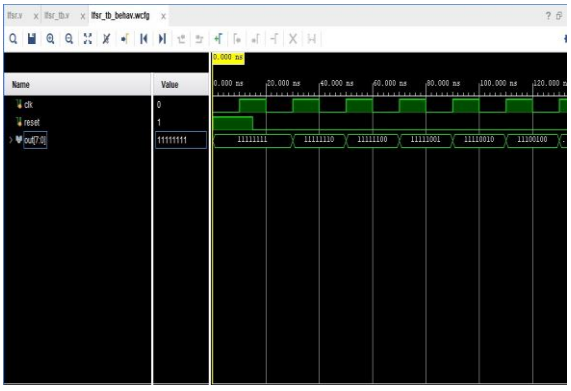

Fig-7: Simulation result of Conventional LFSR

The simulation of 8-bit conventional LFSR is given in Fig-7. In this value, 11111111 seed is fed into the LFSR at the reset with the clock.

2. LFSR with Modified Clock Scheme:

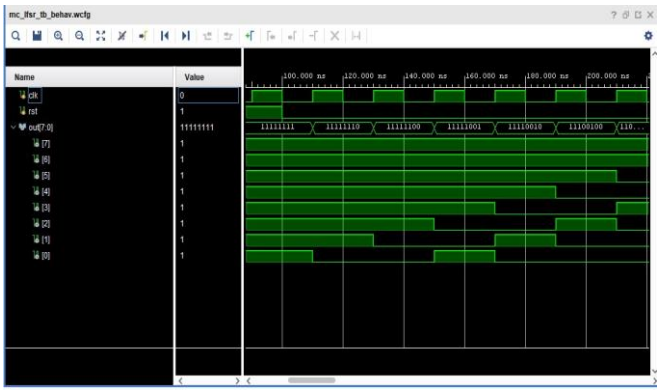

Fig-8: Simulation result of LFSR with Modified Clock

The simulation result of the Modified Clock Scheme LFSR is shown in Fig-8. Initially, the clock is 0 and at the reset, LFSR is loaded with the seed value (11111111). The LFSR output is given by ‘out’.

3.BS-LFSR(Bit-Swapping):

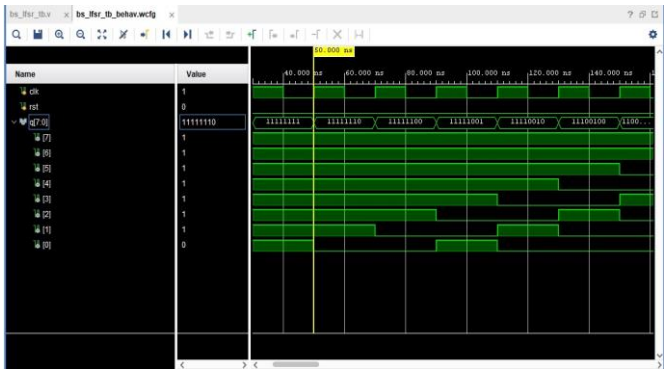

Fig-9: Simulation result of BS-LFSR(Bit-Swapping)

The simulation results for the BS-LFSR technique are as shown in the Fig-9 respectively. Initially, the clock (clk) is 0 and the reset (rst), when the rst is high the LFSR is loaded with the seed value (11111111). Once the rst is 0 the LFSR starts generating the test patterns based on the feedback mechanism. The output is given by ‘out’ and it is shown for both hexadecimal and in decimal value for convenience. When the MSB bit is 0 the bits are swapped.

4. Bit Swapping technique with Modified Clock:

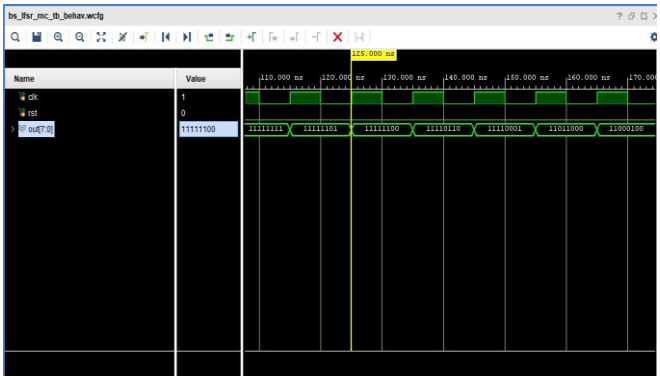

Fig-10: Simulation result of Bit Swapping technique with Modified Clock

The simulation result of the BSMCS LFSR. Initially, the clock (clk) is 0 and the reset (rst) is set, when the rst is high the LFSR is loaded with the seed value (11111111).

5. Low Power transition test pattern generator:

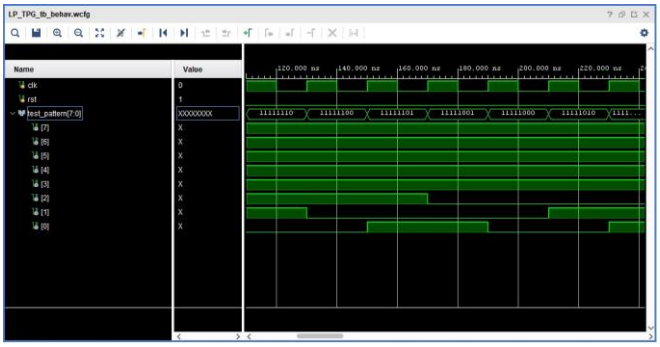

Fig-11: Simulation result of Low Power transition test pattern generator

The Fig-11 shows the simulation result of the LP-TPG. Initially, the clock (clk) is 0 and the reset (rst) is set, when the rst is high the LFSR is loaded with the seed value (11111111). In this method the LFSR is gated (clk) by the two counters i.e., binary (q) and gray (g) counter, when the these counter reaches the count value "00000000" the LFSR is active and the output from the LFSR (out) is then XORed with the output of the gray counter. The final output of the LP-TPG is shown by the signal 'test_pattern'.

LFSR's	Conventional LFSR	MC LFSR	BS LFSR	BSMC LFSR	LP TPG
No of patterns	255	255	255	255	255
Test Power(nw)	3883.785	2885.79	6895.055	5699.287	6463.442
Longest delay path(ps)	853	939	761	882	1276

4. Conclusion

In the process of comparing 8-bit pattern generators for Logic Built-In Self-Test (LBIST), we have discovered important factors that have a direct bearing on the effectiveness and dependability of integrated circuit (IC) testing. Our results emphasize the significance of power consumption and fault coverage as critical parameters in the design and choice of 8-bit pattern generators. The designs we examined have different strengths and limitations, as our fault coverage study has shown. Making educated selections about IC testing methodologies requires a thorough grasp of each pattern generator's capacity to identify various fault kinds. Furthermore, our research has shown that power consumption is a serious issue, particularly when it comes to contemporary integrated circuits (ICs) where energy-efficient functioning is essential.

5. References

1] J. Matsushima, Y. Maeda and M. Takakura, "CooLBIST: An Effective Approach of Test Power Reduction for LBIST," 2008 17th Asian Test Symposium, Hokkaido, Japan, 2008, pp. 264-264, doi: 10.1109/ATS.2008.36.

2] R. Pandey, S. Pandey and C. S. M. Shaul Hammed, "Security in Design for Testability (DFT)," 2017 IEEE International Conference on Computational Intelligence and Computing Research (ICCIC), Coimbatore, India, 2017, pp. 1-4, doi: 10.1109/ICCIC.2017.8524138.

3] Gary K Yeap, "Practical Low Power Digital VLSI Design", ISBN 0792380096, Springer US, 1997.

4] T. Lang, E.Musoll, and J. Cortadella, "Individual flipflops with gated clocks for low power datapaths", IEEE Trans. Circuits Syst. II, Analog Digit. Signal process. Vol. 44, no. 6, pp. 507, Jun. 1997.

5] Praveen Kumar Aggarwal, Vandana Yadav, Arti Noor, "Pattern generation task for Circuit Under Test", International Journal of Engineering Research and

Applications, vol. 1, Issue 2, pp. 190-193.

7] Praveen Kasunde, Shiva Kumar, M. Z. Kurian, "Improved Design of Low Power TPG Using LP-LFSR", International Journal of Computer and Organization trends, volume -102-106, May 2013.

8] Tehranipon M, Nourani M, and Ahmed N, "Low Transition LFSR for BIST- Based Applications", IEEE 14th Asian International Synopsium 2005, pp- 138-143, Dec. 2005.