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Comparative Analysis of Alu Architectures Using Majority and Reversible Logic Gates

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Abstract - Arithmetic Logic Units (ALUs) are critical components determining the performance and power efficiency of digital systems. This paper presents a comparative study of ALU architectures designed using reversible logic gates (Peres, Fredkin, and CNOT) and majority logic gates. While reversible logic aims to minimize energy dissipation by avoiding information loss, practical implementations often introduce overhead via garbage outputs. In contrast, majority logic offers a compact structure for efficient Boolean realization. Both designs were synthesized on an FPGA platform using Verilog. The results indicate that the majority-gate-based ALU achieves an 8.0% reduction in logic utilization and a 4.72% reduction in power consumption compared to the reversible-gate-based design. Thus, majority-gate ALUs are better suited for low-power and area-efficient VLSI applications.

Key Words: ALU, Reversible Logic, Majority Logic, Low-Power VLSI, FPGA, Verilog

1.INTRODUCTION

The Arithmetic Logic Unit (ALU) is the core determinant of execution speed and energy efficiency in modern processors. Conventional CMOS implementations often suffer from significant power dissipation due to information loss and high switching activity. To address these challenges, researchers have explored alternative logic styles like reversible and majority logic.

Reversible logic ensures a one-to-one mapping between inputs and outputs to theoretically eliminate energy loss associated with Landauer's principle. Majority logic, however, determines output based on the majority value of inputs, allowing for functionally complete sets that use fewer components than traditional networks. This work evaluates both paradigms under identical synthesis conditions to assess their practical feasibility

2. METHODOLOGY

Reversible Logic-Based ALU

The reversible ALU was constructed using Peres, Fredkin, and Controlled NOT (CNOT) gates.

- **CNOT Gate:** Used for bit inversion and XOR operations
- **Fredkin Gate:** Utilized for reversible multiplexing and data selection.
- **Peres Gate:** Forms the core of the reversible full adder due to low quantum cost.

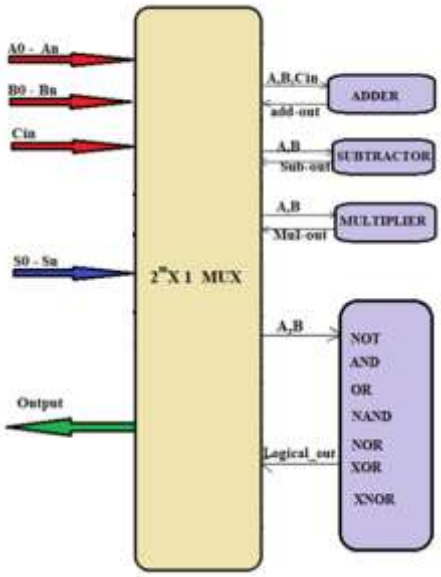

Fig-1: ALU Architecture

Majority-Gate-Based ALU

The majority-gate design focuses on minimizing logic depth and gate count. It utilizes the majority function M(A, B, C) = AB + BC + CA to realize arithmetic and logic blocks.

Adder Design: The carry output is generated directly via a majority gate: Carry = M(A, B, Cin)

Logic Unit: Fundamental operations like AND (M(A, B, 0)) and OR (M(A, B, 1)) are realized with reduced interconnection complexity

RESULTS AND DISCUSSION

The designs were described in Verilog and synthesized using Xilinx Vivado. Performance was evaluated based on Area (Look-Up Tables) and Power consumption

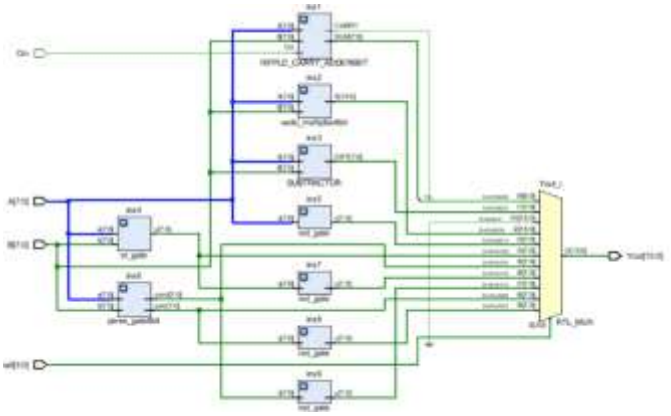

Fig-2: RTL Schematic of ALU using reversible gates

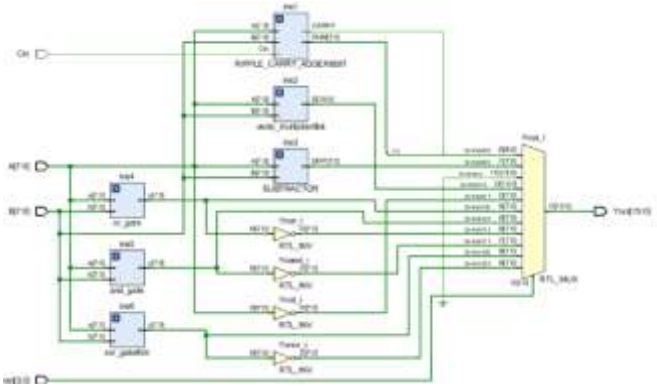

Fig-3: RTL Schematic of ALU using majority gates

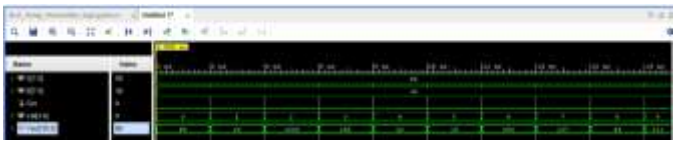

Fig-4: Simulated wave form of ALU using reversible gate

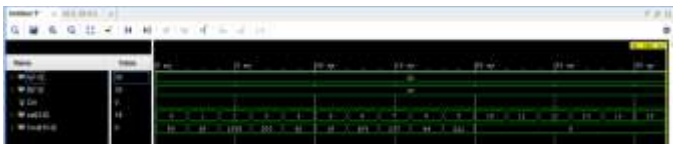

Fig-5: Simulated wave form of ALU using majority gates

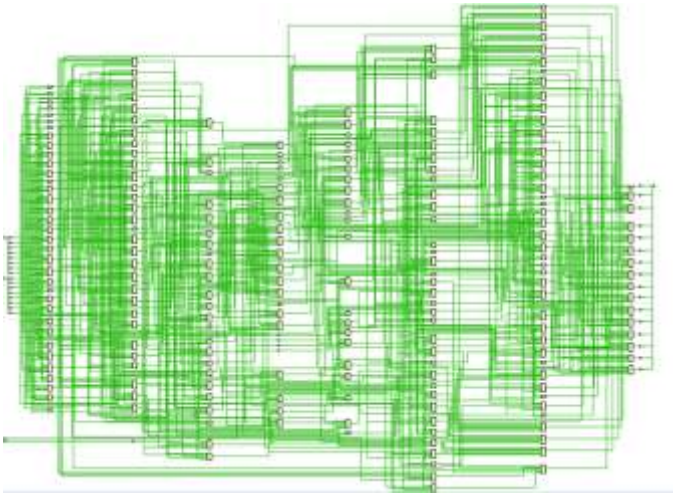

Fig-6: Technology schematic of ALU using reversible gates

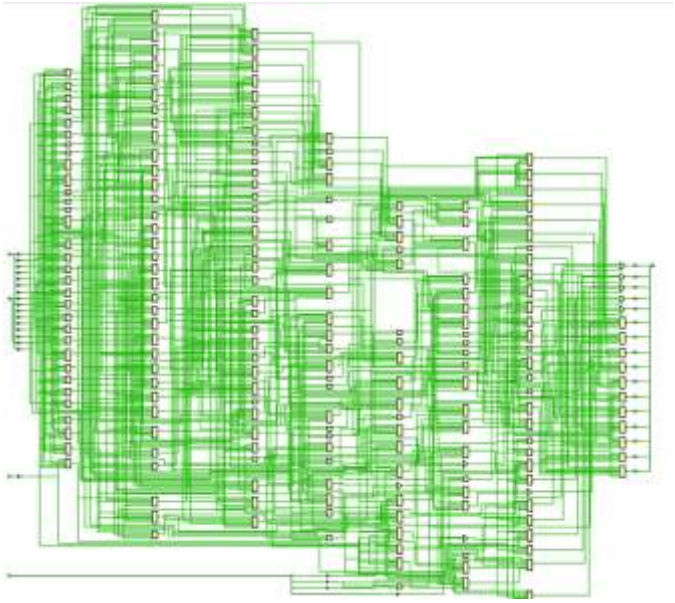

Fig-7: Technology schematic of ALU using majority gates

Parameter	ALU (Reversible Gates)	ALU (Majority Gates)
No. of LUTs	175	161
Total Power (mW)	7.569	7.212

Table -1: Parameter Comparison

Synthesis results demonstrate that the majority-gate-based ALU is more efficient, reducing area by approximately 8.0% and power by 4.72%. While reversible logic is theoretically superior, the practical need for garbage outputs and ancilla bits increases switching activity and routing overhead on standard FPGA platforms.

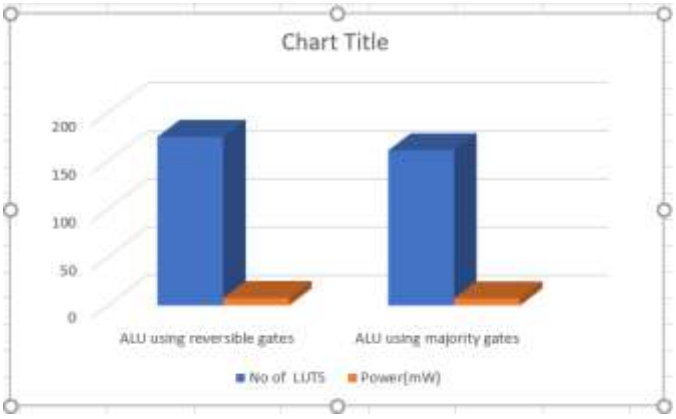

Fig-8: LUT and Power comparison bar graph

CONCLUSIONS

The comparative analysis confirms that majority logic provides a more feasible solution for current low-power digital systems. The majority-gate-based ALU outperformed the reversible-logic design in both area and power metrics during practical FPGA implementation. Future work will involve scaling these architectures to 32-bit designs and exploring hybrid logic structures.

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