Comparative study of shift register using flip flop and latches

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***Abstract*—This paper discusses a comparison of shift registers that use flip-flops and latches. In VLSI circuits, the basic building blocks are flip-flops and latches. Consider the latches and flip-flops in a shift register.As latches are the smallest circuit of flip-flops, they are used instead of flip-flops to save space and electricity. This paper compares numerous shift register approaches based on latches and flipflops. The shift register is built with numerous non overlap delayed clock pulsed latches based on the results for a more accurate manner of consuming less area and power. Multiple non overlap delayed pulsed clocks are applied to the latches to avoid the timing problem in shift registers when latches are used instead of flip-flops. Each latch is enabled by a standard 2:4 decoder. This is a good way for making a low-power, small-area shift register in a VLSI circuit.**

Keywords—Shift Register,Latches,Flipflop,Decoder.

INTRODUCTION

High-speed performance is one of the most important factors in modern Very Large Scale Integration (VLSI) technology. It is possible to achieve very little data processing delay by incorporating an emerging concept of high speed in VLSI design. The clock frequency at which high-performance integrated circuits operate has traditionally been used to define them. Furthermore, delay calculation is handled by various design phases such as logic synthesis, layout (placement and routing), and mapping. As a result, high-speed design can improve the performance of all of the preceding design stages. The clock signal is enforced by synchronising elements such as Flip-Flops (FF) or latches, which operate in response to the clock pulses applied.

I. SHIFT REGISTERS

A. Shift Registers

In a VLSI circuit, the fundamental building block is a shift register.

Shift registers are widely used in a variety of applications, including digital filters, communication receivers, and image processing integrated circuits. To process large image data in image processing ICs, the word length of the shifter register has recently increased as the size of the image data continues to increase due to the high demand for high quality image data. A 4K-bit shift register is used in an image extraction and vector generation VLSI chip. A 2K-bit shift register is used by a 10-bit 208 channel output LCD column driver IC. A 45K-bit shift register is used in a 16-megapixel CMOS image sensor. The area and power consumption of the shift register become important design considerations as the word length of the shifter register increases. A shift register's architecture is quite simple. An N-bit shift register is made up of N data flip-flops connected in series.

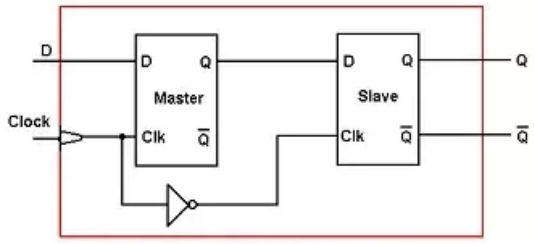
A flip flop or a latch can store a single bit of binary data, such as 1 or 0. If many bits of data must be stored, multiple flip-flops or latches are required. Because a single flip-flop stores one bit, n flip-flops are connected in order to store n bits of data. A register is a device used to store information in digital electronics.

Flip-flops are used to build registers. However, it requires a large amount of power and area; to reduce the power and area, the large flip-flops are replaced by small flip-flops known as pulsed latches. Multiple non-overlapping delayed circuits are used to solve the timing problem of pulsed latches. This paper discusses a comparative study of shift registers based on flip-flops, latches, pulsed latches, and decoder enabled pulsed latches and using pulsed latches, this paper proposes a low-power and area-efficient shift register. Instead of the conventional single pulsed clock signal, the shift register solves the timing problem by using multiple non-overlap delayed

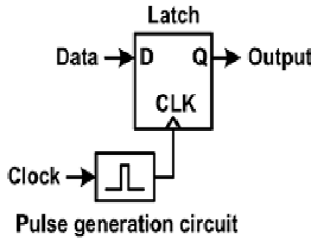
pulsed clock signals. By grouping the latches into several sub shifter registers and using additional temporary storage latches, the shift register uses a small number of the pulsed clock signals.

B. *Flipflops*

Latches and flip-flops are the building blocks of sequential circuits, which can be constructed from logic gates. Latches are simple and small-sized circuits. A flip-flop or a latch can only hold one bit of data at a time. The main distinction between latches and flip-flops is that a latch continuously checks the input and changes the output whenever the input changes. However, a flip-flop is a latch and clock combination that continuously checks input and changes the output time as determined by the clock. Shift registers founded typically with flip-flops consume more power and take up more space.



a.Master slave D-Flipflop



b. Pulsed Latch

The flip-flops are cascaded to form a shift register that shares the same clock, and the data from each flip-flop is passed on to the next flip-flop. Figure 1(a) shows a master-slave flip-flop with two latches that can be replaced by a pulsed latch with a latch and a pulsed clock signal (b). The pulse generation circuit for the pulsed clock signal is [1]shared by all pulsed latches. As a result, the pulsed latch's area and power consumption are nearly half that of the master-slave flip-flop. It is clear from this that the pulsed latch is an appealing solution for small area and low power consumption. Figure 2 shows a timing problem when using pulsed latches. Figure 2 (a) depicts the arrangement of such a circuit, and Figure 2 (b) depicts the result wave form (b). The timing issue between latches in a shift register is depicted by the operational wave form.

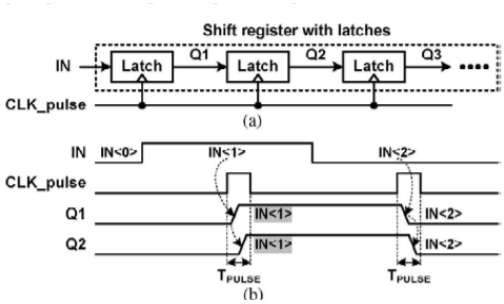


Fig. 2 Shift register with latches and a pulsed clock signal. (a) Schematic. (b) Waveforms

II. PROPOSED METHODS

A. ***Method I:***

One of the solutions to solve the timing problem is to add a delay circuit between each latches. Fig.3 (a) shows such arrangement and fig.3 (b) corresponding result wave form and from the wave form Q1 and Q2 are change in the Tpulse duration.

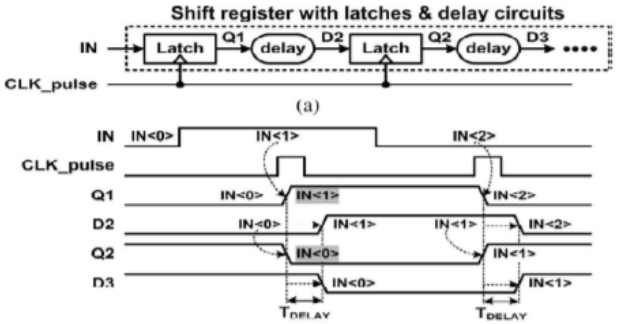


Fig. 3 Shift register with latches, delay circuits, and a pulsed clock signal. (a) Schematic. (b) Waveforms

B. ***Method II***:

1. Another solution is to add delay in clock signal, ie. Multiple non overlap delayed pulsed clock is used to enables each latch. Fig.4 (a) shows the architecture and (b) is the output wave form. From this wave form it is understood that the timing problem is eliminated.

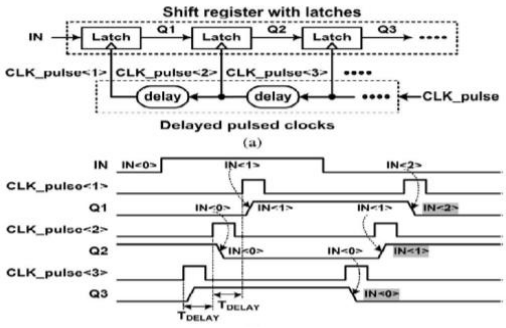


Fig. 4 Shift register with latches and delayed pulsed clock signals. (a) Schematic. (b) Waveforms

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But method I and method II solves the timing problem but takes more power and area because of the delay circuits. Here the number of delay circuits is large.

C. Method III :

Byung-Do Yang introduces a shift register based on delayed pulsed latches and can reduce power and area. The arrangement of such a method is shown in fig.5(a) and corresponding wave form fig.5(b).

2.

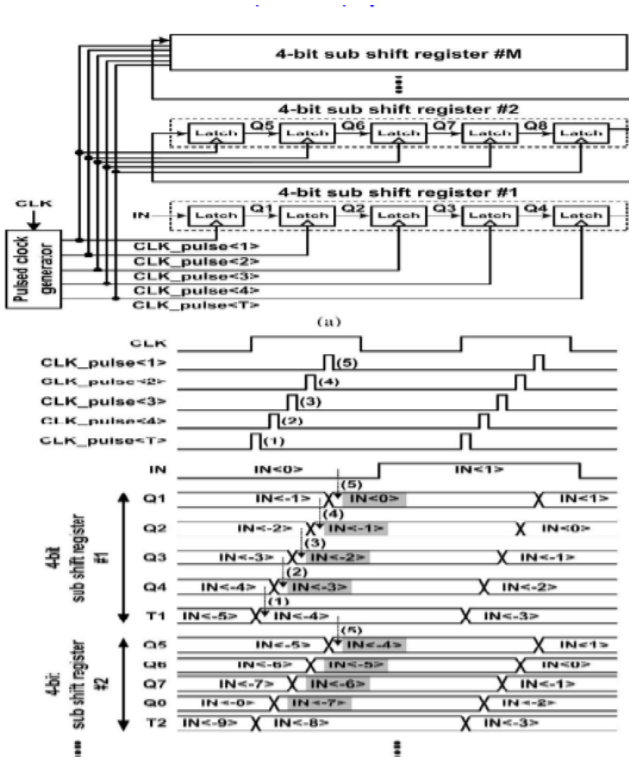

Fig.5 shift register. (a) Schematic. (b) Waveforms

D. *Detailed Analysis of shift register using latches*

Figure 6 depicts the proposed shift register design, which employs a decoder-enabled pulsed latch. Here's an example of a 16-bit shift register divided into four sub-shift registers, each with four latches. The input signal (IN) is applied to the first latch in the first sub shift register, and the output is denoted by the letters Q1-Q16.

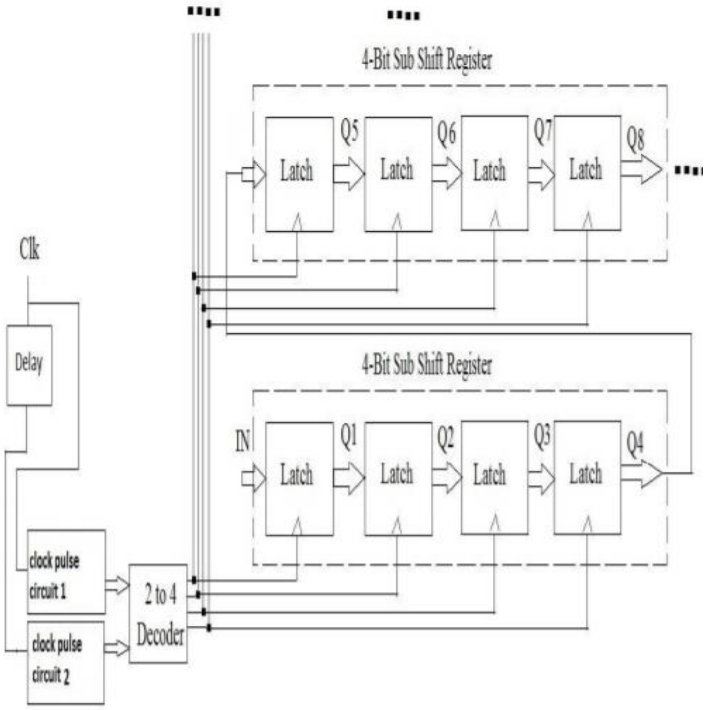

Fig. 6 proposed shift register using decoder enabled pulsed latch

The architecture of the suggested shift register with decoder activated pulsed latch is shown in Figure 6. Here's an example of a 16-bit shift register divided into four sub-shift registers, each with four latches. As shown in fig.7, the suggested solution eliminates the temporary storage latches and modifies the pulsed clock generator circuit. Because the pulse duration of the pulsed clock generator is changed using a 2:4 decoder, the output from the decoder will avoid data loss, hence no temporary storage is necessary. The first latch in the first sub shift register receives the input signal (IN), and the outputs are labeled Q1-Q16.

By utilizing a decoder to replace a delayed clock pulse generator, this solution minimizes the number of delay circuits.

A binary decoder is a logic device that turns a binary integer value to a pattern of output bits using combinational logic. It can convert binary data from n input signals to up to 2n distinct output signals. A decoder in this application has two inputs and four outputs, as indicated in table 1.

Truth Table

A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Table1-Truth Table of 2:4 Decoder.

As a clock signal, a general 2:4 decoder is employed in this suggested shift register. Two clock pulse circuits are employed, with the main clock applied immediately to clock pulse circuit 1 and then connected to clock pulse circuit 2 after a delay. The clock pulse circuit is made up of a delay, an inverter, and an

AND gate; the output of the clock pulse circuit is then coupled to a 2:4 decoder, yielding D3,D2,D1, and D0.

A0 and A1 are inputs And D0-D3 are outputs, both inputs are 0 then get D0 as high, A0 is 0 and A1 is 1 then D1 is high, A0 is 1 and A1 is 0 then D2 is high and both inputs are 1 then get D3 is high. These outputs act as delayed clock pulses for the proposed shift register. The input of decoder, A0 and A1 signals are generated by the clock pulse circuits from the main clock.

E. Power Discussion

From the comparison table 2, the proposed shift register based on decoder enabled pulsed latch can save more power and area than conventional shift register using flip-flops. The shift register based on latches are more suitable for low power VLSI applications and it also reduces the chip size.

parameter	Shift register with flip-flops	Shift register with pulsed latches	Proposed shift register
Power(mW)	134	124	104
Area(gate count)	136	32	30

III. RESULTS AND CONCLUSIONS

According to the results of the analysis, the shift register with latches can reduce area and power. The proposed 16-bit shift register consumes more power and area than conventional shift registers based on flip-flops and other latch-based methods.

The proposed shift register which will be discussed in the second phase is built with pulsed latches, and each latch is enabled by a decoder. The 16/32 bit shift register is divided into four 4/8 bit sub shift registers, and the main clock is changed to delayed non-overlap multiple pulses to solve the latch timing problem. When two clock pulse circuits and a 2:4 decoder are used to generate delayed clock pulses, area and power can be reduced more efficiently. This arrangement is less complicated and simpler than other traditional methods. When compared to conventional shift registers used by flip-flops and other pulsed latches methods, it can save more power and area.

Efficient area and power utilization of shift registers using pulsed latches is proposed in this paper. By replacing flip-flops with pulsed latches, the shift register saves space and power. Instead of a single pulsed clock signal, the timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals. By grouping the latches to several sub shifter registers and using additional temporary storage latches, a small number of the pulsed clock signals are used.

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6. Efficient Area And Power Utilization of Shift Register using Pulsed Latches MOHAMMED YASMEEN , A. ARUN KUMAR,ISSN 2322-0929 Vol.04, Issue.12, November-2016, Pages:1271-1276