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Complex Test Pattern Generator (CTPG)-an extension of ATPG and its Application for Highly Compacted Test Sets

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***Abstract*— Integrated chips or System on chip devices act as the backbone for numerous evolutions in the currently growing technology world. Integrated ICs are helpful to store massive data, to process it effectively, to formulate the compact memory for multi-tasking systems. Soc devices need to be tested before evaluating a digital architecture bare chip testing is applicable in most of the core development platforms where the system on ship platform undergoes various test processes to check the Silicon level fabrication quality before developing a Digital circuit in it. The proposed system is focused on creating an inbuilt test platform with reconfigurable architecture and optimised test pattern generation model to make the soc validation more accurate. The presented system not only focused on optimising the test patterns but also provided a Complex test set to solve the problems in test modules. Here Complex pattern test generator with enhanced version of built-in self-test is implemented. The presented system is analysed by comparing the performance of the developed test model with various FPGA platforms in terms of power area utilisation and latency.**

Keywords*— *Low power design, System on chip (SoC), Built in self-test (BIST), automatic test pattern, soc validation.

I. INTRODUCTION

Built in sectors is the process of developing a set of rules and Hardware framework integrated within the soc platforms to Test the functionality of circuits using various test sets. Built-in self-test is commonly called as design for testability technique that provides electrical testing of on -chip memory. The concept of built-in self-test is applied to all kinds of systems on ship integrated devices to protect the chip from external as well as internal attacks. Before developing a Digital circuit into the fabricated ICS, the system on ship devices needs to be completely tested by providing various test sequences. the main drivers required for global development of built-in self-test techniques or formulated with automatic test pattern generation. Complex integrated circuits or tested with automatic test Pattern Generator to test to the bar I see that should pass all Complex test capability. A built -in self-test is used to create a special test platform that eliminates various testing issues.

In the existing frameworks various automatic test Pattern Generator methods are implemented that satisfy the recoverment of the test set applicable for on optimised applications. the compact test set or required to be reduced to compress the time taken for test sequences. The complex problems need to be reduced by solving the test pattern complexity. Built- in self-tests act as a solution for critical circuit related problems such as butter side channel attacks glitches external pin-oriented noise pin to pin delay fault generation and electrical impulses. various advantages of built-in self-tests or discussed in existing articles. the self-test platform or required to make low-cost testing solutions for all structures of integrated ICs, to give shorter test times if the properly aligned built in self-test platform is incorporated. easy access and support to user designs. capability of the system to produce electrical impulses that could test any kind of environment. the advantage required to make the consumer demands and satisfy the test sequence appropriately. the major disadvantages of implementing The Automatic test pattern generation inside the system on ship platform or additional fabrication cost or included. it reduces the accessing time to the BIST every time the fault is being occurred. automatic hence the automated system needs configurable application that should not coincide with the existing design outcomes. The issues need to be considered while developing the system architecture or discussed below.

The fault needs to be covered completely when implementing the built- in-self test. The test area need to be occupied by the built interceptors need to small external support or required to The reconfigurable memory based built in self-test need to be altered based on the complexity of the data and produce the compact test sequences that should not be the commonly distributed types of built in self-test or logic building self-test that work only on logical analysis where memory built in self-test which considers random testing to the memory using pseudo random testing marching testing checker board testing and various other test sequences to test the memory. Multiple input signature registers-based technique considered the signature analysis ends the pattern of Signature is fetched for testing that should be verified after the marching algorithm. marching is a kind of algorithm which is used to test the complete system on chip memory by writing various patterns of data in the form of March fast. how the March fast happens left to right and right to left in the similar way the system on ship platform gets returned by the input test data from left to right and right to left like March fasting. Checkerboard testing is a kind of alternative writing

of zeros and ones completely into the memory of the system on chip to check any internal fault occurring in the developed platform. Built-in self-test has become one of the fast and alternative solutions to various electrical impulse problems that secure the internal integrated ICS from various drawbacks. The advantages of memory based self-testing includes functionality speed is increased robust memory design reduces the time taken to solve the logical issues testing time is reduced.

Automatic Test pattern generation

ATPG stands for automatic test pattern generation that processes the digital test circuits to get programmed with several test patterns fetched into the circuit and tested with various kinds of logical problems. The automatic test pattern process includes fault coverage fault modelling test pattern generation test pattern simulation test pattern application etc. fall to modelling is the process of creating a type of fault that should be gathered and tested with the created model. ATPG generation is a kind of generating automatic test inputs that should be fetched into the FPGA circuits to check the functionalities.

Test pattern simulation is used to check the effectiveness of the outcome of an integrated circuit by adding up various patterns and simulated in the FPGA software.

Test pattern application automatic application installed inside the FPGA to test the circuit and identify the fault occurring in it. The automatic test Pattern Generator plays an important role in digital circuits and ensures the functionality of the circuit to improve the quality and identify potential issues.

- The proposed system considers the simulation of automated test pattern generation and simulation framework using FPGA.
- The proposed approach considers Memory based an optimized model for continuous test and validation of SOC internal blocks.
- To test the results in terms of Area efficiency, Latency, and Power consumption, the architecture performance is compared with several FPGA architectures.

The remainder of the essay is organised as an exploration of Section II's extensive review of the literature. In Section III, we explore system design methodologies, tool selection, and problem identification. Section IV discusses the system architecture, in-depth methodology, and module development stages. Future improvement is discussed as the study concludes.

K.C. Yang et al. (2019) The author provided a framework for test compression and automatic test pattern development for probabilistic density circuits. The presented system considered an automatic test pattern generation algorithm for analysing the probabilistic enabled digital circuits in terms of propagation delay pattern repetition and accumulation of power. the performance of the system with ISCAS 89 benchmark circuit and achieved the performance in terms of propagation delay compared with the existing circuit 24% reduced time compared with the greedy method.

P. Wang et al. (2019) the author presented automatic test pattern generation Framework with multiple sources of structure fault problems or analyses. The presented system considers the Digital circuit that produces various structure faults in different situations and finds out the fault analysis model by implementing The Automatic test Pattern Generator. The benchmark circuit is ISCAS 89 and IWLS 2005 circuit or considered for making the compact it is pattern generation and acceptable runtime outcome for the generator fault.

K. H. Chen et al. (2019) The author presented a reconvergence circuit to reduce the automatic test pattern generation runtime problems. consider the back tracking method to analyse the fault occurring in the FPGA. The system considers data from our test ability model that produce better outcomes of automatic test pattern generation and provide a clear justification of fault coverage especially during deep logic generation. approach by implementing the reconvergence model.

Y. C. kung et al. (2018) The author presented automatic test pattern generation Framework using DC and ac fault. and implemented AC and DC fault coverage Framework. The presented system is very compact and produces the pattern of outcome that produces less processing time and produces the processing model that covers most of the fall tuckering and the digital circuits. and ITC 199 circuits or considered for analysis. In comparison with various conventional methods of automatic test pattern generation 14.5% the time reduction is made by the ISCAS 89 circuit 11.26% by IWLS 05 circuit and 13.69% reduction by ITC circuit is achieved. The presented system completely covers the fault coverage and degrades the time taken for testing the circuit.

T. Strauch et al. (2019) the presented system considers a functional test analysis platform using Gate in inherent fault (GIF) model. The Random Access provided by the presented approach covers most of the fault fault coverage. RTL code is generated with detailed automatic test pattern generation flow with three essential benefits of multiple cycle of test Provided by the RTL circuit using Gate inherent fault model.

II. SYSTEM DESIGN

The proposed system architecture is put into practise using Register transfer logic (RTL) code generated with behavioural programming in Mentor Graphics Modelsim tool for simulation of ATPG with optimized test framework (OTF). the proposed approach considers the existing challenges in developing the ATPG applications such as extended propagation delay, complex process and intermediate call backs in BIST cells are overcome here using optimized test framework that adopt the environment requirements and fetch the test patterns.

III.METHODOLOGY

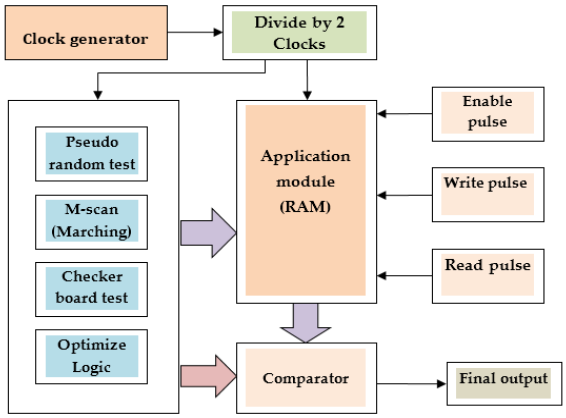


Fig. 1. shows the system architecture developed in VHDL configurable logical blocks using behavioural modelling in FPGA.

The test pattern generator module is the core component of the analogue built-in self-test (BIST). A built-in self-test is carried out by a sample module that is nothing more than a random-access memory (RAM) in the proposed system. In order to test the circuit, different advanced test cases are provided for the BIST RAM. We are applying the necessary experiments to the BIST Smash using the test design generator.

Design of control unit: This module is implemented for regulating all actions in the RAM built-in self-test.

- The control unit makes the command over the composition, perusing, tending to and examination and so on. in the integrated self-test. Additionally, the control unit will make decisions regarding the BIST's process, increasing efficiency.
- Design of Test Pattern Recorder (TPR): During the built-in self-test, the input data will be recorded in the RAM memory regions.

The comparator in the BIST (built-in self-test) system obtains data both from the RAM module and directly from the input with the aid of the BIST controller.

After the comparison, the comparator's output is compared to the inputs, and the BIST RAM is tested using various advanced test cases.

In order to save energy and increase space efficiency, performance is measured in this manner. Additionally, the main module combines all the sub modules, and output signals are directed to the appropriate ports in accordance with the FPGA device.

IV. RESULTS AND DISCUSSIONS

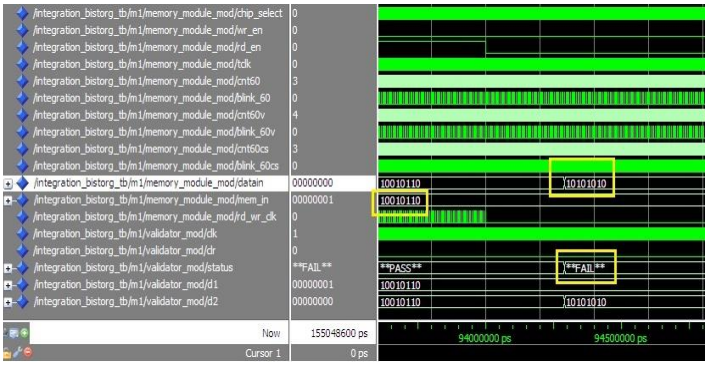


Fig 2. Simulation result - Test outcome

Fig. 2. Shows the result of the Modelsim tool on test outcome in the initial testing phase. the global clock is defined as variable clk, the global reset or the hardware reset of the FPGA is determined here as clr. The FPGA system may not initiate any operation without the triggering clock and reset for clearing the previous state.

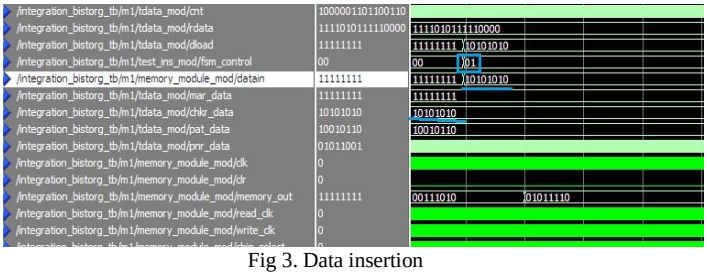


Fig 3. Data insertion

Fig. 3. Shows the system result on data insertion after the test pass. the four types of test patterns are generated separately

by the test generator module. the generator module kept dynamically reconfigurable throughout the system design.

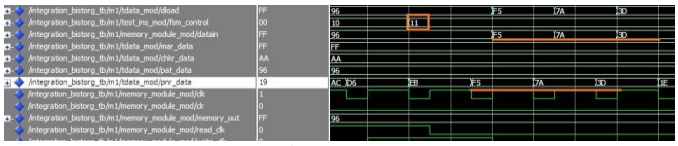


Fig 4. Insertion of Pseudo-random test patterns

Fig 4. shows the insertion of PSNR test patterns. the pseudo random pattern generators or otherwise called as repeated random pattern generators are helpful to make repeated random codes which are predictable

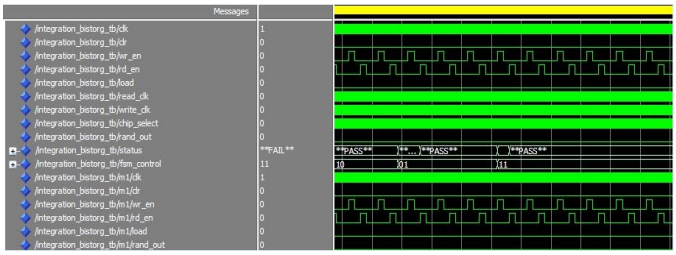


Fig 5. OTF automated test sequence

Fig 5. shows the OTF enabled automated test pattern generation

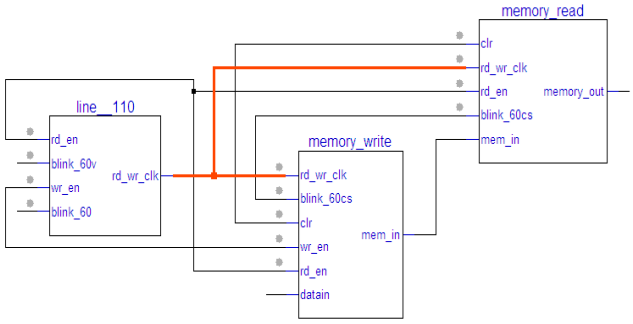


Fig 6. Internal architecture Memory BIST

Fig 6 shows the internal digital architecture generated by the memory BIST.

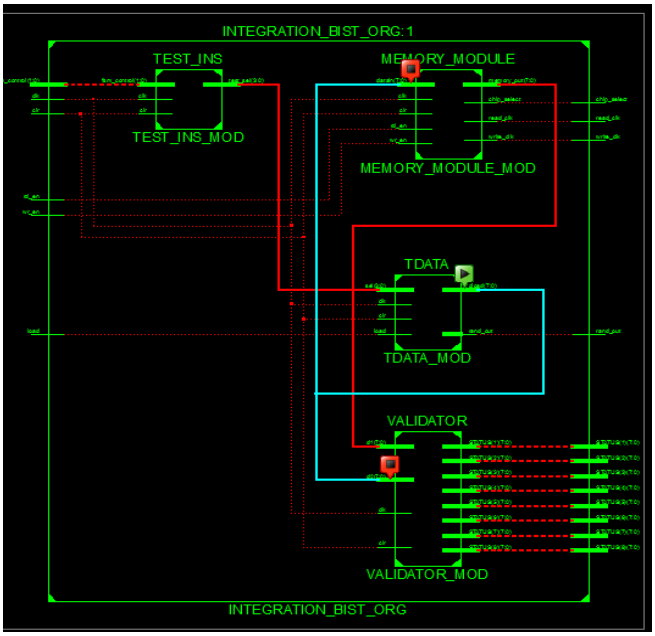


Fig 7. XILINX RTL schematic of OTF model

Table 1. Latency report of proposed OTF model

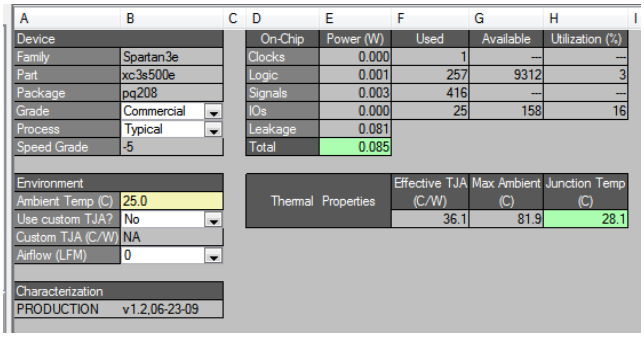
Slno	Summary of Delay	Level
1	Logical Delay	3.683 ns
2	Routing Delay	0.451 ns
3	Total Latency (Fan-out=3)	4.13 ns

Table 1 shows the total latency of proposed OTF model, where the logical delay of 3.683 ns achieved, Routing delay of 0.451 ns is achieved, with fan-out control of 3 for XILINX Spartan 3E FPGA device using simulation.

Table 2. device utilization summary

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	117	9,312	1%
Number of 4 input LUTs	133	9,312	1%
Number of occupied Slices	115	4,656	2%
Number of Slices containing only related logic	115	115	100%
Number of Slices containing unrelated logic	0	115	0%
Total Number of 4 input LUTs	195	9,312	2%
Number used as logic	133		
Number used as a route-thru	62		
Number of bonded IOBs	75	66	113%
IOB Flip Flops	21		
Number of BUFGMUXs	2	24	8%
Average Fanout of Non-Clock Nets	2.47		

table 2. shows the detailed device utilization summary after the implementation and post synthesis with XILINX SPARTAN 3E family FPGA.



Device		On-Chip	Power (W)	Used	Available	Utilization (%)
Family	Spartan3e	Clocks	0.000	1	---	---
Part	xc3s500e	Logic	0.001	257	9312	3
Package	pq208	Signals	0.003	416	---	---
Grade	Commercial	IOs	0.000	25	158	16
Process	Typical	Leakage	0.081			
Speed Grade	-5	Total	0.085			

Environment		Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
Ambient Temp (C)	25.0		36.1	81.9	28.1
Use custom TJA?	No				
Custom TJA (C/W)	NA				
Airflow (LFM)	0				

Characterization	
PRODUCTION	v1.2,06-23-09

Fig 8. Power report

Fig 8 shows the power analysis report of the proposed model. the system achieved 4 mW of power consumption provided by the proposed OTF method. further the SPARTAN XC3S500E model is opted for testing. further expansion of the work includes more optimized devices, and circuits are tested.

V. CONCLUSION

In order to improve the accuracy of SOC validation, the proposed system focuses on developing an integrated test platform with an optimized test pattern generation model and reconfigurable architecture. In addition to focusing on optimizing test patterns, the presented system offered a Complex test set for resolving issues in test modules. This complex pattern test generator uses an improved version of the built-in self-test. The developed test model's performance against a variety of FPGA platforms in terms of power area utilization and latency is used to analyse the presented system.

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