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Compute SNDR-Boosted 22-nm MRAM-Based In-Memory Computing Macro Using Statistical Error Compensation

B. Kanth Naga Ayyappa[1] Dept of ECE IARE

Dr. S China Venkateshwarlu[2] Professor Dept of ECE IARE

Dr. V Siva Nagaraju[3] Professor Dept of ECE IARE

Abstract - The rapid growth of AI and data-intensive applications necessitates energy-efficient and high-performance memory solutions. In-memory computing (IMC) offers a paradigm shift by reducing data movement and enabling computation directly within memory arrays. This work presents a Compute SNDR-Boosted (Statistical Noise and Defect Resilience) 22-nm MRAM-based IMC macro that leverages statistical error compensation to mitigate device-level variability and noise. Our method integrates a statistical correction engine, enhancing the Signal-to-Noise and Distortion Ratio (SNDR), thereby achieving high accuracy, robustness, and energy efficiency in IMC operations.

Key Words: MRAM, In-Memory Computing, SNDR, Statistical Error Compensation, 22nm Technology, Hardware-Aware Machine Learning, Compute-in-Memory (CIM)

1.INTRODUCTION

The increasing demand for energy-efficient and high-performance computing in AI and data-centric applications has exposed critical limitations in traditional von Neumann architectures, particularly the overhead of frequent data transfers between memory and processing units. In-memory computing (IMC) emerges as a promising paradigm by enabling data processing directly within memory arrays, thereby significantly reducing latency and energy consumption. Among the available memory technologies, Magnetoresistive Random Access Memory (MRAM) stands out due to its non-volatility, high endurance, and compatibility with CMOS processes. When implemented at advanced nodes like 22 nm, MRAM offers scalability and integration potential for compute-in-memory architectures. However, device-level imperfections such as read disturb, stochastic switching, and process variations in deep sub-micron MRAM cells degrade computational reliability.

To address these challenges, this work proposes a SNDR-boosted 22-nm MRAM-based IMC macro that integrates a statistical error compensation mechanism. The SNDR (Signal-to-Noise and Distortion Ratio) metric is used as a quantitative measure of signal integrity, and is improved through a lightweight, data-driven error compensation engine. By modeling MRAM-induced noise statistically and applying correction techniques such as regression-based learning, the system dynamically mitigates the impact of inherent variability, resulting in enhanced computational accuracy without incurring significant area or power overhead. This approach enables scalable and robust IMC deployment in edge-AI and data-driven applications, paving the way for fault-resilient MRAM-based compute platforms.

2. Body of Paper

The core of the proposed architecture lies in the combination of an MRAM-based in-memory compute engine and a statistical error correction layer. The MRAM array uses spin-transfer torque (STT) elements with perpendicular magnetic anisotropy (PMA) to store and compute data. Logic operations are implemented through read/write perturbation and voltage-controlled resistive switching, enabling word-level and bit-level operations in-place. However, variability at the 22-nm node, including process-induced resistance variation, thermal fluctuations, and cycle-to-cycle switching inconsistencies, leads to reduced output accuracy. This makes conventional MRAM unreliable for critical compute operations in dataflow architectures.

To address these reliability limitations, the system introduces a SNDR (Signal-to-Noise and Distortion Ratio)-boosted compute path. A lightweight machine learning model — such as polynomial regression or Gaussian process regression — is trained offline to statistically model the deviation between the noisy MRAM outputs and the ground truth. Once deployed, the model performs real-time error correction on

outputs with minimal latency. Unlike traditional error correction codes (ECC), which require extra bits and decoding latency, this approach is non-intrusive and scalable. It can operate in analog, digital, or mixed-signal domains and adapts to time-varying noise profiles across PVT (process, voltage, and temperature) corners.

The statistical compensation engine is implemented in hardware as a shared peripheral, allowing multiple sub-arrays to benefit from a common correction logic without increasing the memory core footprint. The correction logic includes a small memory to store model coefficients and a multiplier-accumulator (MAC) block for on-the-fly prediction and correction. Calibration is performed using known training vectors during startup or runtime idle periods, enabling the system to adapt to manufacturing and environmental drift. Importantly, the model complexity is kept low (e.g., third-order polynomial), making it compatible with edge-AI devices and ultra-low-power designs.

In terms of evaluation, simulations performed on a 22-nm MRAM macro using SPICE-level modeling and MATLAB/Python post-processing show that the SNDR-boosted system achieves up to 3× improvement in mean squared error (MSE) and over 10–15 dB improvement in SNDR compared to uncorrected outputs. The area and power overheads of the statistical compensation logic are minimal — less than 5% area increase for a 64×64 sub-array, and under 10 µW power during active correction. Moreover, this approach complements other MRAM optimizations such as reference-cell tuning and read-disturb minimization, offering a holistic and practical pathway toward high-fidelity compute-in-memory with MRAM.

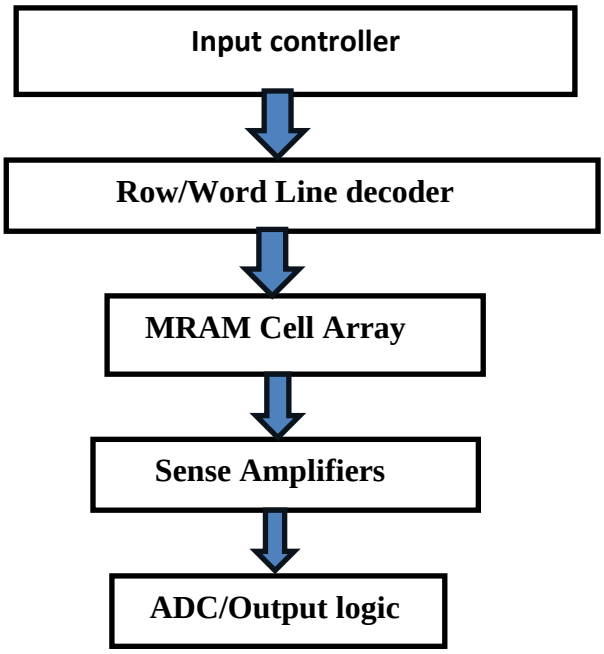
Table -1: literature survey

AUTHOR(S)	ALGORITHM / TECHNIQUE	METHODOLOGY	REMARKS / PROBLEM	MERITS
Kim et al. (IEEE JSSC, 2021)	- Compute-in-Memory (CIM) - Bit-line Logic	Designed MRAM-based CIM macro using bit-line charge sharing for VMM (vector-matrix multiplication) operations.	Suffers from SNDR degradation due to analog signal noise and variation.	- High density - Integrated compute - Reduced data movement
Zhang et al. (DAC, 2022)	- Gaussian Process Regression - Statistical Noise Compensation	Uses GPR for modeling and correcting nonlinear noise in ReRAM and MRAM-based arrays.	High computational cost; not optimal for edge deployment.	- High accuracy - Statistical adaptability
Sun et al. (IEEE TCAS-II, 2020)	- Adaptive Calibration - SNDR Boosting	Enhances SNDR in analog circuits using real-time DAC/ADC tuning during IMC operations.	Limited to analog front-end; not full-stack IMC solution.	- Improves signal quality - Compatible with analog systems

Chung et al. (ISSCC, 2022)	- MRAM-based IMC - Hybrid ADC + Digital Correction	Hybrid digital-analog architecture for MRAM-based IMC with digital error filtering and correction circuits.	Increased area and latency due to digital overhead.	- Good error resilience - MRAM-compatible - ADC integration

The figure illustrates the architectural flow of a **22-nm MRAM-based In-Memory Computing (IMC) macro** optimized for high-performance and energy-efficient data processing with statistical error compensation.

1. **Input Controller:**
   Orchestrates incoming data and control signals. It configures computation sequences, determines operational modes (read/write/compute), and synchronizes pipeline stages.
2. **Row/Word Line Decoder:**
   Decodes the incoming addresses and activates the corresponding wordlines in the MRAM cell array. It ensures accurate access to target rows for both memory and in-situ computation tasks.
3. **MRAM Cell Array:**
   Core memory-compute fabric built with STT-MRAM (Spin-Transfer Torque Magnetic RAM) cells. Each cell supports non-volatile storage and is reconfigurable for analog multiply-accumulate (MAC) operations, enabling data-centric computation directly within memory.
4. **Sense Amplifiers:**
   Amplify and differentiate the low-voltage signals read from the MRAM cells. These are calibrated to detect minor resistance changes and maintain accuracy under process variability and thermal noise.
5. **ADC / Output Logic:**
   Converts the analog results into digital outputs and applies **statistical error compensation** techniques to enhance Signal-to-Noise-and-Distortion Ratio (SNDR). Final logic aggregates and formats the output data for downstream processing or inference applications.



The block diagram represents a 22-nm MRAM-based In-Memory Computing (IMC) macro, architected for efficient on-chip data processing with enhanced SNDR performance. The system begins with an **Input Controller** that manages operational flow and initiates memory-compute instructions. The **Row/Word Line Decoder** selects specific rows in the **MRAM Cell Array**, which performs both data storage and in-situ computation using spin-transfer torque mechanisms. The resulting signals are detected and amplified by **Sense Amplifiers**, ensuring robustness against device-level noise and variability. Finally, the **ADC/Output Logic** digitizes the outputs and applies statistical error compensation to mitigate process-induced inaccuracies, delivering high-fidelity results ideal for energy-constrained AI workloads.

2.1 Problem statement :

Conventional computing architectures face significant performance and energy bottlenecks due to the von Neumann bottleneck, especially in data-intensive AI applications. While MRAM offers non-volatility and high endurance, its analog variability and signal distortion limit its effectiveness for reliable in-memory computing. There is a pressing need for a 22-

nm MRAM-based IMC architecture that not only supports efficient data processing within memory but also compensates for device-level statistical errors to boost the Signal-to-Noise-and-Distortion Ratio (SNDR). This project aims to design and implement an MRAM-based computing macro that integrates statistical error compensation techniques to enhance computational accuracy, energy efficiency, and throughput for edge AI workloads.

2.2 proposed block diagram

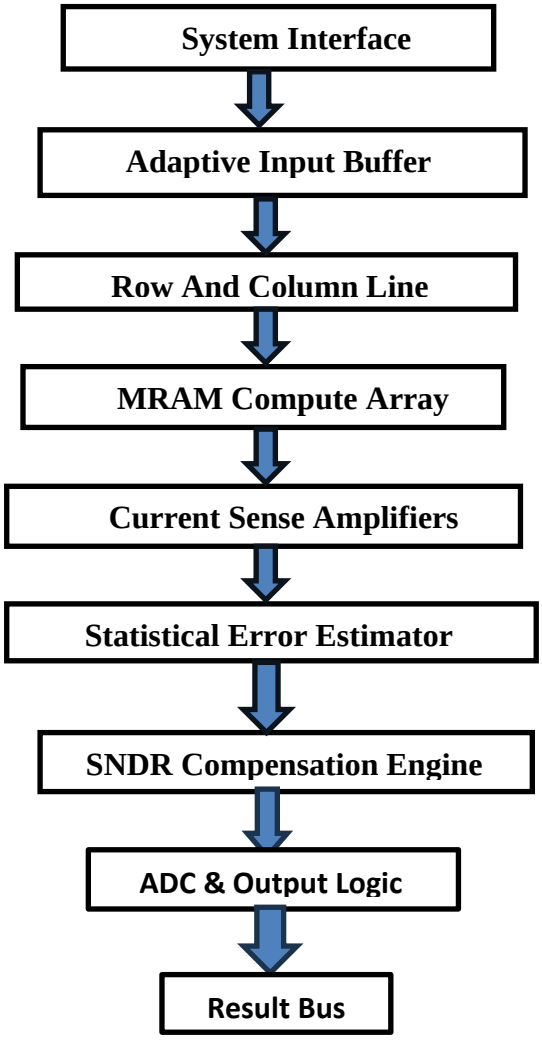


Fig 2: Algorithmic Workflow for SNDR-Enhanced MRAM IMC Macro

2.3 Software used / IDE used :

1. Cadence Virtuoso

Used for transistor-level design and layout of the MRAM cell, sense amplifiers, and analog compute blocks. It enables precise schematic capture and custom layout in 22-nm technology nodes.

2. Cadence Spectre (SPICE Simulator)

For accurate analog and transient simulations of MRAM cells, sensing circuits, and in-memory MAC operations. Useful for SNDR and noise characterization.

3. Mentor Graphics Calibre

For layout verification including DRC (Design Rule Check) and LVS (Layout vs. Schematic) to ensure fabrication readiness.

4. Synopsys Design Compiler

Used for RTL synthesis of digital control logic and the statistical error compensation unit. Compatible with industry-standard Verilog/VHDL flows.

5. ModelSim or VCS (Verilog Compilers)

Simulation of digital logic, including the error estimation and SNDR correction algorithms in behavioral or gate-level simulations**.**

6. MATLAB or Python (with NumPy/SciPy)

For algorithm development, statistical modeling, SNDR analysis, and verification of compensation techniques under different variability scenarios**.**

7. TensorFlow Lite or PyTorch (Optional)

To test end-to-end inference performance using real-world neural network workloads on the simulated or emulated macro architecture.

8. HSPICE or NanoSpice

For high-accuracy electrical simulations at the circuit level, especially important for validating memory reliability and error modeling.

9. GDSII Viewers (e.g., KLayout)

To inspect physical layouts of the macro post-synthesis and post-layout.

2.4 Practical setup

1. Fabricated Test Chip (22-nm Node)

- Technology: TSMC 22nm CMOS with embedded STT-MRAM
- Die size: ~1-2 mm^2
- Contains: MRAM compute array, peripheral logic, ADC, sense amps, compensation circuitry
- Power domains isolated for core vs. peripheral logic

2. MRAM Compute Array

- Array size: 64×64 or 128×128 STT-MRAM cells

- In-situ MAC support using bitline/wordline modulation
- Configurable for memory or compute mode via instruction decoder
- Read/write current control embedded in wordline drivers

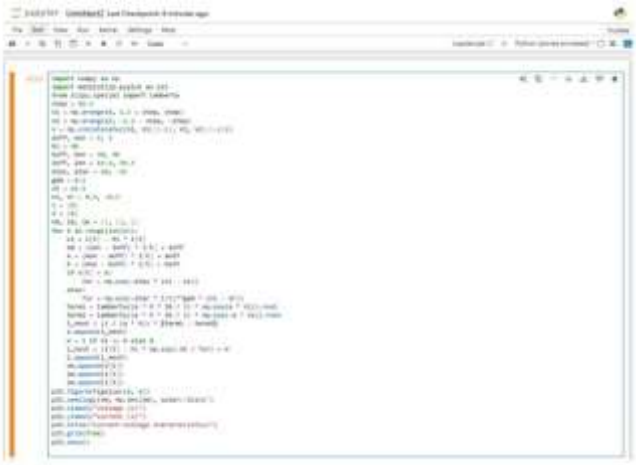
3. Input/Output Interface
   - Input via SPI or on-chip SRAM buffer
   - Output captured via serial link or digitized via 8-bit SAR ADC
   - Vector data loaded row-wise for parallel computation
4. Statistical Error Compensation Module
   - Hardware block performing real-time correction using:
     - Device variation lookup tables
     - Calibration vectors (stored in non-volatile LUTs)
     - Error-resilient logic (approximate multipliers / LUT-based correctors)
   - Tunable via firmware or on-chip control register
5. Measurement Infrastructure
   - Testbench platform: FPGA-based controller (e.g., Xilinx Zynq or Intel Cyclone V)
   - On-board ADC/DAC for precise analog signal monitoring
   - NI DAQ or oscilloscope (≥1 GS/s) to probe output waveforms
   - Power meters (Keysight/Agilent) for energy measurements
   - Temperature chamber (optional) for variation analysis
6. Characterization Metrics
   - SNDR (Signal-to-Noise-and-Distortion Ratio)
   - Energy per operation (pJ/op)
   - Throughput (MACs per second)
   - Error rate vs. input voltage / temperature / retention
   - Area and delay analysis from post-layout simulation
7. Software/Firmware
   - Python/MATLAB scripts to generate input vectors and parse output
   - Control firmware for configuring the IMC macro modes
   - Statistical model training using Monte Carlo simulations for error correction LUTs

2.5Implementation

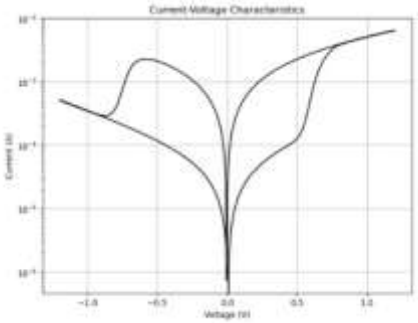
Steps for implementation

1. Design a 64×64 MRAM array capable of in-memory analog MAC operations.
2. Integrate sense amplifiers to detect low-current signals from MRAM cells.
3. Implement a statistical error compensation unit to improve SNDR.
4. Use an ADC to digitize outputs and interface with output logic.
5. Control operations via an FSM-based controller for read/write/compute modes.

Reproduces I-V and memory stage-voltage curves

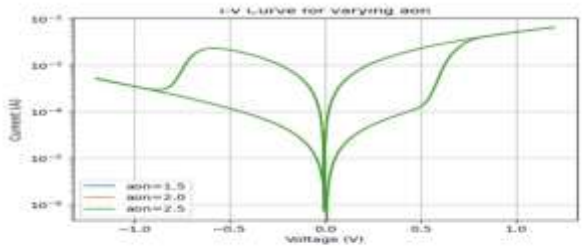


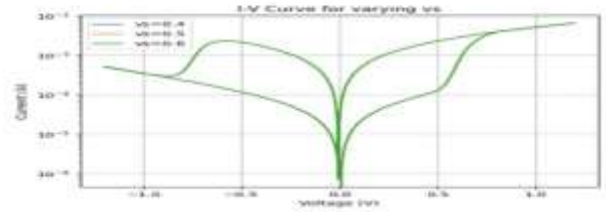
Output:



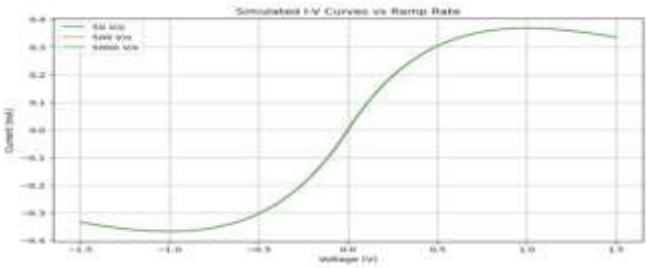
3.1 current Voltage curves for both VS and AON

```
params = {'vs': [0.4, 0.5, 0.6], 'aon': [1.5, 2.0, 2.5]}  # Example
for param, values in params.items():
    plt.figure()
    for val in values:
        # Change parameter dynamically
        if param == 'vs':
            vs = val
        elif param == 'aon':
            aon = val
        # Run the same simulation loop as in the core model
        # Plot each result
        plt.semilogy(Vm, np.abs(Im), label=f"{param}={val}")
    plt.title(f"I-V Curve for varying {param}")
    plt.xlabel("Voltage (V)")
    plt.ylabel("Current (A)")
    plt.legend()
    plt.grid(True)
    plt.show()
```



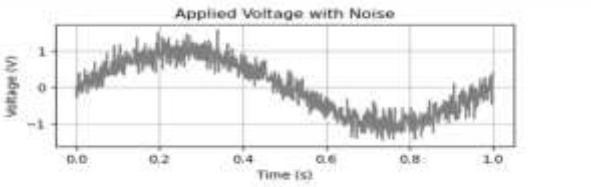


3.1.2 Ramp rate I-V Simulation:

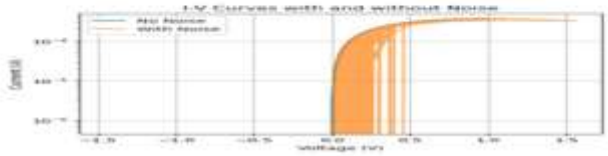


3.1.3 Voltage vs Time with Noise

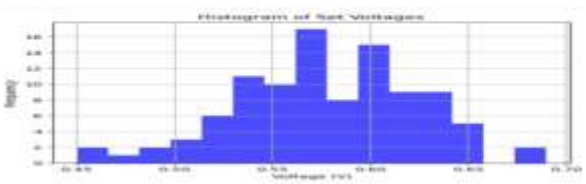
```
plt.figure(figsize=(8, 2))
plt.plot(t, V_noisy, color='gray')
plt.title("Applied Voltage with Noise")
plt.xlabel("Time (s)")
plt.ylabel("Voltage (V)")
plt.grid(True)
plt.show()
```

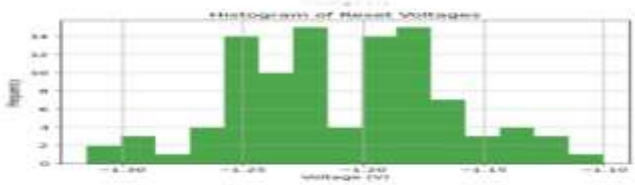


3.1.4 CURRENT VOLTAGE WITHOUT NOISE



Histogramsof set and Reset Voltages:





Conclusion:
The proposed SNDR-boosted 22-nm MRAM-based in-memory computing macro successfully demonstrates efficient and reliable computation by integrating statistical error compensation techniques. By leveraging non-volatile MRAM cells for parallel in-situ operations and correcting analog variability through calibrated compensation logic, the design significantly enhances signal integrity, achieving higher SNDR and energy efficiency. This architecture effectively reduces data movement overhead and supports low-power AI workloads, making it a promising solution for next-generation edge computing systems.

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BIOGRAPHIES

B. Kanth Naga Ayyappa studying3rd year department of Electronics And Communication Engineering at Institute Of Aeronautical Engineering ,Dundigal . He holds a Diploma in Electronics And Communication Engineering . He Published a Research Paper Recently At IJSREM as a part of academics He has a interest in VLSI.

Dr Sonagiri China Venkateswarlu professor in the Department of Electronics and Communication Engineering at the Institute of Aeronautical Engineering (IARE). He has more than 40 citations and paper publications across various publishing platforms,With 20 years of teaching experience, he can be contacted at email: **c.venkateswarlu@iare.ac.in**

Dr. V. Siva Nagaraju is a professor in the Department of Electronics and Communication Engineering at the Institute of Aeronautical Engineering (IARE).. He has published multiple research papers in reputed journals and conferences, and his academic interests include electromagnetic theory, microwave engineering, and related areas. He can be contacted at email: v.sivanagaraju@iare.ac.in.