International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 09 Issue: 12 | Dec - 2025 SJIF Rating: 8.586 ISSN: 2582-3930

Design and Analysis of a Wide Tuning Range Low Power Differential Ring Voltage-Controlled Oscillator in 90nm CMOS Technology

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Abstract
This work presents the design, analysis, and simulation of a four-stage differential ring voltage-controlled oscillator (VCO) aimed at achieving ultra-wide tuning range, low power consumption, and compact silicon area in 90nm CMOS technology. The proposed VCO employs a novel multipath delay cell incorporating primary and secondary delay loops, enabling flexible frequency control across multiple decades. Dual control voltages (Vctr1 and Vctr2) are used to independently regulate low- and high-frequency operation, while a low-threshold NMOS device enhances tuning sensitivity at low frequencies. Pre-layout simulations conducted using Cadence Spectre demonstrate an exceptional tuning range from 1 MHz to 13.8 GHz (99.99%), with power consumption varying from 29.3 µW to 1.715 mW. The design achieves acceptable phase noise of −82.3 dBc/Hz at 1 MHz offset and occupies only 102.457 µm² of silicon area. Comparative analysis confirms that the proposed VCO surpasses most existing designs in tuning range, power efficiency, and integration suitability. This work establishes an effective methodology for developing wideband, low-power oscillators for modern mixed-signal and communication systems.

Index Terms
Differential ring VCO, dual delay loop, low-power oscillator, dual control voltage, CMOS VCO.

I. Introduction

Voltage-controlled oscillators (VCOs) are key building blocks of phase-locked loops (PLLs), frequency synthesizers, and RF transceivers. With the rapid development of wireless systems such as 5G/6G, IoT, and UWB, modern oscillators must support extremely wide tuning ranges while operating under strict power and area constraints. LC-based VCOs provide excellent phase noise but suffer from limited tuning range and large chip area due to on-chip inductors. Ring-based VCOs overcome these limitations by offering wide tuning range, compact area, and high integration capability. However, conventional ring VCOs exhibit degraded phase noise, limited linearity, and restricted frequency stability. Differential ring oscillators (DROs) improve noise immunity and support even-stage oscillation and multi-phase outputs. However, achieving multi-decade tuning with low power and stable PVT behavior remains a major challenge. This work addresses these issues by introducing a dual-path differential ring VCO with dual control voltages and low-VT devices**.**

II. Related Work

Several tuning techniques for ring VCOs have been reported, including current-starved delay cells, cross-coupled loads, injection-locked architectures, and programmable resistive networks. Current-controlled VCOs provide wide tuning but degrade phase noise due to current mirror noise. Multipath ring oscillators extend frequency range but increase circuit complexity and power consumption.

Most reported DROs achieve tuning in the order of a few hundred MHz to several GHz. However, very few designs demonstrate continuous tuning from MHz to multi-GHz without switched capacitors or digital calibration. The proposed design achieves this using a purely analog dual-path tuning mechanism.

III. Proposed VCO Architecture

3.1. Four-Stage Differential Ring Structure

The proposed VCO consists of four differential delay stages connected in a ring configuration. The differential topology provides:

- High common-mode noise rejection
- Even-stage oscillation
- Quadrature phase outputs
- Improved supply noise immunity

Each stage receives two differential inputs corresponding to the primary and secondary delay paths.

3.2. Dual-Delay Loop Mechanism

Two propagation paths are implemented inside each delay cell:

- **Primary delay path:** Provides large delay and controls low-frequency operation.
- **Secondary delay path:** Provides small delay and dominates during high-frequency operation.

The secondary input is phase-advanced by 45°, which accelerates signal transitions and increases oscillation frequency at GHz ranges.

3.3. Proposed Differential Delay Cell

The delay cell consists of:

- NMOS differential input pair (M1, M2)
- PMOS differential input pair (M3, M4)
- Cross-coupled PMOS load (M5, M6)
- PMOS control pair (M7, M8)
- Low-threshold NMOS control transistor (M9)

The low-VT NMOS transistor significantly enhances low-frequency tuning without requiring excessive bias voltage.

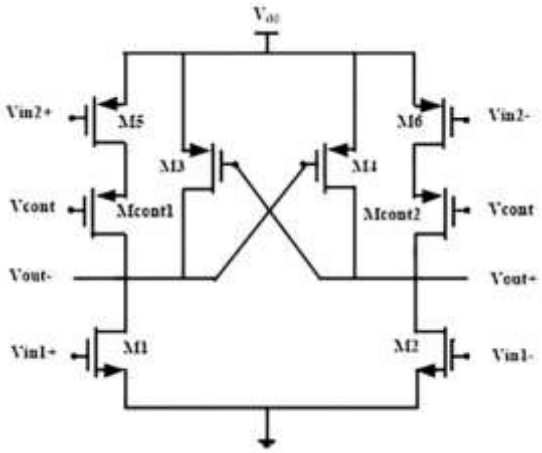

Figure. 1. The delay cell of the voltage-controlled oscillator (VCO)

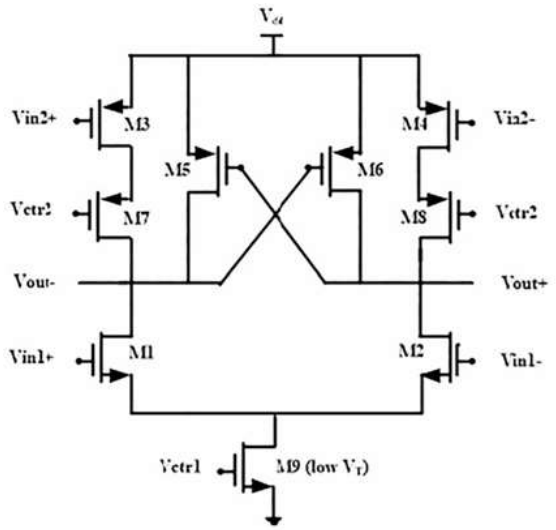

Figure. 2. Proposed delay cell

IV. Dual-Control Voltage Tuning

4.1. Control Voltage Vctr1 (Low-Frequency Control)

Vctr1 controls the conduction of the low-VT NMOS (M9).

- Low Vctr1 → weak conduction → slow transitions → low frequency
- High Vctr1 → strong conduction → fast transitions → high frequency

This control dominates operation from **1 MHz to ~5 GHz**.

4.2. Control Voltage Vctr2 (High-Frequency Control)

Vctr2 drives PMOS control transistors (M7, M8).

- Lower Vctr2 increases secondary-path contribution.
- Effective delay decreases → oscillation frequency increases.

This control dominates the **5 GHz to 13.8 GHz** range.

The dual-control strategy eliminates tuning dead zones and provides smooth frequency transition across multiple decades.

V. Delay and Frequency Analysis

The oscillation frequency of an N-stage differential ring oscillator is:

$$f_{osc} = \frac{1}{2Nt_d}$$

where N = 4 and td is the delay of a single stage.

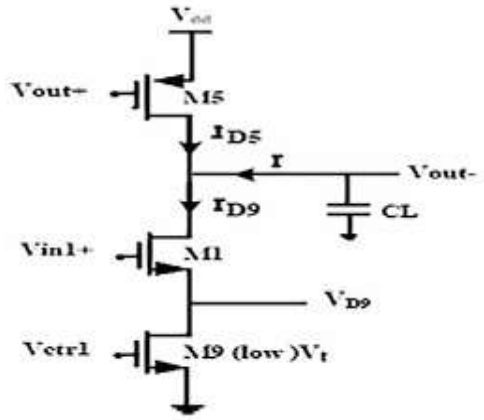

Figure.3 Half-circuit of the proposed delay cell in low-frequency mode

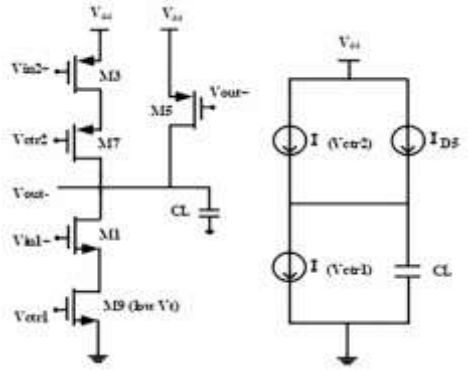

Figure. 4 Hal-circuit of the proposed delay cell in high-frequency mode

The proposed architecture operates in three regions during a low-to-high output transition. These regions arise from the combined operation of NMOS and PMOS devices, especially M1 (input NMOS), M5 (PMOS load), and M9 (low-VT control NMOS).

The delay cell operates in three regions:

PMOS-dominant region: Initial slow transition, independent of Vctr1

PMOS–NMOS transition region: Delay strongly dependent on Vctr1

NMOS-dominant region: Maximum sensitivity to Vctr1, enabling low-frequency oscillation

High-frequency operation is achieved by strengthening the secondary delay path using Vctr2, which minimizes effective stage delay and increases oscillation frequency.

VI. Results and Discussion

The proposed VCO achieves a tuning range from 1 MHz to 13.8 GHz, low power consumption, compact area, and acceptable phase noise.

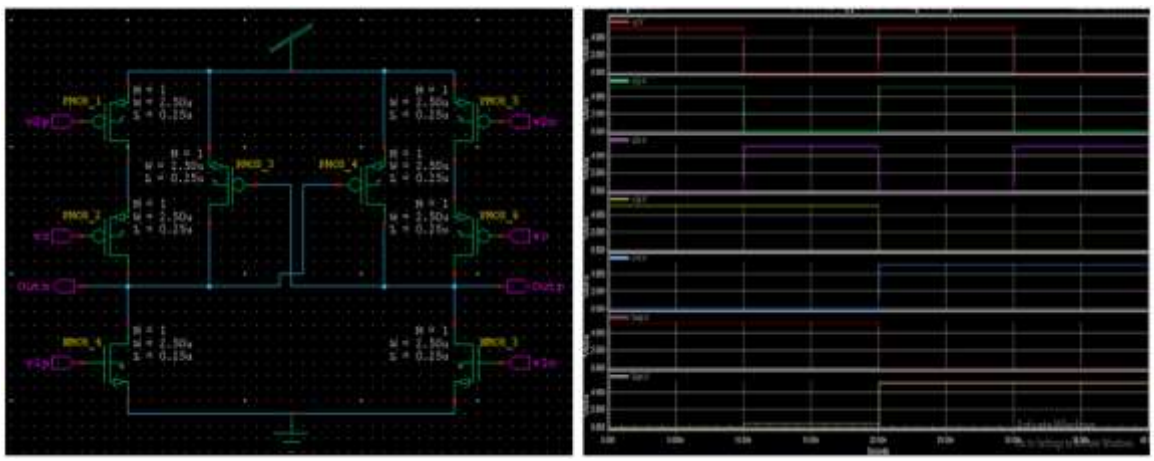

Figure. 5. Schematic design and Output waveform of the delay cell of the Voltage-Controlled Oscillator (VCO)

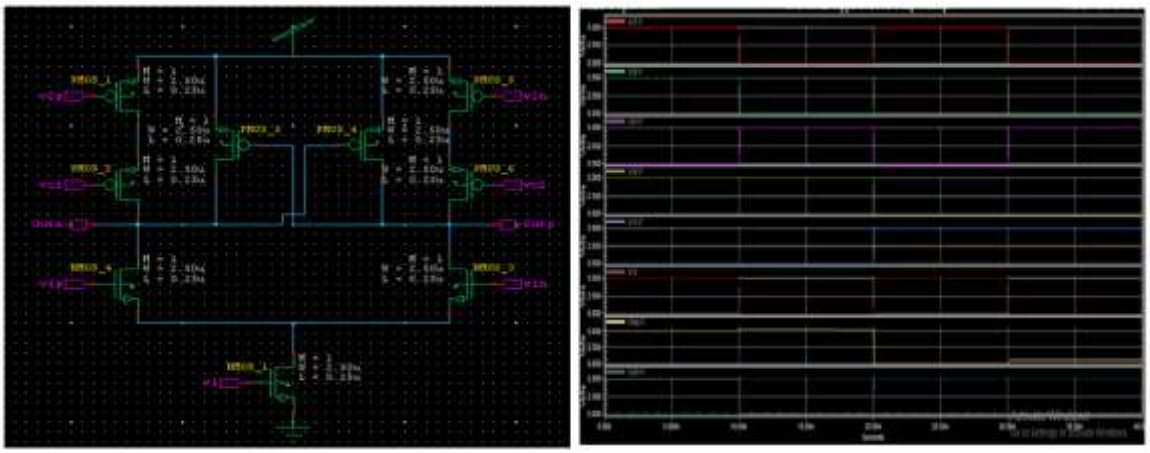

Figure. 6. Schematic Diagram and output waveform Proposed delay cell

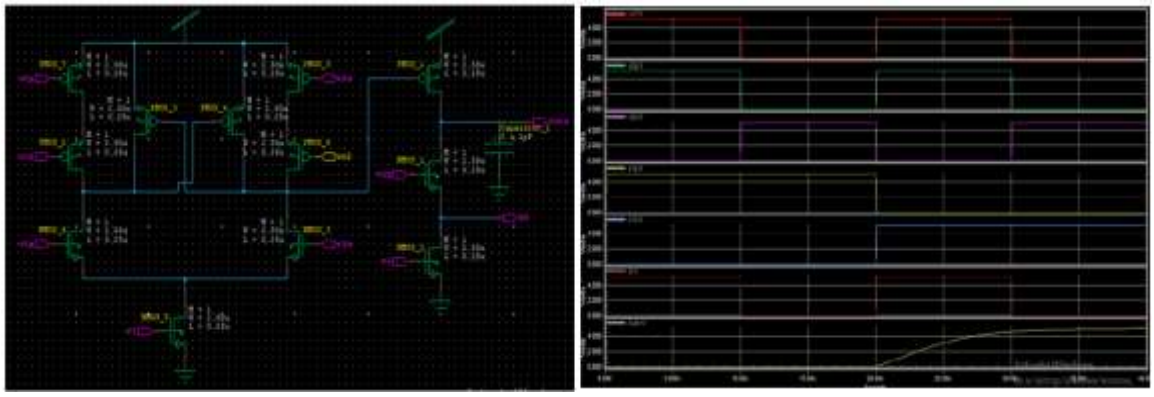

Figure. 7. Schematic Diagram and output waveform the proposed delay cell in Low frequency mode

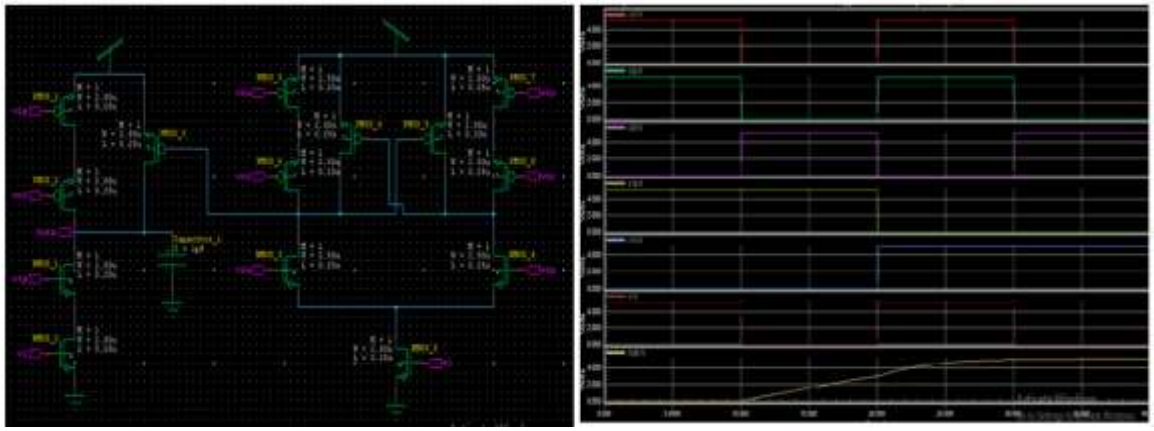

Figure. 8. Schematic Diagram and output waveform the proposed delay cell in High frequency mode

VII. Conclusion

A four-stage dual-path differential ring VCO with dual control voltages has been presented. By integrating primary and secondary delay paths with a low-threshold control NMOS, an ultra-wide tuning range of **1 MHz to 13.8 GHz** with low power consumption and compact area has been achieved. Simulation results validate the effectiveness of the proposed architecture for PLL and RF communication systems.

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