# Design and Analysis of Low Noise Amplifier Using Source Inductor Degenerative Topology

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**Abstract** - The design and analysis of a low-noise amplifier (LNA) with improved performance through source inductor degeneration is presented in this study. Modern communication systems require power efficiency, which is why the suggested LNA seeks to optimize gain and minimize noise figure (NF) while preserving power efficiency. A source inductor degeneration technique improves the amplifier's input impedance, which lowers noise and improves linearity. With findings indicating a low noise figure and high gain, the design shows a notable improvement in overall linearity and noise performance. This LNA offers excellent efficiency, stability, and robust performance in settings with strict noise requirements, making it appropriate for use in RF front-end systems. Performance measurements and simulation results confirm that the suggested design is successful.

***Key Words*** **: Gain, Low Noise Amplifier (LNA), Noise Figure (NF)**

## 1.INTRODUCTION *( Size 11, Times New roman)*

The Low Noise Amplifier (LNA) is arguably one of the receiver circuit's most important requirements.The LNA, which is positioned at the front end, must greatly boost the weak input signals, which normally range from -140 to 40 dBm (0.03µV to 3 mV). Signal strength is further reduced by physical obstacles that result in multi-path and fading, necessitating an LNA that reduces distortion and noise. Because the LNA's performance is closely linked to the receiver circuit's overall operation, designing it is a challenging endeavor that requires balancing trade-offs between clamor figure (NF), gain, linearity, and impedance coordination.

## 2. METHODOLOGY

### 2.1 Source Inductor Degenerative LNA

The source degeneration LNA is a sort of LNA that uses an inductor in the source the input transistor to improve its input matching and noise figure. The commonly used topology for LNA design, particularly in narrow band applications because of its advantages as far as minimal noise level, maximum gain, as well as minimal power consumption.

**Here's how it works:**

I. The inductor (L) in the source of the of the semiconductor (transistor) (M1) LNA, which reduces the figure of noise.

II. Capacitor (C) in parallel with the inductor forms a resonant circuit that helps to enhance the the input matching of the LNA.

III. The input signal an application of signal to the transistor's gate and the sign result is taken from the Channel of the transistor.

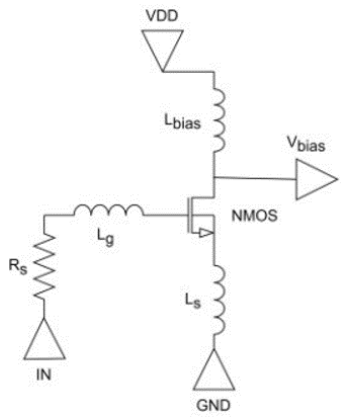



**Figure 1:** Source Inductor Degenerate LNA Circuit.

This section explains the process of creating schematics for the source inductor degenerate LNA utilizing the cadence Virtuoso Platform. The Rhythm Virtuoso Stage is a flexible tool-set for designing full-custom integrated circuits, offering features such as schematic passage,, behavioral displaying, circuit reenactment, and physical layout. For this work, the 180 nm conventional interaction configuration unit (GPDK) is utilized

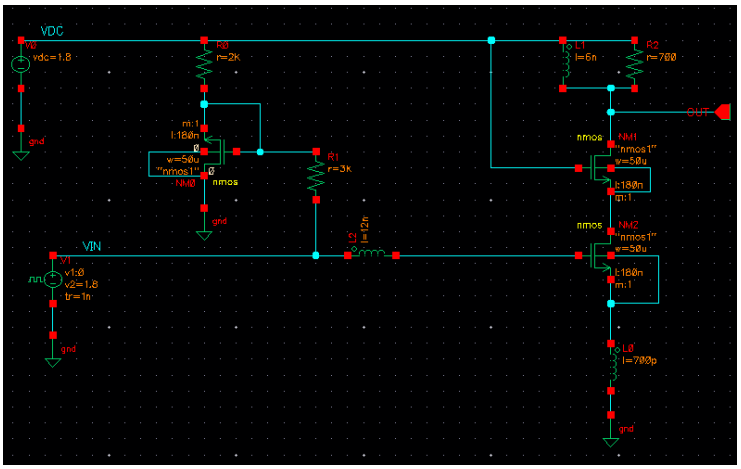


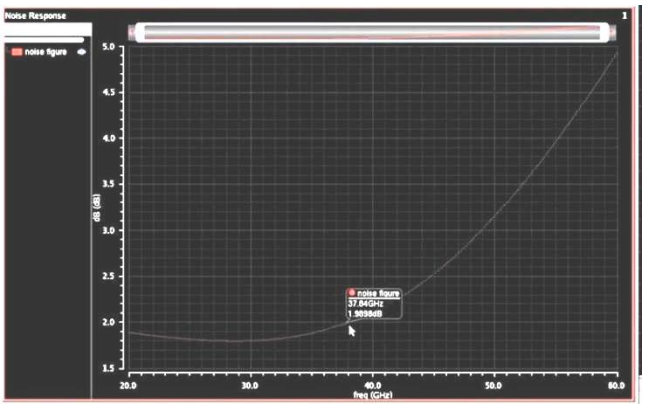

**Figure 2:** Source Inductor Degenerate LNA Circuit designed in Cacdence

The begin with the source inductor degenerate LNA. The schematic is first evolved utilizing the Cadence Virtuoso Plat- form, as illustrated in Figure 2. This schematic consolidates a cascode and an current mirror, addressed by NM1 and NM bias, individually. The cascode's purpose is to enhance input-yield detachment and minimize reverse transmission, effectively eliminating the Miller effect by preventing direct coupling from the result.

The degeneration inductor, Ls, is selected to be 700 pH, according to the maximum size allowed by the 180 nm GPDK process technology. Next, We take into account the resistor-inductor circuit (RL circuit), moreover known as an RL filter or network. This circuit, utilized related to the supply voltage (VDC), allows the inductor to pass the DC bias current while blocking RF signals from returning to the power supply . In Figure 2, the R and L values are decided to be 700 Ohms and 6 nH, respectively. At last, three pins, labeled VDC, IN, and OUT, are placed in the schematic. These pins, or ports, are utilized to make the symbol,empowering the LNA to interact with more significant level circuit parts.

## CONCLUSION

This part presents the outcomes of the reproductions that were done utilizing the Cadence Virtuoso Platform. To demonstrate that the LNA meets performance requirements.




### *Commotion Figure*

The Commotion figure (NF) is a crucial boundary that measures the amount of commotion the LNA adds to the info signal. It is fundamental for the LNA to have a minimal noise figure since, as the principal block in the framework, it has the most significant influence on the general framework's commotion factor, according to the FRIIS Condition. The LNA's NF min and Noise Figure at 2.4 GHz are 0.388 dB and 0.505 dB, separately. These outcomes show that the planned LNA presents an exceptionally small amount of clamor (noise) to the transmitted signal.

Amplifiers, as electronic devices, enhance the power of a signal by amplifying its amplitude through an external power supply. This work aims to explore various LNA topologies, with a specific focus on narrow-band LNAs. Initially, detailed explanations of two LNA designs, namely the source inductor degenerate LNA and the differential LNA, are provided using small signal transistor models. Subsequently, the schematics for these LNAs are constructed on the Cadence Virtuoso Plat- form, followed by simulation and analysis using a test bench. Finally, the obtained results are scrutinized, and a comparative analysis between the two LNAs is conducted.

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