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Design and Analysis of Negative Capacitance FET based 6T SRAM Cell for Next generation low-power Applications

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***Abstract*— Power optimization has become increasingly critical in the VLSI industry due to the rising density of memory systems, which leads to higher power consumption. Static RAM (SRAM) cells are particularly affected by this issue. A significant contributor to power consumption is the leakage current in transistors. Therefore, decreasing power consumption in each memory cell is essential. This paper focuses on optimizing the power of various 6T SRAM cells by employing advanced techniques like power gating, reverse biasing, and transistor stacking in the context of Negative Capacitance Field-Effect Transistors (NCFETs).**

Keywords—SRAM, NCFET, power consumption, power gating, Delay, Transistor Stacking

I. INTRODUCTION

In IOT, SRAM plays a crucial role in enabling fast and efficient data processing, storage, and communication. For example, Smart home devices are electronic devices that can be controlled, monitored, and automated remotely using a smartphone, tablet, or computer. They are designed to make homes more convenient, energy-efficient, and secure. SRAM is used in smart home devices such as thermostats and security cameras to store and process data related to home automation, security, temperature, Humidity, and motion.

Nowadays, the design of semiconductor devices has advanced significantly with the development of Negative Capacitance Field-Effect Transistors (NCFETs), especially as the market shifts to transistors that are more compact and power-efficient. As device dimensions decrease to nanometer scales, conventional planar transistors encounter difficulties in managing leakage currents and short-channel effects [1]. Due to these challenges, NCFETs, which offer enhanced performance, lower power consumption, and improved control over subthreshold swing, have been developed and adopted [2]. NCFETs leverage ferroelectric materials to reduce the subthreshold swing below 60 mV/decade, mitigating leakage and enhancing overall efficiency, making them a promising solution for advanced nanoscale devices.

By integrating ferroelectric materials into the gate stack, NCFET, an advanced kind of transistor, incorporates a negative capacitance effect. By lowering the subthreshold swing below 60 mV/decade, NCFETs improve electrostatic control over the channel, unlike traditional planar transistors, which suffer from inadequate gate control at nanoscale sizes [3].

By integrating ferroelectric materials into the gate stack, NCFET, an advanced kind of transistor, incorporates a negative capacitance effect. By lowering the subthreshold swing below 60 mV/decade, NCFETs improve electrostatic control over the channel, unlike traditional planar transistors, which suffer from inadequate gate control at nanoscale sizes [3]. Leakage currents are greatly decreased by this enhanced gate control, which also raises the device's overall energy efficiency. Furthermore, short-channel effects—a significant worry in conventional transistors at smaller nodes—are lessened by the special negative capacitance effect [4]. Because of this, NCFETs provide next-generation semiconductor applications with enhanced performance, power efficiency, and scalability.

The lowering of subthreshold swing below the 60 mV/decade limit is one of the key characteristics of NCFET technology, which allows it to function at lower supply voltages while retaining great performance. Because of this feature, NCFETs are particularly appealing for power-critical applications such as mobile devices, high-performance computing, and data centers. Without sacrificing speed, NCFETs offer notable power savings by reducing leakage currents and lowering the threshold voltage.

While NCFETs help address heat dissipation problems in closely packed integrated circuits, their lower power consumption in portable devices directly correlates to longer battery life. This improved thermal efficiency makes higher integration densities possible, aiding in the creation of semiconductor devices that are incredibly small and energy-efficient. NCFETs are a viable option for upcoming low-power, high-performance computer systems because of their capacity to reduce short-channel effects, which also improves their scalability for advanced technology nodes [5].

NCFETs offer enhanced switching speeds, reduced power consumption, and improved device variability, making them a promising technology for scaling to advanced technology nodes such as 2nm and beyond [6].

By leveraging the negative capacitance effect in the gate dielectric, NCFETs achieve a lower subthreshold swing, allowing faster transitions between on and off states with reduced energy losses. Due to their ability to maintain reliable performance at ultra-scaled dimensions, NCFETs are increasingly viewed as a key enabler for next-at smaller technology nodes.

generation CPUs, memory components, and other high-

performance computing systems [7]. Their reduced leakage currents and superior electrostatic gate control minimize the impact of short-channel effects, which are critical challengesNCFETs are anticipated to be essential in promoting additional electronic device miniaturization, power efficiency, and performance improvements as the semiconductor industry gets closer to the physical bounds of Moore's Law. NCFETs are positioned as a key technology for the future of nanoscale semiconductor design due to their scalability and capacity to balance speed, power, and thermal efficiency [8].

NCFET technology overcomes the drawbacks of traditional planar transistors by offering better control over leakage currents and reducing short-channel effects, leading to notable gains in performance and power efficiency. By incorporating ferroelectric materials into the gate stack, NCFETs can enable faster switching and reduced power consumption by lowering the subthreshold swing below the conventional 60 mV/decade limit.

NCFETs have the potential to become a key component of contemporary semiconductor design as semiconductor technology advances, spurring innovation in a variety of fields, including high-performance computer systems and energy-efficient mobile devices [9]. NCFETs are positioned as a crucial technology for upcoming generations of nanoscale electronics because of their scalability, improved gate control, and power-saving characteristics, which will allow for further improvements in device miniaturization, performance, and efficiency.

II. LITERATURE SURVEY

In this study [9], the power optimization analysis of different SRAM cells using NC-FETs was well discussed. The paper covers the basic conventional SRAM structure and the working principles of an SRAM cell. Instead of the transistor stacking technique, NCFETs are utilized to achieve power reduction through improved electrostatics and lower subthreshold swings. The analysis includes power consumption calculations of various SRAM cells implemented with NC-FETs at different supply voltages. The power calculations are performed without the stacking method, demonstrating the advantages of NC-FETs in reducing power dissipation while maintaining stable SRAM operation
.
The NCFET technology-based low-power SRAM cell design for embedded memory was discussed well [10].The advantages of using NCFET technology compared to CMOSTechnology also discusses how leakage current will increase the power consumption of any circuit. Why we want to move to NCFET technology. It also discusses the power consumption of the SRAM cell 6T circuit in NCFET technology.

In [11], low-power and high-efficiency NC-FET designs for SRAM cell were introduced, showcasing advancements in memory technology. SRAM cells with 6T and 7T architectures are widely used but struggle with power consumption and noise at smaller nodes. NCFETs, with improved electrostatics and negative capacitance effects, offer better gate control, reduced leakage, and enhanced noise immunity. Studies show NCFET SRAM exhibits lower power dissipation, improved stability, and resilience to variations, making it ideal for next-generation low-power devices.

The design and development of efficient SRAM cells using NC-FETs for low-power memory applications are introduced [12], emphasizing significant power reduction while maintaining performance. NCFET-based SRAM designs are favored for their ability to enhance gate control, reduce leakage power, and mitigate short-channel effects using negative capacitance. Researchers focus on optimizing SRAM architectures, such as 6T, 7T, and multi-transistor configurations, leveraging NC-FETs to achieve a balance between power efficiency, stability, and performance in advanced technology nodes.

In [13], the design of a 12T SRAM cell with improved read and write performance using NCFET technology is proposed. The 12-transistor SRAM cell is crucial in high-performance memory systems where speed and power efficiency are essential. Conventional 6T and 8T SRAM designs struggle with leakage power and stability at smaller nodes. NCFETs, with negative capacitance effects, enhance gate control, reduce leakage, and improve read/write operations. Recent research focuses on optimizing bit-line and word-line architectures to minimize delays while ensuring data integrity and low power consumption.

The design of a 45nm NCFET-Based Compute-in-SRAM for Energy-Efficient Machine Learning Applications explores advancements in hardware accelerators for ML, highlighting the need for efficient solutions beyond traditional GPUs. It introduces Compute-in-Memory (CIM) architecture to reduce memory access delays and power consumption. NCFETs, with low threshold voltage and high sub-threshold slope, enhance energy efficiency, achieving a 3X reduction in energy and 18X speed improvement over CMOS. NCFETs also mitigate leakage issues, maintaining performance at lower voltages.

The paper explores advanced SRAM design techniques for leakage reduction and stability enhancement. Techniques such as forward/reverse body biasing, Multi-Threshold CMOS (MTCMOS), and fingering transistors effectively control leakage. Stability is improved through transistor width modulation, voltage scaling, and charge pump circuits, though trade-offs in area and leakage exist. Innovations like 7T and 8T SRAM cells enhance read stability and energy efficiency but introduce area overhead.
Simulations using Cadence Virtuoso on UMC 55nm technology validate these optimizations, ensuring a balance between power efficiency, stability, and performance in modern SRAM architectures.

From the above literature survey, we can conclude that NC-FET technology offers lower leakage power compared to other technologies while delivering enhanced performance. Due to the negative capacitance effect, NC-FETs provide better electrostatic control, reducing power consumption and improving energy efficiency. As the number of transistors increases in SRAM, read and write stability improves, and overall power dissipation decreases. NC-FET-based SRAM designs demonstrate superior

reliability, making them a promising choice for next-generation low-power memory applications.

III. METHODOLOGY

TRANSISTOR STACKING TECHNIQUE

Consider a CMOS inverter, as shown in the figure below. Depending on the input condition, the PMOS or NMOS transistor will be turned off, allowing the other to conduct. Under steady-state operation, the current flowing through the circuit is ideally either zero or very minimal. However, when one of the transistors is in the off state, leakage currents—such as subthreshold leakage, gate leakage, and junction leakage—can still flow through the transistor. These leakage currents, though small, contribute to static power dissipation and become more significant as technology scales down. As a result, leakage current plays a critical role in increasing the overall power consumption of the circuit, particularly in low-power and high-density designs.

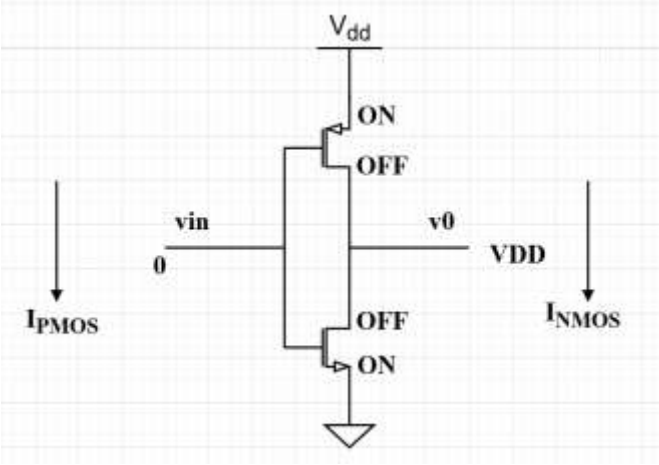

Fig 1: CMOS Inverter

The power absorbed from V_{DD}
Power From $V_{DD} = V_{DD} X I_{NMOS}$ or $V_{DD} X I_{PMOS}$ ----------(1)
Average Power = $V_{DD} X (I_{NMOS}+I_{PMOS})/2$ ----------(2)
$I_{NMOS} = (W/L) I_0 e^{(Vgs - Vth/n_{\phi t})}(1-e^{-Vds/_{\phi t}})$ ----------(3)

In Figure 2, the transistors off condition current is shown as *I′*, and in Figure 3, the transistors N1 and N2 have off condition currents of *I*1 and *I*2, respectively. The two-inverter stack's current must be equal for

I1 = I2 ----------(4)

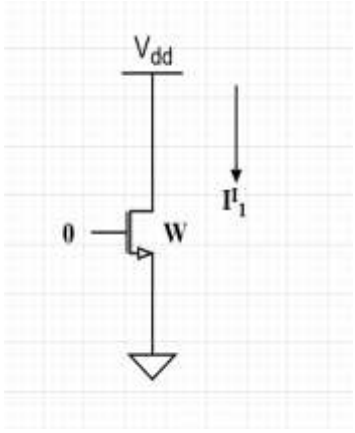

Fig 2: NMOS Transistor

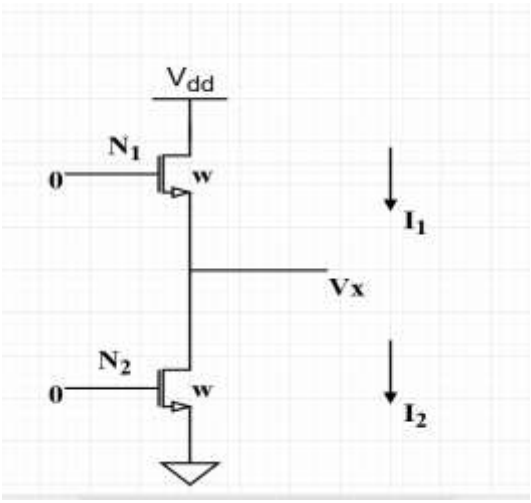

Fig 3: Inverter

Table 1: Vgs and Vds

	VGS	VDS
N1	$-V_X$	$V_{DD}-V_X$
N2	0	V_X

By substituting above values in eq(3),we get

$$I_1 = \left(\frac{W}{L}\right) I_0 e^{\left(\frac{-V_X - V_{Tn}}{\phi_t}\right)} \text{ ----------(5)}$$

$$I_2 = \left(\frac{W}{L}\right) I_0 e^{\left(\frac{-V_{Tn}}{\phi_t}\right)} \left(1 - e^{-\frac{V_x}{\phi_t}}\right) \quad \text{----------(6)}$$

By substituting I_1 and I_2 in eq(4), we get

$$I_1 = 1/2 \left(\frac{W}{L}\right) I_0 e^{\left(\frac{-V_{Tn}}{\phi_t}\right)} \quad \text{----------(7)}$$

$$I_1' = \left(\frac{W}{L}\right) I_0 e^{\left(\frac{-V_{Tn}}{\phi_t}\right)} \quad \text{----------(8)}$$

We can conclude from the above equations that the current flowing through a single transistor is half the current flowing through two transistors, so the leakage current flow through the transistors is reduced. However, instead of using two transistors, we can use a single transistor with half the width and get the same leakage current. Using two transistors increases delay and area.

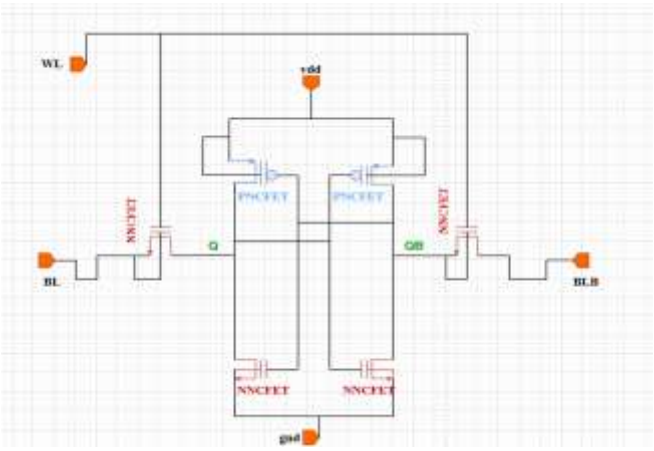

Fig 4: Conventional 6T NCFET SRAM Cell

In figure 5, we use two sleep transistors, which will act like a stack, and figure 4 diagrams represent conventional 6T SRAM circuit and figure 5 represents 6T SRAM with stacking technique.

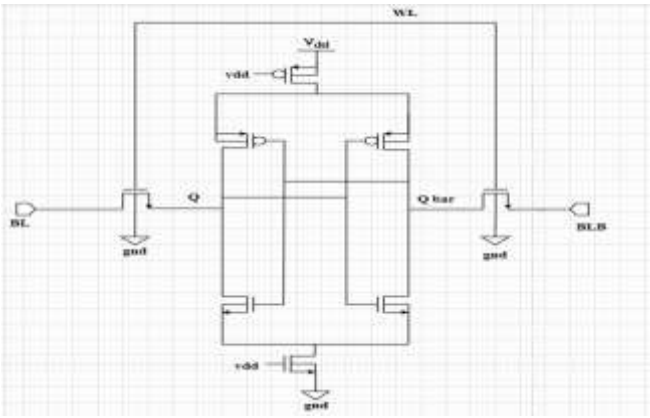

Fig 5: Proposed NCFET SRAM cell with Stacking effect

IV. RESULTS

The schematic, which is shown in figure 4 and figure 5, is implemented in cadence software. The circuit of 6T SRAM is implemented, and the output waveforms, read and write waveforms, and power are calculated we are getting 77.66nW. The transistor stacking technique is also implemented, and we are getting power as 212.68pW. Figure 6 explains the characteristics obtained in the transient analysis of 6T SRAM cell, and figure 7 and figure 8 explain the read and write operations.

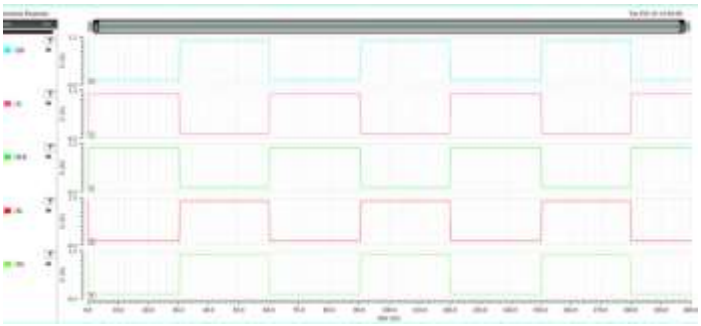

Fig 6: Transient Analysis of SRAM cell

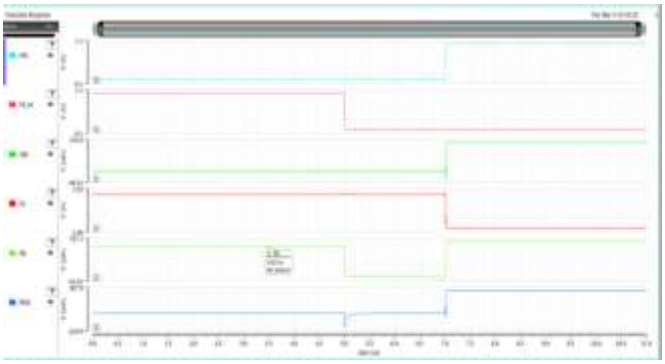

Fig 7: Demonstration of Read operation

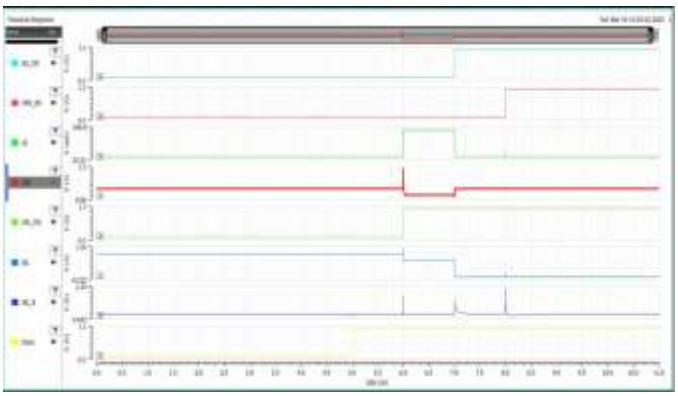

Fig 8: Demonstration of write operation

Table 2: Power consumption comparison of 6T SRAM

NCFET SRAM	Power consumption	Delay
Conventional SRAM	77.66nW	12.4ps
SRAM with Stacking effect	212.68pW	182ps

V.CONCLUSION

In this work, we proposed SRAM with better stability and less power consumption performed with 6 transistors in NCFET technology. In NCFET-based low-power 6T SRAM cell designs, the goal is to address key challenges associated with conventional planar CMOS technology, particularly in power consumption and leakage currents. By utilizing the NCFET technology, which offers superior control over short-channel effects and reduced leakage currents, this 6T SRAM cell achieves lower static and dynamic power consumption, making it ideal for low-power applications, such as portable electronics and high-density memory arrays. Additionally, the use of 6 transistors improves read and write stability, particularly in ultra-scaled devices where conventional SRAM cells face challenges related to process variations and device mismatch. The enhanced stability ensures reliable data retention, especially at lower supply voltages, further contributing to energy savings. The proposed 6T NCFET SRAM has a decrease in power consumption compared to conventional 6T NCFET SRAM. Overall, the NCFET-based 6T SRAM cell stands out as a promising solution for modern low-power, high-performance VLSI systems.

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