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Design and Analysis of Performance Parameters of a 3-bit Universal Shift Register

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Abstract **- Sequential circuits usually contain both combinational logic circuits and memory elements to store the data. The basic memory elements are flip-flops and registers. The three kinds of register operations namely parallel loading, bidirectional and unidirectional are performed by a universal shift register (USR). Select lines decide the mode in which the USR operates. The cadence tool is used to design and analyse the USR. Gpdk180 technology file is used. It is also implemented, simulated, and synthesized using Xilinx ISE 14.7 and the RTL schematic is obtained. The objective of this paper is to analyse USR concerning its power and delay performance parameters and use it accordingly in higher complex VLSI systems.**

Key words **-** ***Universal shift register, cadence 180nm technology, performance parameters.***

I. INTRODUCTION

Digital circuits are categorized into combinational and sequential circuits considering the output and elements used in them. Logic gates and other elements constructed by these gates are used in combinational circuits whereas Memory elements are used in sequential circuits such as Flip-flops and latches. Flip-flops are mainly used in almost all the VLSI circuits because they can be controlled by clock or signal transitions rather than signal or clock level.

Registers are constructed by cascading Flip-flops so that the ability to store bits increase. The data or the binary bits which are being stored shall be moved within the system or out of the system and those are called shift registers. There are basically four types of shift registers namely parallel in parallel out, parallel in serial out, serial in serial out and serial in parallel out. These are unidirectional registers. Universal shift register performs all of these together along with left shit that is bidirectional operation. The universal shift register is employed in four modes:

- Lock mode
- Right shift
- Left shift
- Parallel load

The universal shift register incorporates a 4:1 multiplexer and D flip flops. The 4:1 Mux is used to select among the modes in which USR operates For an n-bit Universal shift registers, n-4:1 multiplexers and n-D flip flops are used.2 select lines are used to select the modes. Active low reset is used. LSB_in is used for the left shift operation and MSB_in is used for right shift operation.

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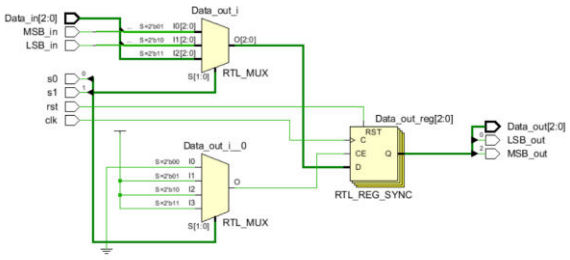

Fig. 1 Schematic Diagram of USR.

II. UNIVERSAL SHIFT REGISTER COMPONENTS

A. D Flip-flop

D Flip-flops are the sequential circuit that is transparent. When the clock's active edge arrives, input is propagated to output. Else output retains its previous value. D flip-flop can be constructed from an SR flip-flop and an inverter. The D flip-flop in this design contains both PRESET and clear which are active low

TABLE I
TRUTH TABLE FOR D FLIP-FLOP

PRESET'	CLEAR'	CLOCK	D	Q	Q'
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	X	X
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	0	X	Q_0	Q_0'

B. 4:1 Multiplexer

This is a combinational circuit that is used to select among the 2n given inputs using n select lines. In this design 4:1 Multiplexer is used to select among 4 modes using two select lines. If S0 is 0 and S1 is 0, then it selects I0 input due to which USR operates in the locked state. If S0 is 1 and S1 is 0, USR operates in right shift mode. If S0 is 0 and S1 is 1, USR

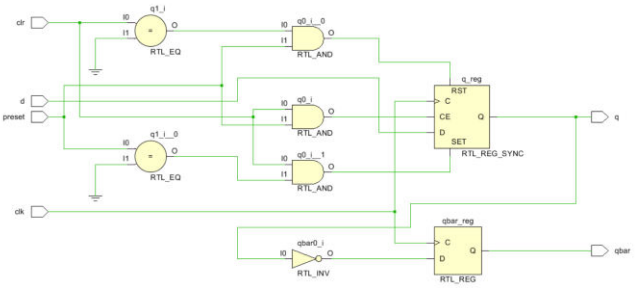

Fig. 2 Schematic Diagram of DFF

Operates in left shift mode and if S0 is 1 and S1 is 1, USR operates in parallel load mode. The circuits have been designed using CMOS technology considering its high noise immunity and low static power dissipation

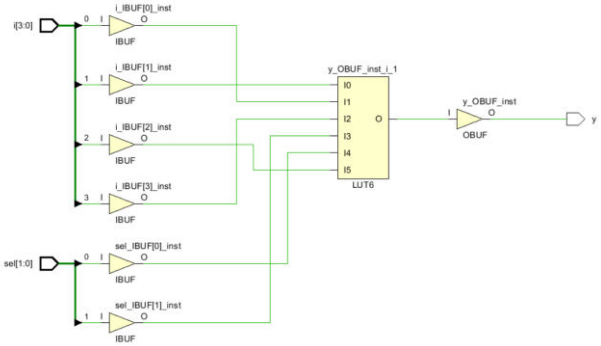

Fig. 3 Schematic Diagram of 4:1 MUX

TABLE II
TRUTH TABLE FOR MUX

S1	S0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

III. RESULTS AND SIMULATIONS

A 3-bit Universal Shift Register is designed in Cadence Virtuoso tool along with the 4 channel multiplexer and the D flip-flop. The schematics of these are created in 180nm technology. The sizing of transistor is done considering the width of PMOS as 2.5 times the width of NMOS.

The VDD that is the power supply for the entire design is given 1.8v.The simulation outputs of 4:1 mux and D flip-flop with and without delay is given.

Figure 4 shows that the output Q of the flip-flop follows the input signal D only at the positive transition of the clock. When preset is made low, then the output Q changes to high irrespective of the clock and the D input. When clear is made low, output Q will become low irrespective of the D input and clock. When both these control inputs are high, then the output follows D input considering the clock's active edge.

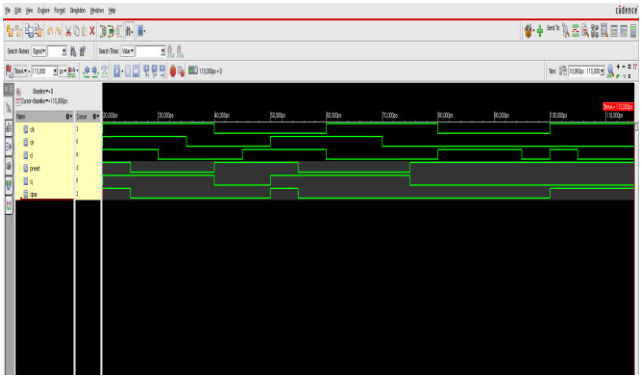

Fig. 4 Simulation waveform of DFF

Figure 5 shows that the multiplexer output carries I0 input when both the select lines are made logic 0, carries I1 when s1 is made 0 and S0 is made 1, carries I2 when S1 is made 1 and S0 is made 0 and carries I3 when both S0 and S1 are made 1.

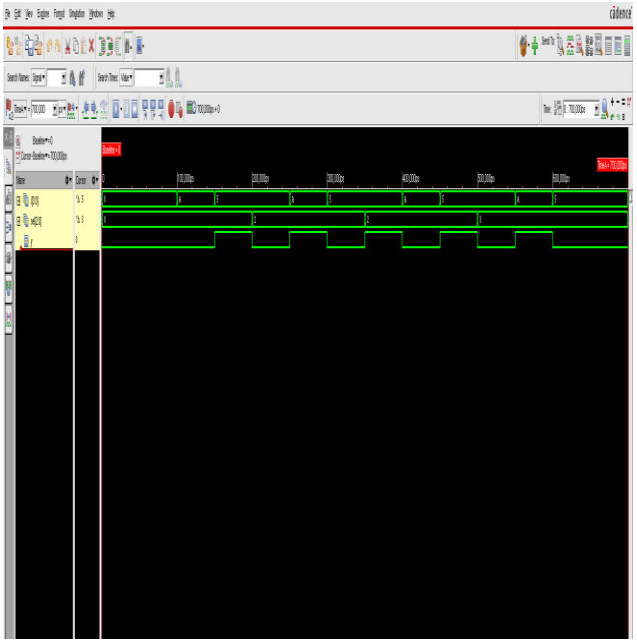

Fig. 5 Simulation waveform of 4:1 MUX

The power consumed because of some reverse biased diodes or during the subthreshold conduction is basically the leakage power. And it will usually be very less compared to dynamic power which is basically the power dissipated when the switching action is taking place in a CMOS transistor.
The total cells and power consumed both leakage and dynamic power are noted down and are shown in the table III.

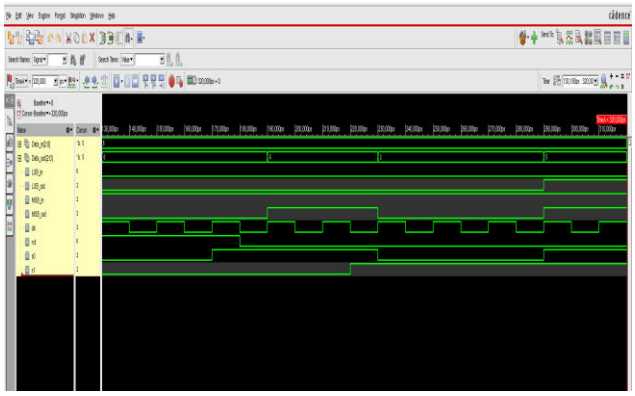

Fig. 6 Simulation waveform of 3 bit USR

TABLE III
PERFORMANCE PARAMETERS OF USR, DFF AND MUX

Circuit	Total cells	Leakage power(nW)	Dynamic power(nW)	Total power(nW)
4:1 Mux	11	0.292	29187.685	29187.977
D flip-flop	7	0.462	27378.974	27379.435
USR	33	1.271	65358.954	65360.226

IV. CONCLUSION

The universal shift register is an essential component in digital circuits which performs four different operations within a single system. Hence a high speed low power consuming universal shift register is necessary. The USR which is designed using Cadence 180nm technology is energy efficient and fast. The results are compared with that of the circuit designed using Xilinx ISE 14.7. Hence highly preferred in high speed and low power applications. Both D flip-flop and 4:1 MUX which are designed are energy efficient and can find its applications in many areas in VLSI.

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