

Design and Comparative Analysis of a Modified Performance Optimized BBL-PT Full Adder In 90nm CMOS Technology

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Abstract -Full adder is one of the basic circuits in arithmetic operations and its performance affects the speed and power dissipation of VLSI systems. Though the existing BBL-PT full adder has low power dissipation and less transistor count; however, there exists voltage stepping in PTL-based sum block due to PMOS restorer circuit which degrades the output signals quality and increases delay. Though the hybrid LP XOR/XNOR full adder eliminates this problem; it increases transistor count. To overcome these problems, three modified BBL-PT full adder designs are proposed. Proposed designs aim for elimination of voltage stepping, reduction in transistor count, reduction in power dissipation, and improvement in Power-Delay Product (PDP). All proposed circuits have been designed and simulated using Cadence Virtuoso at 90nm CMOS technology having supply voltage of 1.2V. Simulation results show improvement in power dissipation, delay, and PDP as compared to the existing full adder designs.



Fig1: BLOCK DIAGRAM OF FULL ADDER

Keywords: Full Adder, BBL-PT, Hybrid Logic, XOR/XNOR, CMOS, PDP, Cadence Virtuoso

I. INTRODUCTION

Today, low-power and high-speed arithmetic circuits play a major role in modern VLSI systems like processors, digital signal processors, communication systems, and portable electronic systems. In various arithmetic circuits, full adder is one of the most important components because full adder is widely used in adders, multipliers, ALUs, and address generation units. Hence, design of a full adder with low power consumption, reduced delay, and improved Power-Delay Product (PDP) is an important area of research.

There are different logic styles like CMOS, Pass Transistor Logic (PTL), Complementary Pass Transistor Logic (CPL), Transmission Gate Logic (TGL), and Hybrid logic styles that have been suggested to improve the performance of full adder. Conventional CMOS full adders have good reliability operation and full voltage swing but they suffer from more transistor count and high power dissipation. PTL-based full adder reduces transistor count and switching capacitance; however, they suffer from threshold voltage loss and degraded output level. Hybrid logic styles make use of different logic styles for improved trade-off between power, delay, and area. Existing BBL-PT full adder uses Branch Based Logic (BBL) in carry block and PTL in sum block to reduce critical path delay and power dissipation. However, there is voltage stepping in PTL-based sum block due to PMOS restorer circuit which degrades the output signal quality and increases delay. To overcome this problem, this paper proposes a modified hybrid full adder using low-power XOR/XNOR structure.

II. LITERATURE REVIEW

Several researchers have proposed various architectures for full adders to improve power efficiency and circuit speed. Zimmermann & Fichtner [1] compare CMOS and Pass Transistor Logic (PTL) full adders for comparison of power, delay, and transistor count. CMOS full adders have reliable operation and full voltage swing but require more number of transistors; while PTL full adders have lesser transistor count and low power dissipation but

suffer from signal degradation and low noise margin. This work shows the need of hybrid approach to combine the benefits of both logic styles.

Chang et al. [2] have reviewed different full adder architectures which are implemented in 0.18 μm CMOS technology including static CMOS, PTL, and hybrid logic. This review work indicates that hybrid logic style achieves good balance between power and delay as compared to the conventional CMOS logic style. It motivates for further design of hybrid full adders. Goel et al. [3] have proposed hybrid CMOS full adders for deep submicron technologies to improve the power, delay, and PDP performance. These hybrid CMOS full adders provide good low voltage operation and driving capability but suffer from increased circuit complexity. Kandpal et al. [4] have designed a 10T XOR-XNOR circuit with full voltage swing in 90 nm CMOS technology. This improved XOR-XNOR circuit helps in reducing power dissipation and delay which leads to better PDP performance when incorporated in full adder circuit.

Suresh et al. [5] have designed a hybrid CMOS full adder using 10T XOR-XNOR module in Cadence Virtuoso. In this design, there is reduction in power dissipation and delay along with improved switching efficiency. Chauhan et al. [6] have designed a hybrid CMOS full adder using 8T grounded keeper XOR-XNOR circuit in 45 nm technology. It improves signal integrity and leakage control along with significant reduction in PDP. Hassoune et al. [7] have proposed a hybrid Branch-Based Logic and Pass Transistor Logic (BBL-PT) full adder for ultra-low-power applications. It is implemented in 0.13 μm CMOS technology and it gives better PDP and lower static power as compared to CMOS and CPL designs. Akshath et al. [8] have proposed a compact 10T full adder using enhanced XOR-XNOR gates to reduce the chip area and power dissipation. Although it achieves energy efficiency but suffers from some disadvantages like voltage degradation and reduced noise margins.

Ishraq et al. [9] have proposed a 16T full adder using static energy recovery XNOR gates and transmission gate logic to overcome the threshold voltage loss. It achieves lower power dissipation and better PDP along with full voltage swing outputs. Jain et al. [10] have designed a 12T hybrid full

adder in 90 nm CMOS technology using Tanner EDA tools. In this design, there is reduction in power dissipation and delay as compared to conventional CMOS full adders; although low transistor count creates signal reliability issues. Trupthi et al. [11] have designed a Ripple Carry Adder using static CMOS logic in 180 nm technology. This design is easy and power efficient but suffers from increased propagation delay with increase in bit width. Das et al. [12] have designed a 14T PTL-based full adder in 90 nm CMOS technology. It achieves reduced power dissipation and faster operation due to lower transistor count; however, signal degradation and driving capability are still problems. Kandpal et al. [13] have proposed a 20T hybrid full adder with modular XOR/XNOR based architecture in 90 nm technology. This design shows significant improvement in delay and PDP. These studies indicate that hybrid logic based full adder achieves improved PDP and lesser transistor count.

III. IMPLEMENTATION

The implementation of different full adder architectures considered in this work. Existing designs such as Conventional CMOS, CPL, BBL-PT, and Hybrid LP XOR/XNOR full adders are studied to understand their operating principles, advantages, and limitations related to power consumption, propagation delay, transistor count, and signal integrity. Based on the limitations identified in these architectures, modified and novel full adder designs are proposed with the objective of achieving improved power efficiency, reduced delay, lower circuit complexity, and enhanced overall performance for low-power VLSI applications.

A. EXISTING BBL-PT FULL ADDER

The existing full adder used in this work is based on the Branch-Based Logic with Pass Transistor (BBL-PT) architecture. The design uses branch-based logic for carry generation and pass transistor logic for sum generation to achieve low power consumption and reduced propagation delay. The carry output is generated using the majority function:

$$C_{out} = AB + BC_{in} + AC_{in} \dots\dots\dots(\text{eq1})$$

while the sum output is generated using:

$$S = A \oplus B \oplus C_{in} \dots\dots(\text{eq2})$$

The branch-based carry structure minimizes switching activity and reduces the critical path delay. The PTL-based sum block decreases transistor count and switching capacitance, thereby improving speed and reducing area.

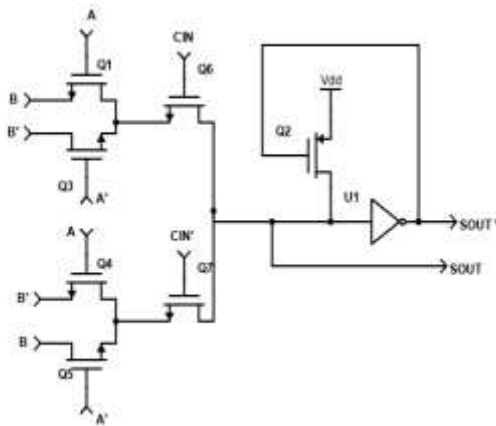


Fig 2(a):sumblock

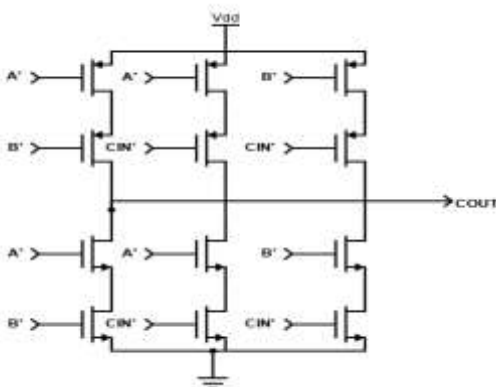


Fig 2(b):carry block

Although the BBL-PT full adder provides improved performance compared to conventional CMOS designs, the sum block suffers from a voltage stepping problem due to the PMOS restorer transistor used in the PTL network. During output transitions, especially from logic '0' to logic '1', the output waveform temporarily remains at an intermediate voltage level before reaching the final output voltage. This degraded transition increases propagation delay and reduces signal integrity and noise margin.

B. PROPOSED DESIGNS

To overcome the voltage stepping problem observed in the conventional BBL-PT full adder, modified hybrid full adder designs are proposed using optimized XOR/XNOR structures and hybrid logic techniques. The proposed circuits improve signal restoration capability and provide clean output transitions without intermediate voltage stepping.

In this work, three hybrid full adder architectures are proposed with the objective of improving power efficiency, propagation delay, transistor count, and overall circuit performance. The proposed designs combine the advantages of Branch-Based Logic (BBL), Pass Transistor Logic (PTL), transmission gate techniques, and CMOS restoration circuits to achieve better speed and lower power consumption compared to existing full adder architectures.

The proposed circuits are based on the standard full adder equations as shown in eq1 and eq2.

Where the sum output is generated using XOR-based hybrid structures and the carry output is implemented using optimized branch-based or CMOS logic networks.

The first proposed design is a Modified BBL-PT Full Adder, which combines Branch-Based Logic for carry generation and Pass Transistor Logic for sum generation. Multiple parallel transistor branches are used to reduce unnecessary switching activity and logic depth, thereby lowering power consumption and improving propagation speed. The sum path uses XOR-based PTL stages along with PMOS restoration transistors to maintain proper logic levels. A controlled current source is also incorporated to stabilize internal node voltages and reduce short-circuit power as shown in fig3. Due to its reduced transistor count and efficient branch structure, the design achieves improved Power Delay Product (PDP) and faster operation compared to conventional architectures.

The second proposed architecture is a Novel BBL-PT Full Adder, designed by separately optimizing the sum and carry paths for better overall performance. The sum generation block uses XOR-based pass transistor or transmission gate logic to minimize transistor count and switching capacitance, while output restoration inverters are used to maintain full

voltage swing. The carry output is implemented using complementary CMOS logic based on the optimized carry expression:

$$C_{out} = AB + C_{in}(A + B) \dots\dots\dots(\text{eq3})$$

This structure allows reuse of intermediate signals and reduces redundant logic operations, resulting in lower propagation delay and improved circuit efficiency as shown in Fig4. The carry path is intentionally designed with fewer logic levels to achieve faster signal propagation and better signal integrity.

The third proposed design uses a hybrid combination of pass transistor logic, transmission gate concepts, and static CMOS inverters to achieve a balanced trade-off between speed, power, and silicon area as shown in Fig 5. In this architecture, the intermediate XOR signal ($X = A \oplus B$) is generated using a reduced transistor pass network and combined with the carry input to produce the final sum output. The carry output is realized using a compact hybrid logic structure :

$$C_{out} = XC_{in} + X'A$$

$$C_{out} = (A \oplus B)C_{in} + (A \oplus B)' \cdot A$$

$$C_{out} = (A'B + AB')C_{in} + (AB + A'B')A$$

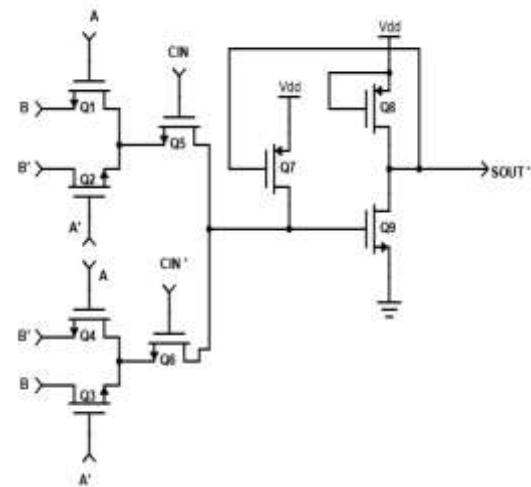
$$C_{out} = C_{in}A'B + C_{in}AB' + AB$$

$$C_{out} = C_{in}(A \oplus B) + AB$$

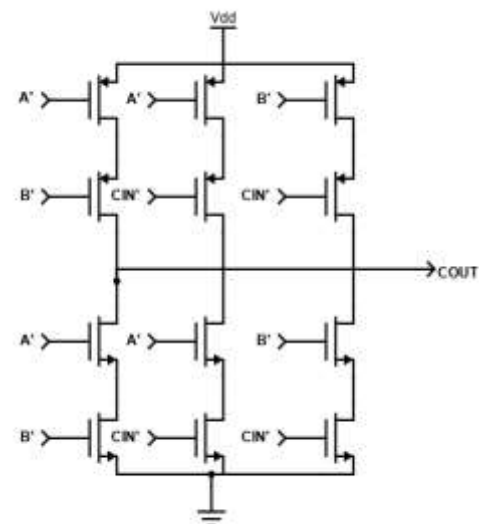
that minimizes transistor count and parasitic capacitances. Output restoration inverters are included to overcome threshold voltage degradation and ensure reliable logic levels. The reduced logic complexity and lower switching capacitance help improve propagation delay, dynamic power consumption, and overall PDP performance.

Overall, the proposed hybrid full adder architectures provide significant improvements in terms of reduced power consumption, lower delay, compact transistor count, and enhanced Power Delay Product compared to conventional CMOS and other existing full adder designs, making them

suitable for modern low-power and high-speed VLSI applications.

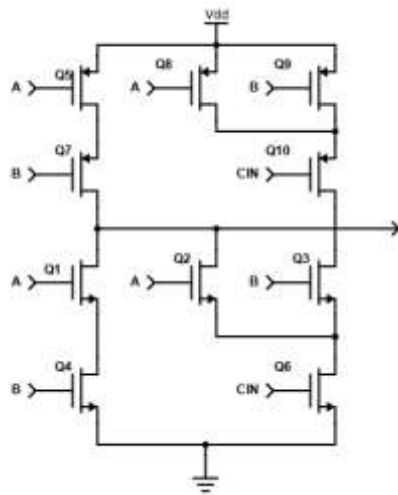


3 (a): sum block



3(b):Carry block

Fig3:proposed circuit 1:3(a)sum block,3(b)carry block



4(a)carry block

Fig4:proposed circuit 2 with modified carry block 4(a).

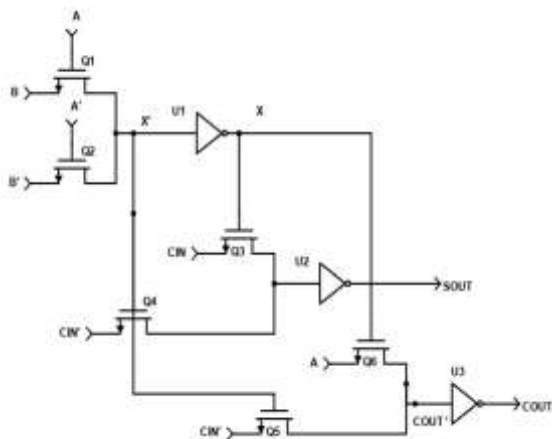


Fig 5 :Proposed circuit 3.

IV. RESULTS

All full adder circuits were designed and simulated using Cadence Virtuoso in GPDK 90nm CMOS technology with a supply voltage of 1.2V. The performance metrics evaluated include propagation delay, average power consumption, transistor count, and Power Delay Product (PDP). The simulation results show that the conventional BBL-PT full adder exhibits a voltage stepping problem in the sum output waveform, resulting in degraded transitions and increased delay. The proposed modified designs successfully eliminate the voltage stepping issue and produce smooth transitions between logic levels.

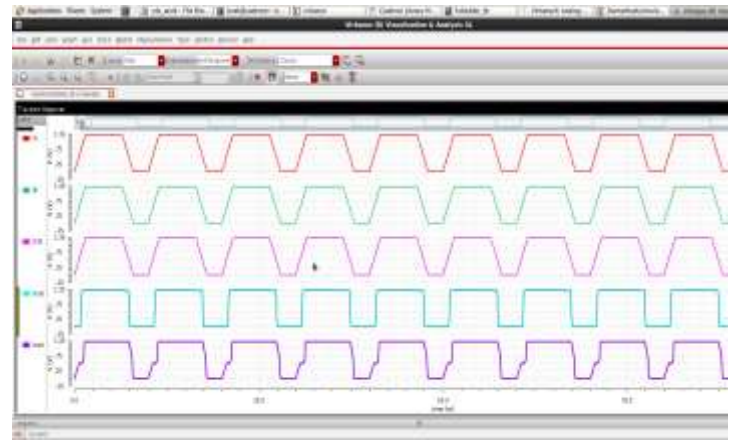


Fig 6 :simulated waveform for the existing BBL-PT FA

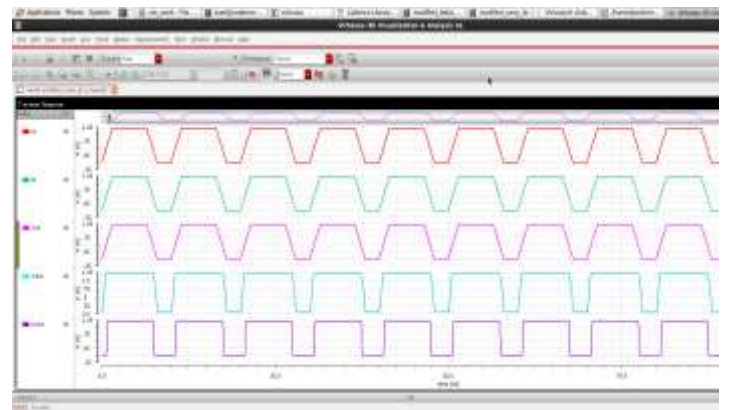


Fig 7 : simulated waveform for the Proposed FA Design 1&2

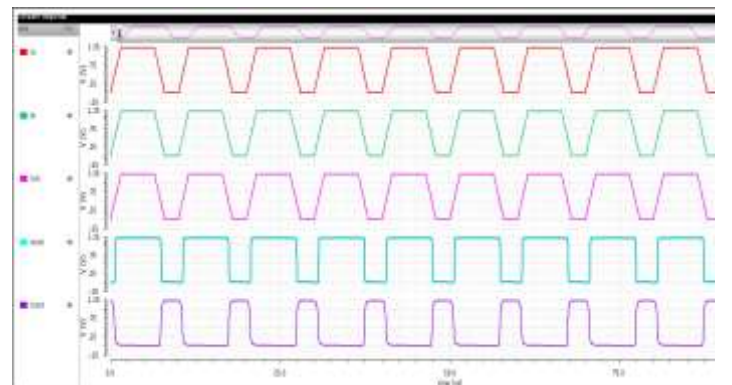


Fig 8: simulated waveform for the proposed circuit 3

A. MOSFET OPERATION ANALYSIS:

To validate the correct logical operation of all three proposed full adder designs a detailed transistor level analysis was carried out. This section describes which transistors are in the ON state and which transistors are in the OFF state for each of the eight possible input combinations of the full adder. This analysis provides a clear understanding of the current conduction paths that are activated for each input condition and confirms that the correct sum and carry outputs are produced in every case for all three proposed designs.

Table 1: MOSFET ON/OFF State Summary for Circuit 3(a) Sum Block

A	B	C _{in}	Q1	Q2	Q3	Q4	Q5	Q6	Q8	Q9	SOUT*
0	0	0	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	1
0	0	1	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	0
0	1	0	OFF	ON	ON	OFF	OFF	ON	OFF	ON	0
0	1	1	OFF	ON	ON	OFF	ON	OFF	OFF	ON	1
1	0	0	ON	OFF	OFF	ON	OFF	ON	OFF	ON	0
1	0	1	ON	OFF	OFF	ON	ON	OFF	OFF	ON	1
1	1	0	ON	ON	ON	OFF	OFF	ON	ON	OFF	1
1	1	1	ON	ON	ON	OFF	ON	OFF	OFF	ON	0

Table 2: MOSFET ON/OFF State Summary for 4(a) Carry Block.

A	B	C _{in}	Active PMOS	Active NMOS	COUT
0	0	0	Q5,Q7,Q8,Q9,Q10	None	0
0	0	1	Q5,Q7,Q9	Q6 only	0
0	1	0	Q5,Q8,Q10	Q3 only	0
0	1	1	None complete	Q3,Q6	1
1	0	0	Q7,Q9,Q10	Q4 only	0
1	0	1	None complete	Q4,Q6	1
1	1	0	Q8,Q9	None complete	1
1	1	1	None complete	Q2,Q3	1

Table 3: MOSFET ON/OFF State Summary for Circuit Fig 5.

A	B	C _{in}	Q1	Q2	Q3	Q4	Q5	Q6	SOUT	COUT
0	0	0	OFF	ON	OFF	ON	OFF	OFF	0	0
0	0	1	OFF	ON	ON	OFF	ON	OFF	1	0
0	1	0	OFF	ON	OFF	ON	OFF	OFF	1	0
0	1	1	OFF	ON	ON	OFF	ON	OFF	0	1
1	0	0	ON	OFF	OFF	ON	OFF	ON	1	0
1	0	1	ON	OFF	ON	OFF	ON	ON	0	1
1	1	0	ON	OFF	OFF	ON	OFF	ON	0	1
1	1	1	ON	OFF	ON	OFF	ON	ON	1	1

Table 4: Comparative Analysis

References used	Circuit diagrams	Delay(ps)	Power(uw)	Power delay product(pdp)	Number of transistors used
[7]	existed BBLPT full adder	278.91	22.42	6.254 f	23
[7]	hybrid full adder	154.12	88.73	9.9183f	24
[9]	full adder using 16T	3.81	48.71 n	186.01 z	16
[12]	Full adder using 14T	3.38	59.37 n	200.76	14
[10]	FA using 12T	113.65	5.65	642.42 a	12
[13]	20T hybrid full adder	31.8	25.8	820.44 a	20
[5]	Hybrid CMOS full adder using 10t XOR circuit	43.2	25.9	1106.82 a	20
[8]	full adder using 10T	2.21	41.99 n	92.97 z	10
Present work	proposed circuit 1	19.64	40.01	785.90 a	23
Present work	proposed circuit 2	20.44	21.84	446.55 a	21
Present work	proposed circuit 3	75.91	11.14	846.46 a	18

compared to the conventional BBL-PT full adder. Among all proposed architectures, Proposed Design 2 achieves the best overall PDP performance, while Proposed Design 3 achieves the lowest transistor count and power consumption.

V. CONCLUSION

This work presented the design and comparative analysis of three modified BBL-PT based full adder architectures implemented using 90 nm CMOS technology. The study began by analyzing existing full adder designs, including Conventional CMOS, Complementary Pass Logic (CPL), the BBL-PT full adder, and the Hybrid LP XOR/XNOR full adder. Although these architectures offer improvements in specific performance metrics, the conventional BBL-PT full adder suffers from a voltage stepping problem in the PTL-based sum block due to the PMOS restorer, while the Hybrid LP XOR/XNOR design increases transistor count and circuit complexity. These limitations motivated the development of modified BBL-PT architectures capable of achieving a better balance between power consumption, propagation delay, transistor count, and signal integrity.

To address these challenges, three modified full adder architectures were proposed with different optimization

objectives. The first design improves voltage stability by incorporating a current-source-assisted sum block, the second design employs optimized hybrid logic with separate sum and carry paths to reduce the critical path delay, and the third design utilizes a compact hybrid pass transistor structure to minimize transistor count and switching capacitance. Simulation results obtained using Cadence Virtuoso demonstrate that all three proposed designs successfully eliminate the voltage stepping issue and improve the overall performance of the full adder. Among them, Proposed Design-2 achieves the best overall Power-Delay Product (PDP) and propagation delay, whereas Proposed Design-3 offers the lowest transistor count and power consumption. These results indicate that the proposed architectures are promising candidates for energy-efficient and high-speed arithmetic circuits in modern VLSI systems.

VI. FUTURE SCOPE

Future work may focus on implementing the proposed full adder architectures in advanced CMOS technology nodes such as 45 nm, 28 nm, and 16 nm to evaluate their performance under deep-submicron conditions. The designs can also be extended to multi-bit arithmetic circuits, including Ripple Carry Adders (RCA) and Carry Look-Ahead Adders (CLA), to assess their scalability. Furthermore, layout implementation with DRC/LVS verification and FinFET-based realization can be explored to investigate silicon area, manufacturability, leakage power, and overall performance in next-generation low-power VLSI applications.

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