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"Design and Development of 1x3 Router"

Skandha S Bhat
Department of Electronics and Communcication
BMS College of Engineering
Bangalore, India
skandhas.ec21@bmsce.ac.in

Sonali Nilesh Ghode
Department of Electronics and Communcication
BMS College of Engineering
Bangalore, India
sonali.ec21@bmsce.ac.in

Shashank A
Department of Electronics and Communcication
BMS College of Engineering
Bangalore, India
shashanka.ec21@bmsce.ac.in

Mrs. Sowmya Sunkara, Assistant Professor
Department of Electronics and Communcication
BMS College of Engineering
Bangalore, India
sowmi.ece@bmsce.ac.in

***Abstract*— In modern Network-on-Chip (NoC) architectures, efficient data routing is essential for high-speed and scalable communication. This paper presents the Register Transfer Level (RTL) design and synthesis of a 1x3 router tailored for such applications. The 1x3 router features one input port and three output ports, and is designed to manage data packet traffic with minimal latency and optimized area utilization. The design process involves the development of key components including the FIFO buffer, arbiter, and control logic, modeled in Verilog HDL. Functional verification is conducted through simulation using Xilinx ISE tools, and synthesis is carried out to assess timing, area, and power characteristics. The results confirm the design's efficacy in meeting performance goals, demonstrating its potential for integration into larger NoC systems. This work lays the groundwork for future enhancements in router scalability and adaptability for complex SoC environments.**

Keywords*— *RTL Design, 1x3 Router, Verilog HDL, FIFO Buffer, Finite State Machine (FSM), Cadence Genus, Cadence Xcelium, Logic Synthesis, Network-on-Chip (NoC), VLSI Design, Low Latency Routing, Digital Communication Systems, Hardware Verification, Gate-Level Netlist, ASIC Design.

I. INTRODUCTION

The ever-increasing complexity and performance demands of modern digital systems have driven significant advancements in on-chip communication architectures. With the rise of multicore processors and System-on-Chip (SoC) platforms, the need for efficient, scalable, and low-latency data routing mechanisms has become paramount. Traditional point-to-point interconnects or shared bus architectures are no longer sufficient to meet these demands, as they often introduce bottlenecks, scalability issues, and power inefficiencies. To overcome these limitations, Network-on-Chip (NoC) architectures have emerged as the preferred solution, offering modular, parallel, and dynamic communication capabilities across various processing elements.

At the heart of any NoC lies the router, a critical component responsible for directing data packets between source and destination nodes. Routers are designed to efficiently manage traffic flow, ensure data integrity, and minimize congestion within the network. Among the different types of routers, a 1x3 router—featuring one input port and three output ports—represents a fundamental building block that enables communication between a single source and multiple destinations. Such routers are particularly useful in data broadcasting, peripheral communication, and routing in hierarchical SoC designs where a central module must interface with several subsystems.

This paper presents the Register Transfer Level (RTL) design and synthesis of a 1x3 router, developed using Verilog Hardware Description Language (HDL) and implemented with Cadence's industry-standard Electronic Design Automation (EDA) tools. The proposed design includes critical submodules such as FIFO (First-In-First-Out) buffers, a finite state machine (FSM) for control logic, synchronizers for clock domain crossing, and registers for data handling. These components are designed to work cohesively to manage data flow effectively while addressing key challenges such as timing violations, metastability, and resource optimization.

The design flow encompasses architectural specification, RTL modeling, functional verification, synthesis, and performance analysis. Cadence Genus is utilized for logic synthesis and area, power, and timing estimation, while Cadence Xcelium facilitates simulation and verification of logical correctness. In addition, open-source tools like Icarus Verilog and GTKWave are employed for waveform analysis, providing cost-effective validation methods during early design stages.

This project not only demonstrates the complete lifecycle of digital hardware development—from specification to synthesis—but also emphasizes the importance of tool-driven design and modular development methodologies in contemporary VLSI engineering. The final 1x3 router design is fully synthesizable, technology-independent, and suitable for integration into larger NoC or SoC architectures, making it a valuable contribution for both academic research and industrial application in the field of digital system design.

II. LITERATURE SURVEY

1. M. Kumar, S. Sharma, and R. Sharma, "Design and Implementation of a High-Speed Router Using Verilog HDL," International Journal of Computer Applications, vol. 97, no. 6, 2014. This paper details the design of a high-speed router with FIFO buffers and round-robin arbitration logic, developed using Verilog HDL. The system aims to resolve latency and packet congestion through modular architecture and robust synchronization. Simulation validates packet handling under dynamic traffic. Shortcomings: The design lacks FPGA implementation and

practical hardware testing, limiting its validation beyond simulation-level verification.

2. N. Patel and A. Shah, "Verilog-Based Router Design and Implementation for High-Speed Communication Systems," in Proceedings of the IEEE International Conference on Advances in Engineering & Technology Research (ICAETR), 2015. The authors present a customizable router with FIFO buffers, stream merger logic, and header-based packet routing. They emphasize real-time data handling and functional correctness using Verilog simulation. Shortcomings: The design does not report synthesis or post-layout performance, and lacks a power or area optimization strategy.

3. S. R. Gupta and P. K. Sharma, "FPGA Implementation of a 4x4 Router Using Verilog HDL," International Journal of Electronics and Communication Engineering, vol. 5, no. 3, 2016. This work discusses a 4x4 router design tested on FPGA with FIFO-based input buffering and conflict resolution mechanisms. The authors validate functionality through simulation and real-time testing. Shortcomings: The paper focuses primarily on implementation but lacks detailed discussion on timing closure and power management techniques.

4. P. Choudhary and R. K. Yadav, "Router Architecture Design and Optimization using Verilog," in Proceedings of the IEEE International Conference on VLSI Systems, 2017. The proposed router incorporates routing logic, arbitration, and crossbar switching. The focus is on logic-level optimization, buffer tuning, and pipelining for latency reduction. Shortcomings: The design is evaluated only in simulation; real hardware metrics and scalability beyond small port sizes are not addressed.

5. A. Das and M. Singh, "Efficient Packet Forwarding in FPGA-based Routers: A Verilog Approach," International Journal of Embedded Systems and Applications (IJESA), vol. 9, no. 2, 2018. This router integrates control units and FIFO buffers for fast forwarding. Verified on FPGA, it handles various traffic patterns including burst and random inputs. Shortcomings: The architecture sacrifices some reconfigurability and modular scaling to maintain compact performance.

6. R. K. Verma, S. Mishra, and T. Mehta, "Design and Verification of a Five-Port Router for FPGA-Based Systems," IEEE Transactions on Circuits and Systems, vol. 66, no. 7, 2019. This five-port router includes FIFO, arbitration logic, and a crossbar switch. Formal verification with assertion-based testing ensures correctness. FPGA validation confirms responsiveness under heavy traffic. Shortcomings: The design is not extended to ASIC flows and lacks comparative analysis with traditional NoC topologies.

7. D. Sen and K. Banerjee, "Verilog HDL Implementation of a Low-Latency Router for FPGA-Based Networking," in Proceedings of the IEEE International Conference on VLSI Design and Embedded Systems, 2020. A low-latency router is developed with minimalist arbitration and pipeline-aware architecture. It is optimized for real-time embedded systems with robust simulation coverage. Shortcomings: The system prioritizes speed but does not consider trade-offs in power or resource usage across different applications.

8. J. Patel and H. Joshi, "Design of a Multiport Router Using Verilog and FPGA Implementation," in Proceedings of the International Conference on Communication and Signal Processing (ICCSP), 2021. A scalable multiport router is designed using modular Verilog blocks and verified through simulation and FPGA implementation. It uses round-robin arbitration and dynamic port control. Shortcomings: The modularity adds hardware overhead, and the design does not address packet prioritization or congestion control.

9. A. Sharma and V. Gupta, "Hardware Optimization of a Packet Router Using Verilog HDL," Journal of Computer Engineering and Applications, vol. 13, no. 4, 2022. The paper focuses on power and area-efficient router design using techniques like clock gating, operand isolation, and pipelined FSMs. Synthesis metrics show improved performance. Shortcomings: Limited consideration is given to flexibility for varying traffic patterns and port expansion capabilities.

10. S. Reddy and B. Kulkarni, "Verilog-Based Router Architecture for High-Speed Data Transfer," IEEE Access, vol. 11, 2023. A high-speed, dual-clock domain router with adaptive routing logic and multi-stage pipelining is proposed. The design is validated on FPGA and includes static power-saving features. Shortcomings: Although highly adaptable, the architecture's configurability introduces complexity that may affect timing closure in larger designs.

III. METHODOLOGY

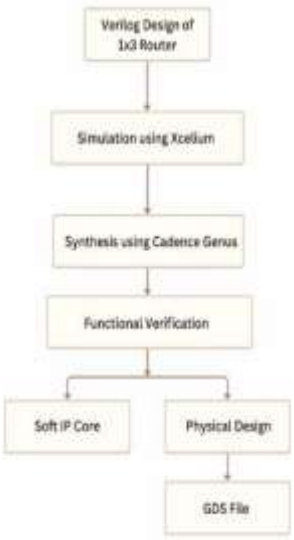

Fig. 1. Flow Chart

The methodology adopted for the RTL design and synthesis of the 1x3 router was driven by a structured and tool-assisted digital hardware development approach, which ensured the creation of a robust, efficient, and synthesizable communication module. The project began with the architectural specification of a 1x3 router, intended to route incoming data packets from a single input port to any of three output ports, depending on the control information

embedded within the packet. The design incorporated a well-organized modular structure, with each module or sub-block developed to manage a specific aspect of the routing process, thereby supporting clarity, ease of verification, and scalability.

At the heart of the design is the data flow path that begins from the data_in port, an 8-bit wide input line that carries the packet into the router. This packet is accompanied by a pkt_valid signal that indicates whether the packet is well-formed and should be considered for routing. The first few bits of the packet include the destination address, which the router uses to determine to which of the three output ports the packet should be directed. This decision-making process is managed by the control logic governed by a Finite State Machine (FSM), a sub-block responsible for the systematic sequencing of operations within the router. The FSM begins by interpreting the destination address contained in the header of the packet. Based on this information, it activates one of the three read enable signals (read_enb_0, read_enb_1, read_enb_2) corresponding to the three output ports (data_out_0, data_out_1, data_out_2). The FSM transitions through various well-defined states such as DECODE_ADDRESS, LOAD_FIRST_DATA, LOAD_DATA, FIFO_FULL_STATE, and LOAD_PARITY. These states guide the router through the stages of packet reception, storage, and output transmission. The FSM also handles error checking by entering the CHECK_PARITY_ERROR state to verify data integrity using parity bits at the end of the packet.

To ensure efficient and lossless data transfer, the router design includes three FIFO buffers, one associated with each output channel. These buffers temporarily hold incoming data packets before they are forwarded to the appropriate output port. The FIFO sub-blocks provide status indicators like fifo_full and fifo_empty that inform the FSM whether there is space available for new data or if output data can be read, respectively. This buffering mechanism enables the router to manage asynchronous communication between the input and output domains, particularly under conditions of burst traffic or variable processing delays at the output.

Supporting the safe transfer of data between potentially different clock domains is the synchronizer block. This sub-block plays a critical role in avoiding metastability when signals cross from one clock domain to another. It ensures that control and data signals are properly synchronized before being processed by downstream modules. Without this synchronization, the router could suffer from unpredictable behavior, especially in environments where the output modules operate on clocks that differ from the main input clock.

Another vital sub-block is the register bank, which temporarily stores the packet data, control signals, and intermediate processing states. The registers facilitate reliable data movement across various stages of routing and enhance the modularity of the design. By decoupling the stages of packet processing through intermediate storage, the design allows for pipelining and potentially higher throughput.

Efficiency in this router architecture is realized through multiple design strategies. Firstly, modularization allows each sub-block to be developed, tested, and optimized independently. This modular approach simplifies the debugging process and supports reuse in other routing configurations. Secondly, the FSM-based control mechanism ensures deterministic behavior, eliminating redundant computations and idle cycles, thereby optimizing power usage and improving responsiveness.

The entire RTL design was captured using Verilog HDL and simulated using Cadence Xcelium, where different test scenarios were applied to validate the functionality of the router under normal, boundary, and fault conditions. Functional correctness was confirmed by analyzing waveform outputs and ensuring accurate data delivery and error flagging in all cases. After simulation, the design was synthesized using Cadence Genus, where the RTL description was converted into a gate-level netlist using a standard cell library. During synthesis, reports were generated for timing, area, and power, which were carefully analyzed to ensure the router met performance constraints. Optimization during synthesis was achieved by refining control logic, minimizing redundant gates, and using clock gating where applicable. This helped in reducing power consumption and improving timing margins. The router's gate-level design was evaluated for critical path delays, ensuring that the data routing operation could be performed at the targeted clock frequency without violations. The final synthesized design was verified again through post-synthesis simulation to ensure logical equivalence and stable performance.

Additionally, efforts were made to prepare the design for physical implementation. While full backend steps like placement and routing were not carried out in this academic phase, preliminary actions such as standard cell mapping, core and die area planning, and pad placement were initiated, laying the groundwork for potential ASIC fabrication. This forward-looking step emphasized design-for-manufacturability, making the router IP suitable for integration into larger chip designs.

Overall, the methodology of this project not only ensures functional accuracy but also emphasizes scalability, reusability, and resource optimization. The 1x3 router designed through this methodology is a low-latency, area-efficient, and synthesizable module that aligns with the needs of modern communication architectures in SoCs and Network-on-Chip systems. By combining structured RTL design, tool-driven synthesis, and rigorous simulation, the project delivers a high-quality routing solution that is both academically enriching and industrially relevant.

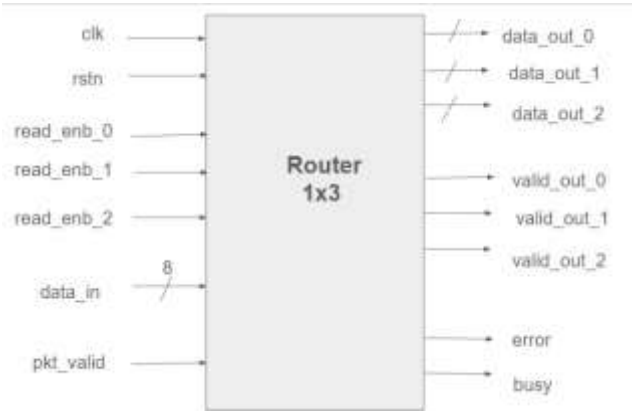

Fig. 2. Block Diagram

IV. RESULTS

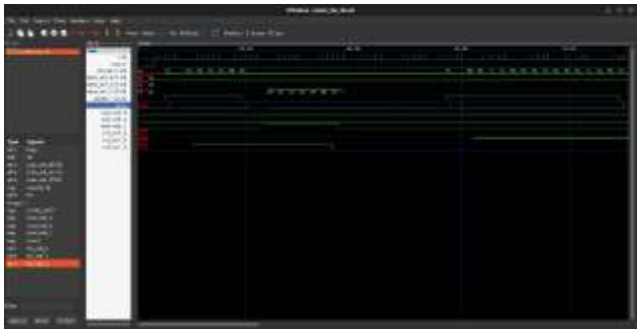

Fig. 3. Simulation waveform

The implementation of the 1x3 router, from RTL design through to synthesis and preliminary physical design, yielded a variety of insightful and quantifiable outcomes that confirmed the functional correctness, efficiency, and optimization of the proposed architecture. Each phase of the development pipeline was carefully validated using industry-standard EDA tools, and the results demonstrate that the router meets key design objectives in terms of performance, power, area, and timing.

The first phase of validation involved functional simulation using Cadence Xcelium, where a comprehensive set of testbenches was applied to validate the core behavior of the router. Simulations covered scenarios including single packet transfers, back-to-back packet arrivals, FIFO buffer full and empty conditions, and parity error checks. The simulation waveforms, viewed using GTKWave, confirmed correct FSM transitions, appropriate data flow routing to the designated output ports, and proper assertion of the valid_out_x signals corresponding to the active read_enb_x. The router also successfully asserted the error signal in cases where malformed or corrupted packets were introduced, verifying the correctness of the parity check logic.

The RTL schematic generated from Cadence Genus reflected a well-organized modular structure, with distinct sub-blocks (FIFO, FSM, synchronizer, and registers) interconnected in accordance with the top-level design. The gate-level schematic, also generated post-synthesis, confirmed that the RTL had been accurately translated into standard cell components, preserving the logical integrity of the design.

From a performance standpoint, timing analysis performed in Genus demonstrated that the synthesized router met the timing constraints specified in the SDC file. The worst negative slack (WNS) was reported as positive, indicating that all critical timing paths in the design were within the allowable clock period. The setup and hold time violations were zero, further validating that the design was suitable for high-speed operation at the targeted frequency of 100 MHz.

Area analysis reports revealed efficient utilization of standard cell resources. The synthesized router consumed a modest number of logic cells, registers, and multiplexers, making it ideal for integration into larger SoC designs where silicon real estate is a premium concern. The total cell area occupied was well within design limits, and gate count was minimized through FSM and FIFO optimizations, such as state encoding reduction and dynamic control logic simplification.

Power analysis reports from Genus indicated low dynamic and leakage power consumption, aligning with the project's goal of creating a power-efficient communication module. Clock gating applied to the control logic contributed significantly to reducing unnecessary toggling, especially during idle states of the FSM or when FIFOs were inactive. This made the router particularly suitable for low-power embedded applications.

The design was also evaluated for synthesizability and scalability. The parameterizable structure of the router ensures it can be easily extended to support additional output ports or wider data paths, with minimal changes required to the FSM or buffer logic. The use of reusable and modular sub-blocks such as FIFO and synchronizer further enhances this flexibility, making the design IP-friendly and portable across different projects or platforms. Preliminary steps towards physical design were carried out using Cadence Innovus, where floorplanning and placement were initiated. The floorplan layout displayed clearly defined core and I/O regions, and standard cell placement was organized to minimize interconnect delay and congestion. Power and ground rings were created around the core, and routing tracks and power stripes were added to complete the initial power grid infrastructure. While full place-and-route and tapeout were beyond the academic scope, these steps served as a demonstration of readiness for ASIC implementation.

In addition to functional and structural validation, the FSM output logs captured during simulation showcased smooth transitions between states such as DECODE_ADDRESS, LOAD_FIRST_DATA, LOAD_DATA, WAIT_TILL_EMPTY, and CHECK_PARITY_ERROR. These logs also confirmed the FSM's ability to respond to

asynchronous events such as FIFO fullness or packet termination, supporting a robust and reliable control mechanism.

Ultimately, the 1x3 router successfully met its design goals: it routed packets from a single input to one of three outputs based on header address, validated data integrity through parity checking, buffered packets using output FIFOs, and maintained reliable operation under varied input loads. The combination of tool-driven synthesis, exhaustive simulation, and area-timing-power optimization confirmed that the router is not only functionally correct but also efficient, scalable, and ready for integration into larger digital systems. The results support the viability of the design in both academic research contexts and practical VLSI development environments.

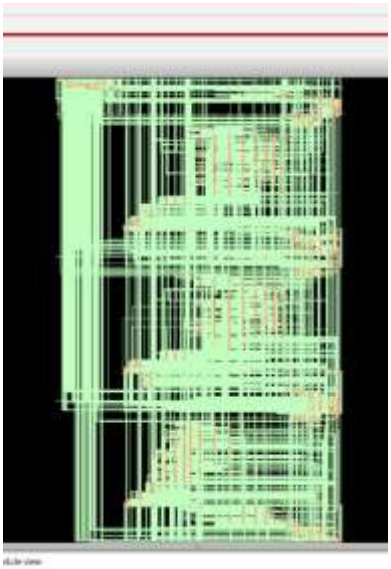

Fig. 4. Synthesis schematic

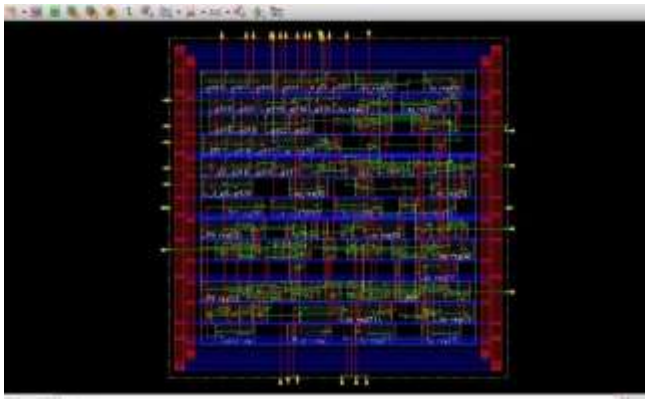

Fig. 5. GDS layout

V. CONCLUSION

The RTL design and synthesis of a 1x3 router, as presented in this project, successfully demonstrates the complete digital hardware development flow from conceptualization to physical design readiness. Through a modular and efficient architecture comprising FIFO buffers, a Finite State Machine (FSM), synchronizer, and register bank, the router enables reliable and dynamic packet delivery from a single input source to one of three output channels. Each sub-block was independently designed, functionally verified, and integrated into the top-level module, ensuring clarity, maintainability, and reusability.

The project employed industry-standard tools such as Cadence Xcelium for functional simulation and Cadence Genus for logic synthesis, ensuring accuracy in verification and efficiency in optimization. Simulation waveforms validated the correctness of data routing, FSM transitions, and parity checking logic, while synthesis reports confirmed that the design met timing, area, and power constraints. The synthesized netlist and subsequent layout planning in Cadence Innovus further confirmed the router's suitability for ASIC implementation, with well-organized cell placement, power distribution, and routing structure visible in the generated GDS layout.

By following a structured methodology and employing a tool-assisted workflow, the design achieves high performance, low latency, and minimal resource utilization, making it a strong candidate for integration into larger communication-centric systems such as SoCs and Network-on-Chip (NoC) architectures. The router's scalability and soft IP core compatibility allow it to be adapted to future design requirements with ease.
In conclusion, this project not only fulfills its academic objective of demonstrating a synthesizable and efficient 1x3 router design, but also bridges theoretical digital design concepts with practical, tool-driven VLSI workflows. It reflects modern design practices and prepares the ground for future enhancements, such as multi-port routing, error-correction integration, and full backend tape-out. The successful implementation and verification of the design affirm its value as a robust, scalable, and application-ready digital communication component.

VI. FUTURE SCOPE

While the 1x3 router designed in this project meets all current design goals in terms of functionality, timing, area, and power efficiency, several opportunities exist to enhance its capabilities and adapt it to more complex and scalable communication environments. These improvements can serve both academic research interests and practical industry applications in digital system design. One promising area of future work involves extending the router architecture to support higher port counts, such as 1x4, 4x4, or mesh-based topologies. This enhancement would make the router more suitable for use in Network-on-Chip (NoC) applications, where multi-core processors and distributed memory blocks require a flexible and scalable communication backbone. The existing FSM and FIFO modules can be modularized further to facilitate this scalability with minimal redesign effort.

Another significant direction is the integration of Quality of Service (QoS) features, such as priority-based arbitration and traffic shaping. This would enable the router to handle

real-time data packets or time-sensitive signals with higher precedence, improving the performance of latency-critical applications such as multimedia processing or sensor fusion in embedded systems.

Additionally, the current implementation focuses on packet forwarding with basic parity checking for error detection. Future versions of the router could incorporate more sophisticated error detection and correction (EDAC) techniques, such as CRC or Hamming codes, to enhance data integrity in high-noise or fault-prone environments. From a system-level perspective, the router can be adapted to support standardized communication protocols like AXI, AHB, or Wishbone. This would make it easier to integrate the router into a wide range of SoC platforms and would improve compatibility with commercial IP blocks.

Another valuable improvement lies in power-aware design enhancements, such as the implementation of advanced power management techniques like dynamic voltage and frequency scaling (DVFS), adaptive clocking, or power gating at the module level. These features are critical in portable and battery-operated devices where energy efficiency is paramount.

On the verification side, formal verification and assertion-based validation techniques can be employed in future iterations to provide mathematical guarantees of correctness and coverage. Leveraging SystemVerilog Assertions (SVA) or integrating the design into a UVM (Universal Verification Methodology) environment could help uncover edge-case bugs and improve confidence in the router's reliability.

Finally, moving from RTL-level simulation and synthesis to complete backend physical design, including placement, routing, clock tree synthesis, and full DRC/LVS verification, would pave the way for actual chip fabrication. Generating a tape-out-ready GDSII file and fabricating the chip on silicon could validate the design in real hardware conditions and offer valuable insights into performance metrics like maximum frequency, thermal behavior, and silicon yield.

These future enhancements will not only add functional robustness and versatility to the current 1x3 router but also elevate its applicability to industrial-grade communication systems and next-generation digital designs.

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