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DESIGN AND FPGA IMPLEMENTATION OF 8-BIT VEDIC MULTIPLIER

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Abstract - *This paper awaits the design of the Vedic Multiplier using the Ancient Indian Technique known as the Vedic Mathematics modified to improve the performance of processors. Processor performance is highly dependent on the frequency used which is one of the Basic hardware block in most processing systems. This paper describes the design of a powerful 8-bit fast-paced architecture using the Urdhva – Triyakbhyam Sutra Vedic method of repetition. This 8-bit multiplier is designed using four 4-bit multipliers and 3 Ripple Carry Adders. This 8-bit Vedic Multiplier was coded with VHDl integrated and copied using Xilinx software ISE14.2 and performed the same on FPGA (Spartan 3E).*

1.INTRODUCTION

Introduction With the growing and growing demand for VLSI technology, more and more people are pushing for portable, dynamic and embedded digital signal processing (DSP) systems. In implementing the many algorithms of Fast Fourier Transform (FFT), Discrete Fourier Transform (DFT) etc., duplicates of high speed and low power are very important. In today's world many signal and data processing operations involve duplication. Although speed is a very important factor in the VLSI problem, therefore an increase in speed can be achieved by reducing the number of steps required in the calculation process, thereby increasing the efficiency of the designed system. We can use Urdhva-Tiryak-Bhyam in the construction of a multiplier at high speeds to reduce delays at least as much as we can. Vedic mathematics is the name given to an ancient Indian mathematical system that was rediscovered in the early twentieth century. Vedic figures are based primarily on sixteen principles or a formula called the Sutras. Urdhva-Tiryak-Bhyam is the name given to the Sutra meaning Direct-Crossing. this sutra was traditionally used in ancient India to multiply two decimals by a relatively short period of time. The software implementation of the above method is done using the FPGA kit. FPGA provides a hardware location where dedicated processors can be tested for performance. They perform a variety of high-speed functions that can be detected by a simple microprocessor. The main benefit offered by FPGA is Site Design. Therefore, create an ideal platform to use and test the performance of a dedicated processor designed using HDL

2. LITERATURE SURVEY

P.S.H.S.Lakshmi, S.Rama Krishna and Chaitanya "High Speed and Low Power 4-Bit Multiplier".
This research paper discusses the circuit design of the new high speed and low power 4-bit Braun Multiplier. The multiplier is used using different power reduction techniques. The design uses sensible CMOS circuits to reduce power consumption while maintaining computer performance. It presents an accurate way to emulate a product of power dissipation, delay and power delay, using 250nm technology with a given power of 2.5v. 41% power dissipation and approximately 26% delay are decent levels of power outages.

Rutuparna Panda, M.Pradhan, "Speed Comparison of 16 * 16 Vedic multipliers".
This research paper introduces the concepts behind the repetition methods of "Urdhva-Tiryak-Bhyam Sutra" and "Nikilam Sutra". It then demonstrates the design of a 16x16 bit Vedic Multiplier module using the Urdhva-Tiryak-Bhyam Sutra. The paper then expanded 16x16 Vedic repetition using the "Nikilam Sutra" method. The module uses four 8x8 Vedic multipliers, one 16-bit adder adder, and two full 17-item adders. This 16x16 Vedic multiplier is used on the Spartan 2 FPGA XC2S30-5pq208 device. The results of performance testing based on speed and device usage are compared to previous recurrence structures.

Siba Kumar Panda, Ritisnigdha Das, S K Saifur, and TapasaRanjan "VLSI Introduction to Vedic Multiplier Using Urdhva-Tiryak-Bhyam Sutra in VHDL Environment: A Novelty"
This research paper anticipated the design of the Vedic Multiplier novel using Old Indian Vedic Mathematics techniques modified to improve its functionality. In this paper an 8-bit multiplier uses new Vedic Mathematics methods called Urdhva-Tiryak- Bhyam Sutra which is used to produce part of the products. The addition of a product component to Vedic Multiplier is done using the

carry-skip process. The 4x4 Vedic Multiplier is designed using a full 9 adder and a special 4-bit adder with reduced latency. Then an 8-bit multiplier is designed using four 4-bit multipliers and an adder with 3 ripple. VHDL code for more duplicates is created in the Xilinx ISE 8.2 software.

P.Verma, K.K.Mehta, "Effective multiplication based on Vedic Mathematics using the EDA Tool"

This paper shows a very high 8x8 bit Vedic multiplier architecture that is very different from the usual method of multiplication such as addition and subtraction. It produces all the incomplete products and its quantity in one step. This also provides opportunities for modular design where smaller blocks can be used for larger designs. The complexity of the design is therefore reduced to a large number of inputs. bits and modularity increase. The VHDL code for the above design is copied using the EDA (Electronic Design Automation) Tool

PROPOSED SYSTEM

URDHVA-TRIYAKHBYAM (UT)

Vedic Mathematics was rebuilt from ancient Indian texts (Vedas) by Swami BharatiTirthaji Maharaja (1884- 1960) after his eight years of research on the Vedas. Vedic Mathematics is based on sixteen principles or word-formulas called sutras. Urdhva-Tiryak-Bhyam is one of the sixteen Sutras. The word „Urdhva-Tiryak-Bhyam" is a Vedic sutra literally meaning vertically and crosswise. Usually this sutra is used to multiply two numbers in a decimal number system. The advantage of using this type of multiplier is that with the increase in the number of bits, both the delay and space increase at a much lower value compared to other standard multipliers

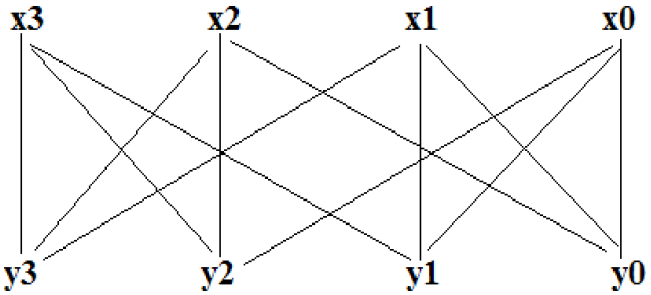

Fig-1.] Example of 4-bit multiplication using (UT)

Step 1: x0*y0

Step 2: x1*y0+x0*y1

Step 3: x2*y0+x0*y2+x1*y1

Step 4: x3*y0+x0*y3+x2*y1+x1*y2

Step 5: x3*y1+x1*y3+x2*y2

Step 6: x3*y2+x2*y3

Step 7: x3*y3

MULTIPLIER ARCHITECTURE

The architecture design of 2x2,4x4 and 8x8 bit vedic multiplier module is shown below. The importance of Vedic duplication is that here the partial products and additives are made in conjunction. Therefore, they are well aligned with the same processing, which also reduces the delay which is the main motivation behind this work.

A] Vedic Multiplier 2x2 bit module

The method shown below is for two bit numbers, 2 which is X and Y when X = x1x0 and Y = y1y0. Initially, the smaller beats are repeated and the key bits of the final product (vertical) are obtained. Then the LSB multiplication is repeated with the next high bit of the multiplier and added, with the LSB multiplication output next at the top. bit of the multiplicand (crosswise) .The amount gives the second part of the final product and the bearing is added to the product by the fraction obtained by multiplying the MSB pieces to give the corresponding amount and bearing. The 2x2 bit Vedic multiplier is operated using the four gates AND the two component add-ons shown in their block diagram in Fig 2. The same method can be extended to 4 -bit and 8-bit inputs but with increasing number. bits architectural design becomes very complex.

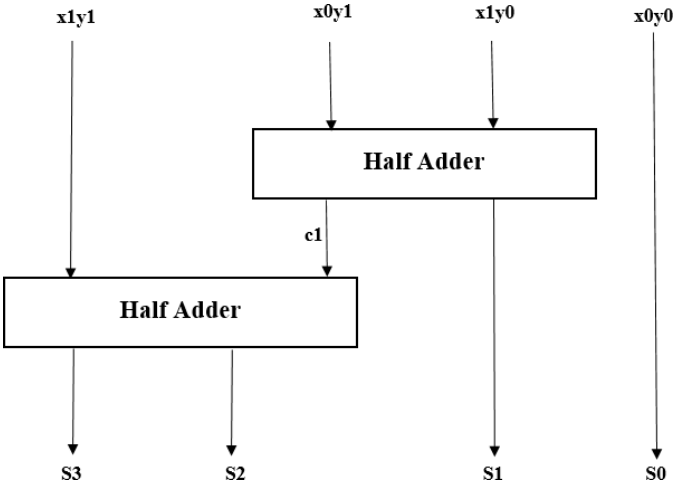

Fig-2.] Block diagram of 2x2 bit Vedic multiplier

B] Vedic Multiplier for 4x4 bit module

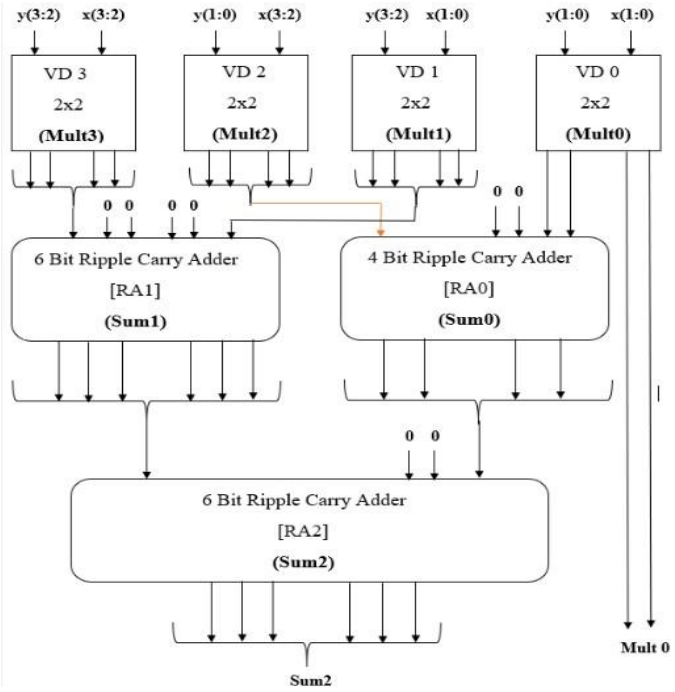

Fig-3.] Block diagram of 4x4 bit Vedic multiplier

The 4x4 bit vedic multiplier module is implemented using four 2x2 bit vedic multiplier modules as shown in fig.3. Let‟s analyze 4x4 multiplications, say X= X3X2X1X0 and B=B3B2B1B0. The output line of the multiplication result is your connection to both Sum 2 and Mult 0. In order to understand the concept,the block diagram of 4x4 bit multiplier is shown in fig.3.To get the final product (Sum2 and Mult0), four 2x2 bit multipliers two 6-bit ripple carry adder and one 4- bit ripple carry adder is used. In addition 8x8 bit Vedic multiplier modules are used using four 4x4 bit multiplication modules.

C.] Vedic Multiplier for 8x8 bit module

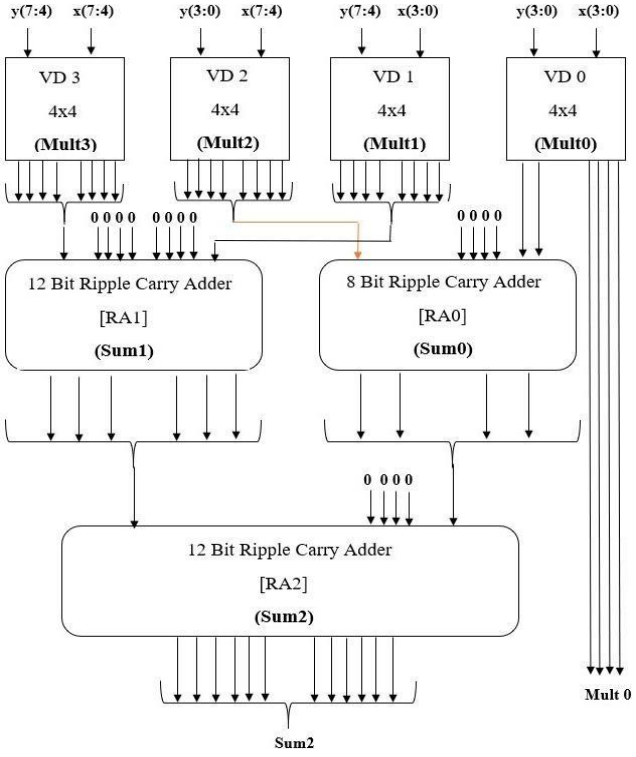

Fig-4.] Block diagram of 8x8 bit Vedic multiplier

The 8x8 bit Vedic multiplier module as shown in block diagram in fig. 4 can be easily implemented using four 4x4 bit Vedic multiplier modules Let‟ analyze 8x8 multiplications, say

X=X7X6X5X4X3X2X1X0 and

Y=Y7Y6Y5Y4Y3Y2Y1Y0. The output line for multiplication result will be of 16 bits and it would be the contactnation result of both Mult0 and Sum2. Let‟s divide X and Y into two parts, say the 8-bit multiplicand X can be decomposed into pair of four bits.Similarly multiplicand Y can be decomposed into pair of four bits. Using fundamentals of Vedic multiplication, taking four bits at a time and using 4-bit multiplier blocks as discussed above we can perform the multiplication.The outputs of 4x4 bit multipliers are added accordingly to obtained the final product.Here a total of three Ripple-Carry Adders are required, out of which two adders are of 12-bits and one adder is of 8-bits

Results

The proposed 8-bit Vedic multiplier uses the „Urdhva-Tiryak-Bhyam‟ binary sutra operated using the VHDL

language. The whole code is combined. Synthesis is done through

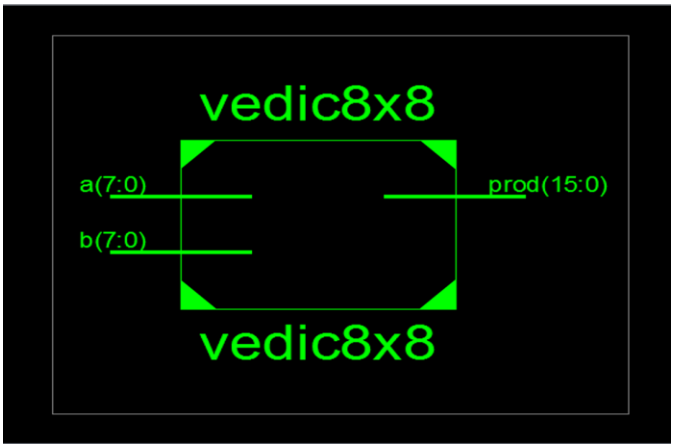

Fig-5.] RTL Schematic of 8x8 bit Vedic multiplier

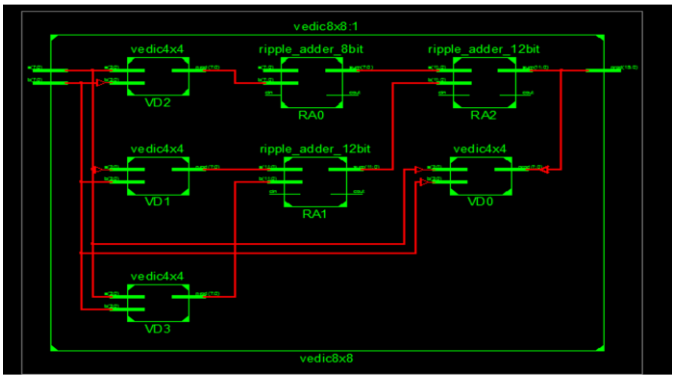

Fig-2.] diagram of 2x2 bit Vedic multiplier

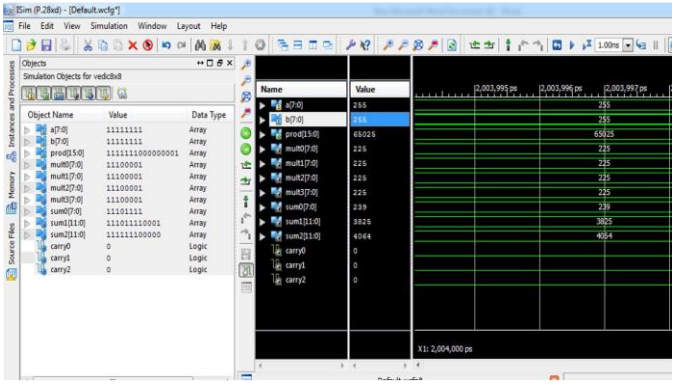

Fig-3.] Block diagram of 4x4 bit Vedic multiplier

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Timing Detail:
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All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 391 / 8
-------------------------------------------------------------------------
Delay:               16.114ns (Levels of Logic = 9)
  Source:            b<1> (PAD)
  Destination:       prod<7> (PAD)

  Data Path: b<1> to prod<7>
                                Gate     Net
    Cell:in->out      fanout    Delay    Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             9    0.715    1.250  b_1_IBUF (b_1_IBUF)
     LUT4:I0->O            1    0.479    0.740  RA0/FA1/HA1/Mxor_sum_Result_SW1 (N36)
     LUT4:I2->O            2    0.479    0.745  RA0/FA1/HA1/Mxor_sum_Result (sum0<1>)
     MUXF5:S->O            2    0.540    1.040  RA2/FA1/cout_f5 (RA2/carry2)
     LUT3:I0->O            2    0.479    0.804  RA2/FA3/HA1/Mxor_sum_Result11 (N11)
     LUT3:I2->O            4    0.479    1.074  RA2/FA3/cout1 (RA2/carry4)
     LUT4:I0->O            1    0.479    0.740  RA2/FA5/HA1/Mxor_sum_Result111 (RA2/FA5/HA1/Mxor_sum_Result11)
     LUT3:I2->O            1    0.479    0.681  RA2/FA5/HA1/Mxor_sum_Result20 (prod_7_OBUF)
     OBUF:I->O                  4.909          prod_7_OBUF (prod<7>)
    ----------------------------------------
    Total                      16.114ns (9.038ns logic, 7.076ns route)
                                        (56.1% logic, 43.9% route)

=========================================================================

Total REAL time to Xst completion: 6.00 secs
Total CPU time to Xst completion: 5.68 secs
```

Fig-4.] Block diagram of 8x8 bit Vedic multiplier

3. CONCLUSIONS

This paper shows the most effective method of multiplication using the Urdhva-Tiryak-Bhyam Sutra. It is a system of successive repetitive design that clearly demonstrates the calculation benefits offered by the Vedic method. The delay of the proposed 8x8 bit Vedic repetition method is 19ns from the Isim template. Vedic mathematical power can be tested to use high performance multiplier in VLSI applications

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