Design and Implementation of a High-Efficiency Seven-Level Inverter for Solar Power Generation Systems

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***Abstract*— This paper presents a novel solar power generation system that integrates a DC/DC power converter with a new seven-level inverter, offering enhanced efficiency and simplified design. The DC/DC power converter combines a boost converter and a transformer to produce two independent voltage sources. These are processed by a capacitor selection circuit and a full-bridge power converter in cascade to generate a seven-level AC voltage. The proposed inverter topology uses only six power electronic switches, with only one switch operating at high frequency at any given time, thereby minimizing switching losses and improving overall power conversion efficiency. The reduced switching harmonics also decrease filter inductor requirements, contributing to a compact and cost-effective design. A prototype system was developed and tested, demonstrating its ability to deliver sinusoidal output current synchronized with utility voltage, confirming its suitability for residential solar power applications. This system represents a significant advancement in the field of solar energy conversion, addressing key challenges of efficiency, cost, and reliability.**

Keywords

Seven-level inverter, DC/DC power converter, solar power generation, multilevel inverter, high-efficiency inverter, renewable energy, grid-connected inverter, switching loss reduction, photovoltaic systems.

I. INTRODUCTION

The extensive use of fossil fuels has led to increased greenhouse gas emissions and environmental concerns. Additionally, the finite nature of fossil fuel reserves ensures their future scarcity and rising costs. Solar energy, with its environmentally friendly characteristics and decreasing costs of photovoltaic (PV) technology, has become a promising alternative energy source. Small-capacity distributed power generation systems utilizing solar energy are expected to see widespread adoption in residential applications.

In grid-connected solar power generation systems, the power conversion interface plays a critical role. It converts the direct current (DC) power generated by solar cell arrays into alternating current (AC) power compatible with utility grids. Since solar cell arrays typically produce low output voltage, a DC/DC power converter is required to boost the voltage to match the DC bus voltage of the inverter. High power conversion efficiency is essential to minimize energy losses and ensure optimal utilization of the energy generated by solar panels.

Traditional inverters face challenges related to power losses, including conduction losses from active devices and switching losses proportional to the voltage and current changes during each switching operation. Additionally, filter inductors are used to process switching harmonics, which also contribute to power losses. To address these challenges, multilevel inverter technology has been developed to enhance power conversion efficiency and reduce switching stress and harmonics.

Conventional multilevel inverter topologies include diode-clamped, flying-capacitor, and cascade H-bridge types. While these designs offer improved performance, they have limitations. For example, diode-clamped and flying-capacitor inverters require complex capacitor voltage regulation, and the circuit complexity increases with the number of voltage levels. Cascade H-bridge inverters achieve higher voltage levels using asymmetric voltage technology, but they still require a significant number of power electronic switches.

Recently, novel multilevel inverter designs have been proposed to address these limitations. One such design is the seven-level grid-connected inverter, which uses six power electronic switches but involves three DC capacitors, complicating voltage balancing. Other designs incorporate modular approaches or multilevel DC-link inverters to overcome issues such as partial shading in series-connected PV modules.

This paper proposes a new solar power generation system featuring a DC/DC power converter and a simplified seven-level inverter. The DC/DC power converter integrates a boost converter and transformer to generate two independent voltage sources. The seven-level inverter, composed of a capacitor selection circuit and a full-bridge power converter in cascade, requires only six power electronic switches. This design reduces circuit complexity and ensures that only one switch operates at high frequency at any given time, minimizing switching losses and enhancing efficiency. The reduced switching harmonics also lower filter inductor requirements, contributing to a more compact and cost-effective system.

A prototype of the proposed system was developed and tested to validate its performance. The results demonstrate the ability of the system to generate a sinusoidal AC output current in phase with utility voltage, confirming its potential for residential solar power applications. This innovative approach offers a significant improvement in efficiency, reliability, and cost-effectiveness for solar energy conversion systems.

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II. CIRCUIT CONFIGURATION

Fig. 1 shows the configuration of the proposed solar power generation system. The proposed solar power generation system is composed of a solar cell array, a dc–dc power converter, and a new seven-level inverter. The solar cell array is connected to the dc–dc power converter, and the dc–dc power converter is a boost converter that incorporates a transformer with a turn ratio of 2:1. The dc–dc power converter converts the output power of the solar cell array into two independent voltage sources with multiple relationships, which are supplied to the seven-level inverter. This new seven-level inverter is composed of a capacitor selection circuit and a full-bridge power converter, connected in a cascade. The power electronic switches of capacitor selection circuit

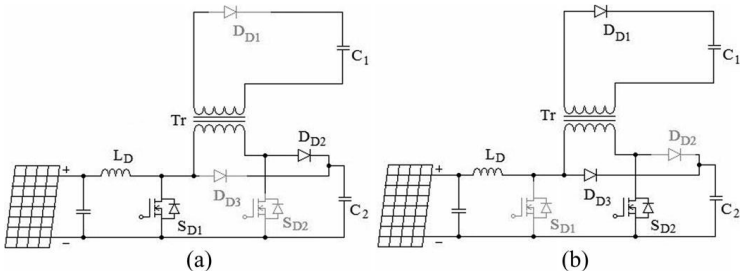


Fig.1

A. DC DC POWER CONVERTER

The DC–DC power converter, as shown in Fig. 1, integrates a boost converter and a current-fed forward converter. The boost converter consists of an inductor LD, a power electronic switch

SD1, and a diode DD3, which charges capacitor C2 of the seven-level inverter. The current-fed forward converter comprises inductor LD, switches SD1 and SD2, a transformer, and diodes DD1 and DD2, charging capacitor C1. Notably, LD and SD1 are shared between the two converters, simplifying the circuit design.

When SD1 is ON, the solar cell array supplies energy to inductor LD. When SD1 is OFF and SD2 is ON, as shown in Fig. 2, capacitors C1 and C2 are charged in parallel through the transformer. This configuration ensures that the voltage ratio of C1 and C2 matches the transformer's turn ratio (2:1), resulting in proportional voltage levels. The boost converter operates in continuous conduction mode (CCM), with C2 voltage given by:

$$Vc2 = Vs / (1 - D)$$

and C1 voltage by:

$$=Vc1 = Vs / [2(1 - D)].$$

The magnetizing inductance energy of the transformer is delivered to C2 through DD2 and SD1 when SD2 is OFF, improving efficiency

B.SEVEN-LEVEL INVERTER

As seen in Fig. 1, the seven-level inverter is composed of a capacitor selection circuit and a full-bridge power converter, which are connected in cascade. The operation of the seven level inverter can be divided into the positive half cycle and the negative half cycle of the utility. For ease of analysis, the power electronic switches and diodes are assumed to be ideal, while the voltages of both capacitors *C*1 and *C*2 in the capacitor selection circuit are constant and equal to *V*dc/3 and 2*V*dc/3, respectively. Since the output current of the solar power generation system will be controlled to be sinusoidal and in phase with the utility voltage, the output current of the seven-level inverter is also positive in the positive half cycle of the utility. The operation of the seven-level inverter in the positive half cycle of the utility can be further divided into four modes, as shown in Fig. 3.

Mode 1: The operation of mode 1 is shown in Fig. 3(a).
Both *SS*1 and *SS*2 of the capacitor selection circuit are OFF, so *C*1 is discharged through *D*1 and the output voltage of the capacitor selection circuit is *V*dc/3. *S*1 and *S*4 of the full-bridge power converter are ON. At this point, the output voltage of the seven-level inverter is directly equal to the output voltage of the capacitor selection circuit, which means the output voltage of the seven-level inverter is *V*dc/3.

Mode 2: The operation of mode 2 is shown in Fig. 3(b). In the capacitor selection circuit, *SS*1 is OFF and *SS*2 is ON, so *C*2 is discharged through *SS*2 and *D*2 and the output voltage of the capacitor selection circuit is 2*V*dc/3. *S*1 and *S*4 of the full-bridge power converter are ON. At this point, the output voltage of the seven-level inverter is 2*V*dc/3.

Mode 3: The operation of mode 3 is shown in Fig. 3(c). In the capacitor selection circuit, *SS*1 is ON. Since *D*2 has a reverse bias when *SS*1 is ON, the state of *SS*2 cannot affect the current flow. Therefore, *SS*2 may be ON or OFF, to avoiding switching of *SS*2. Both *C*1 and *C*2 are discharged in series and the output voltage of the capacitor selection circuit is *V*dc. *S*1 and *S*4 of the full-bridge power converter are ON. At this point, the output voltage of the seven-level inverter is *V*dc.

Mode 4: The operation of mode 4 is shown in Fig. 3(d). Both *SS*1 and *SS*2 of the capacitor selection circuit are OFF. The output voltage of the capacitor selection circuit is *V*dc/3. Only *S*4 of the full-bridge power converter is ON. Since the output current of the seven-level inverter is positive and passes through the filter inductor, it forces the anti parallel diode of *S*2 to be switched ON for continuous

conduction of the filter inductor current. At this point, the output voltage of the seven level inverter is zero. Therefore, in the positive half cycle, the output voltage of the seven-level inverter has four levels: *V*dc, 2*V*dc/3, *V*dc/3, and 0. In the negative half cycle, the output current of the seven-level inverter is negative. The operation of the seven-level inverter can also be further divided into four modes, as shown in Fig. 4. A comparison with Fig. 3 shows that the operation of the capacitor selection circuit in the negative half cycle is the same as that in the positive half cycle. The difference is that *S*2 and *S*3 of the full-bridge power converter are ON during modes 5, 6, and 7, and *S*2 is also ON during mode 8 of the negative half cycle. Accordingly, the output voltage of the capacitor selection circuit is inverted by the full-bridge power converter, so the output voltage of the seven-level inverter also has four levels: −*V*dc, −2*V*dc/3, −*V*dc/3, and 0. In summary, the output voltage of the seven-level inverter has the voltage levels: *V*dc, 2*V*dc/3, *V*dc/3, 0, −*V*dc/3, −2*V*dc/3, and −*V*dc.

The seven-level inverter is controlled by the current-mode control, and pulse-width modulation (PWM) is use to generate the control signals for the power electronic switches. The output voltage of the seven-level inverter must be switched in two levels, according to the utility voltage. One level of the output voltage is higher than the utility voltage in order to increase the filter inductor current, and the other level of the output this way, the output current of the seven-level voltage is lower than the utility voltage, in order to decrease the filter inductor current. In this way, the output current of the 7 level inverter can be controlled to trace a reference current. Accordingly, the output voltage of the seven-level inverter must be changed in accordance with the utility voltage.

In the positive half cycle, when the utility voltage is smaller than *V*dc/3, the seven-level inverter must be switched between modes 1 and 4 to output a voltage of *V*dc/3 or 0. Within this voltage range, *S*1 is switched in PWM. The duty ratio d of *S*1 can be represented as

$$d = vm/V\text{tri} \quad (3)$$

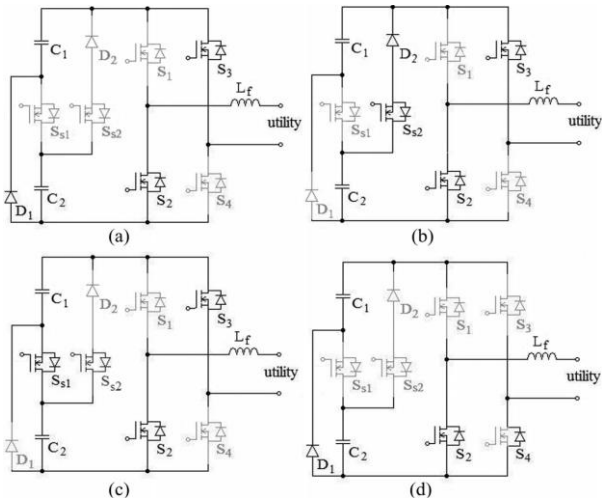


Fig. 4. Operation of the seven-level inverter in the negative half cycle:
(a) mode 5, (b) mode 6, (c) mode 7, and (d) mode 8.

where *vm* and *V*tri are the modulation signal and the amplitude of carrier signal in the PWM circuit, respectively. The output voltage of the seven-level inverter can be written as

$$vo = d \cdot V\text{dc}/3 = k\text{pwm}vm \quad (4)$$

where *k*pwm is the gain of inverter, which can be written as

$$k\text{pwm} = V\text{dc}/3V\text{tri} . \quad (5)$$

Fig. 5(a) shows the simplified model for the seven-level inverter when the utility voltage is smaller than *V*dc/3.

The seven-level inverter is switched between modes 2 and 1, in order to output a voltage of 2*V*dc/3 or *V*dc/3 when the utility voltage is in the range (*V*dc/3, 2*V*dc/3).Within this voltage range, *SS*2 is switched in PWM. The duty ratio of *SS*2 is

the same as (3). However, the output voltage of seven-level inverter can be written as

$$vo = d \cdot Vdc/3 + Vdc/3 = k\text{pwm}vm + Vdc/3. \quad (7)$$

Fig. 5(b) shows the simplified model for the seven-level inverter when the utility voltage is within this voltage range.

The seven-level inverter is switched between modes 3 and 2 in order to output a voltage of *V*dc or 2*V*dc/3, when the utility voltage is in the range (2*V*dc/3, *V*dc). Within this voltage range, *SS*1 is switched in PWM and *SS*2 remains in the ON state to avoid switching of *SS*2 . The duty ratio of *SS*1 is the same as (3). However, the output voltage of seven-level inverter can be written as

$$vo = d \cdot Vdc/3 + 2Vdc/3 = k\text{pwm}vm + 2Vdc/3. \quad (8)$$

Fig. 5(c) shows the simplified model for the seven-level inverter when the utility voltage is within this voltage range. The closed-loop transfer function can be derived as

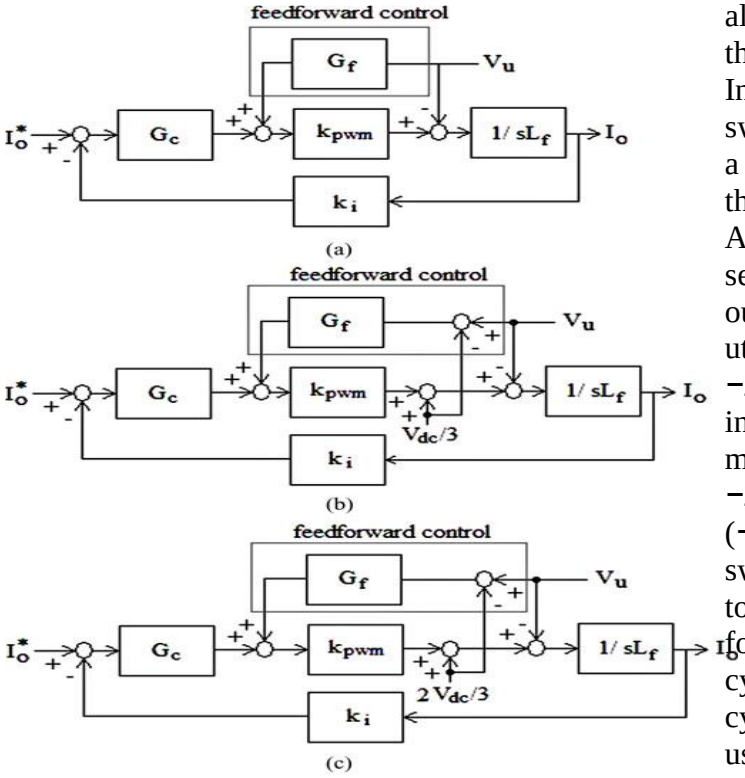


Fig. 5. Model of the seven-level inverter under different range of utility voltage,
(a) in the range of smaller than *V*dc /3, (b) in the range of (*V*dc /3, 2*V*dc /3),
(c) in the range of higher than 2*V*dc /3.

TABLE I
STATES OF POWER ELECTRONIC SWITCHES FOR A SEVEN-LEVEL INVERTER

	S_{S1}	S_{S2}	S_1	S_2	S_3	S_4
positive half cycle						
$\lvert v_u\rvert < V_{dc}/3$	off	off	PWM	off	off	on
$2V_{dc}/3 > \lvert v_u\rvert > V_{dc}/3$	off	PWM	on	off	off	on
$\lvert v_u\rvert > 2V_{dc}/3$	PWM	on	on	off	off	on
negative half cycle						
$\lvert v_u\rvert < V_{dc}/3$	off	off	off	on	PWM	off
$2V_{dc}/3 > \lvert v_u\rvert > V_{dc}/3$	off	PWM	off	on	on	off
$\lvert v_u\rvert > 2V_{dc}/3$	PWM	on	off	on	on	off

As seen in (6), (8), and (10), the second term is the disturbance. Hence, a feed forward control, which is also shown in Fig. 5, should be used to eliminate the disturbance, and the gain *Gf* should be 1/*k*pwm. In the negative half cycle, the seven-level inverter is switched between modes 5 and 8, in order to output a voltage of −*V*dc/3 or 0, when the absolute value of the utility voltage is smaller than *V*dc/3. Accordingly, *S*3 is switched in PWM. The sevenlevel inverter is switched in modes 6 and 5 to output a voltage of −2*V*dc/3 or −*V*dc/3 when the utility voltage is in the range (−*V*dc/3, −2*V*dc/3).Within this voltage range, *SS*2 is switched in PWM. The seven-level inverter is switched in modes 7 and 6 to output a voltage of −*V*dc or −2*V*dc/3, when the utility voltage is in the range (−2*V*dc/3, −*V*dc). At this voltage range, *SS*1 is switched in PWM and *SS*2 remains in the ON state to avoid switching of *SS*2 . The simplified model for the seven-level inverter in the negative half cycle is the similar to that for the positive half cycle. Since only six power electronic switches are used in the proposed seven-level inverter, the power

circuit is significantly simplified compared with a conventional seven-level inverter. The states of the power electronic switches of the seven-level inverter, as detailed previously, are summarized in Table I. It can be seen that only one power electronic switch is switched in PWM within each voltage range and the change in the output voltage of the seven-level inverter for each switching operation is *V*dc/3, so switching power loss is reduced. Figs. 3 and 4 show that only three semiconductor devices are conducting in series in modes 1, 3, 4, 5, 7, and 8 and four semiconductor devices are conducting in series in modes 2 and 6. This is superior to the conventional multi-level inverter topologies, in which at least four semiconductor devices are conducting in series. Therefore, the conduction loss of the proposed seven-level inverter is also reduced slightly. The drawback of the proposed seven-level inverter is that the voltage rating of the full-bridge converter is higher than that of conventional multilevel inverter topologies. The leakage current is an important parameter in a solar power generation system for transformer less operation. The leakage current is dependent on the parasitic capacitance and the negative terminal voltage of the solar cell array respect to ground [22], [23]. To reduce the leakage current, the filter inductor *Lf* should be replaced by a symmetric topology and the solar

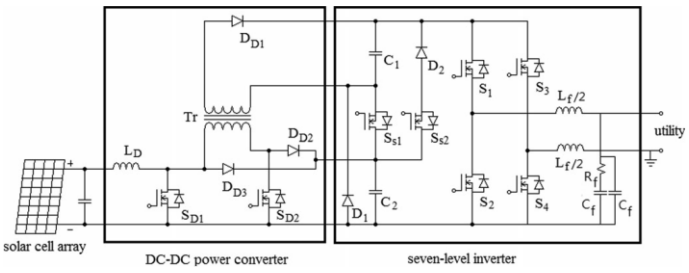


Fig. 6. Configuration of the proposed solar power generation system for suppressing the leakage current.

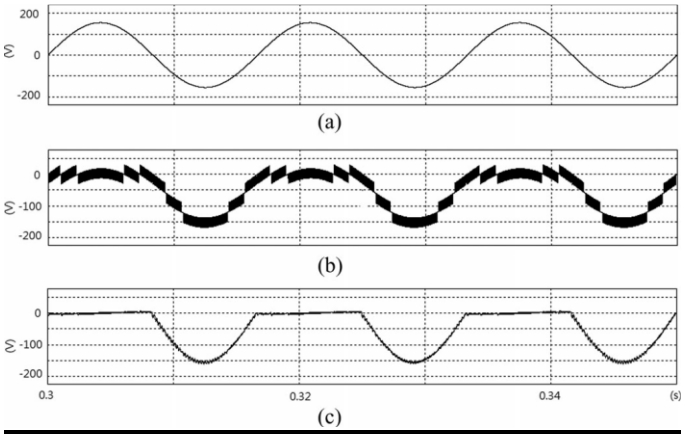


Fig. 7. Simulation results of the proposed solar power generation system:
(a) utility voltage, (b) negative terminal voltage for adding the symmetric filter inductor, and (c) negative terminal voltage for adding the symmetric filter inductor and the extra filter *Cf –Rf –Cf* .

power generation system is redrawn as Fig. 6. Fig. 7 shows the simulation results of the proposed solar power generation system. Fig. 7(b) is the negative terminal voltage of the solar cell array for the seven-level inverter with the symmetric filter inductor of 0.95 mH. As seen in Fig. 7(b), this voltage contains a high-frequency ripple. The peak-to-peak value of the high frequency ripple is about 30 V, which is much smaller than that of a full-bridge inverter with unipolar switching. This high-frequency ripple will result in a leakage current of solar cell array. If the leakage current of solar cell array is too high
to be accepted, an extra filter *Cf –Rf –Cf* , as shown in Fig. 6, can be added. Since the switching of *S*4 is synchronized with the utility voltage, the extra filter *Cf –Rf –Cf* is only added in the power-electronic leg (*S*1, *S*2). Fig. 7(c) shows the negative terminal voltage of a solar cell array for the seven-level inverter with the symmetric filter inductor and the extra filter *Cf –Rf –Cf* of 1 μF–25 Ω–1 μF. As seen in Fig. 7(c), the high-frequency ripple is attenuated effectively, so the leakage current can be further reduced.

V. CONTROL BLOCK

The proposed solar power generation system consists of a dc– dc power converter and a seven-level inverter. The seven-level inverter converts the dc power into high quality ac power and feeds it into the utility and regulates the voltages of capacitors *C*1 and *C*2. The dc–dc power converter supplies two independent voltage sources with multiple relationships and performs maximum power point tracking (MPPT) in order to extract the maximum output power from the solar cell array.

A. Seven-Level Inverter

Fig. 8(a) shows the control block diagram for the seven-level inverter. The control object of the seven-level inverter is its output current, which should be sinusoidal and in phase with the utility voltage. The utility voltage is detected by a voltage detector, and then sent to a phase-lock loop (PLL) circuit in order to generate a sinusoidal signal with unity amplitude. The voltage of capacitor *C*2 is detected and then compared with a setting voltage. The compared result is sent to a PI controller. Then, the outputs of the PLL circuit and the PI controller are sent to a multiplier to produce the reference signal, while the output current of the seven-level inverter is detected by a current detector. The reference signal and the detected output current are sent to absolute circuits and then sent to a subtractor, and the output of the subtractor is sent to a current controller. The detected utility voltage is also sent to an absolute circuit and then sent to a comparator circuit, where the absolute utility voltage is compared with both half and whole of the detected voltage of capacitor *C*2 , in order to determine the range of the operating voltage. The comparator circuit has three output signals, which correspond to the operation voltage ranges, (0, *V*dc/3), (*V*dc/3, 2*V*dc/3), and (2*V*dc/3, *V*dc).

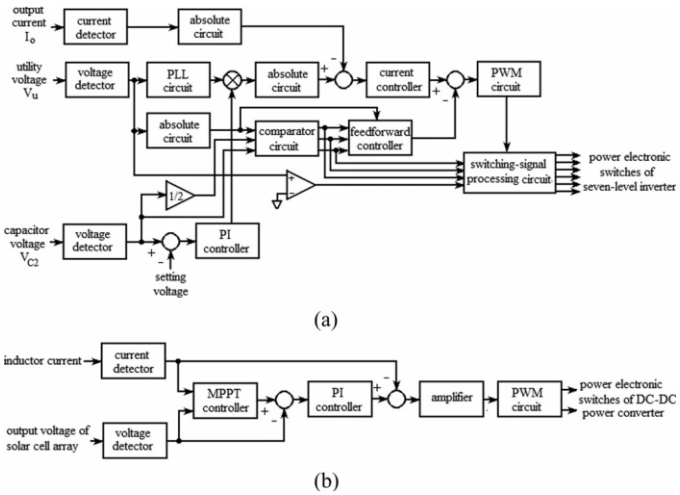


Fig. 8. Control block: (a) seven-level inverter and (b) dc–dc power converter.

The feed-forward control eliminates the disturbances of the utility voltage, *V*dc/3 and 2*V*dc/3, as shown in (6), (8), and (10). The absolute value of the utility voltage and the outputs of the compared circuit are sent to a feed-forward controller to generate the feed-forward signal. Then, the output of the current controller and the feed-forward signal are summed and sent to a PWM circuit to produce the PWM signal. The detected utility voltage is also compared with zero, in order to obtain a square signal that is synchronized with the utility voltage. Finally, the PWM signal, the square signal, and the outputs of the compared circuit are sent to the switching signal processing circuit to generate the control signals for the power electronic switches of the seven-level inverter, according to Table I. The current controller controls the output current of the seven level inverter, which is a sinusoidal signal of 60 Hz. Since the feed-forward control is used in the control circuit, the current controller can be a simple amplifier, which gives good tracking performance. As can be seen in (6), (8), and (10), the gain of the current controller determines the bandwidth and the steady state error. The gain of the current controller must be as large as possible in order to ensure a fast response and a low steady-state error. But the gain of the current controller is limited because the bandwidth of the

power converter is limited by the switching frequency.

B. DC–DC Power Converter

Fig. 8(b) shows the control block diagram for the dc–dc power converter. The input for the DC-DC power converter is the output of the solar cell array. A ripple voltage with a frequency that is double that of the utility appears in the voltages of *C*1 and *C*2, when the seven-level inverter feeds real power into the utility. The MPPT function is degraded if the output voltage of solar cell array contains a ripple voltage. Therefore, the ripple voltages in *C*1 and *C*2 must be blocked by the dc–dc power converter to provide improved MPPT. Accordingly, dual control loops, an outer voltage control loop and an inner current control loop, are used to control the dc–dc power converter. Since the output voltages of the DC-DC power converter comprises the voltages of *C*1 and *C*2, which are controlled by the seven-level inverter, the outer voltage control loop is used to regulate the output voltage of the solar cell array. The inner current control loop controls the inductor current so that it approaches a constant current and blocks the ripple voltages in *C*1 and *C*2. The perturbation and observation method is used to provide MPPT. The output voltage of the solar cell array and the inductor current are detected and sent to a MPPT controller to determine the desired output voltage for the solar cell array. Then the detected output voltage and the desired output voltage of the solar cell array are sent to a subtractor and the difference is sent to a PI controller. The output of the PI controller is the reference signal of the inner current control loop. The reference signal and the detected inductor current are sent to a subtractor and the difference is sent to an amplifier to complete the inner current control loop. The output of the amplifier is sent to the PWM circuit. The PWM circuit generates a set of complementary signals that control the power electronic switches of the dc–dc power converter.

VI. EXPERIMENTAL RESULTS

To verify the performance of the proposed solar power generation system, a prototype was developed with a controller based on the DSP chip TMS320F28035. The power rating of the prototype is 500 W, and the prototype was used for a single-phase utility with 110Vand 60 Hz. Table II shows the main parameters of the prototype. Figs. 9 and 10 show the experimental results for the seven level inverter when the output power of solar power generation system is 500 W. Fig. 9 shows the experimental results for the AC side of the seven-level inverter. Fig. 9(b) shows that the output voltage of the seven-level inverter has seven voltage levels. The output current of the seven-level inverter, shown in Fig. 9(c), is sinusoidal and in phase with the utility voltage, which means that the grid-connected power conversion interface feeds a pure real power to the utility. The total harmonic distortion (THD) of the output current of the seven-level inverter is 3.6%. Fig. 10 shows the experimental results for the dc side of the seven-level inverter. Fig. 10(b) and (c) show that the voltages of capacitors *C*2 and *C*1 of the capacitor selection circuit have multiple relationships and are maintained at 60 and 120 V, respectively. Fig. 10(d) shows that the output voltage of the capacitor selection circuit has three voltage levels (60, 120, and 180 V). Fig. 11 shows the experimental results for the dc–dc power converter. Fig. 11(b) and (c) shows that the ripple voltages in capacitors *C*1 and *C*2 of the capacitor selection circuit are evident. However, the ripple current in the inductor of the dc–dc power converter is less than 0.5 A when the average current of inductor is 8 A, as shown in Fig. 11(a). Therefore, the ripple voltages in *C*1 and *C*2 are blocked by the dc–dc power converter. Fig. 12 shows the output power scan for the solar cell array when the output voltage changes from 40 to 70 V. Fig. 13 shows the experimental results for the beginning of MPPT for the dc–dc converter. Fig. 13

shows that the output power of the solar cell array is almost constant when maximum power tracking is achieved and its value is very close to the maximum power shown in Fig. 12. Fig. 14 shows the experimental results for the power efficiency of the proposed solar power generation system. The solar cell array was replaced by a dc power supply to simplify the adjustment of output power in the experimental process. With higher step-up gain of the dc–dc power converter, there is lower power efficiency. Hence, the higher input voltage of solar power generation system will result in better power efficiency of the dc–dc power converter. Since a transformer is used in the dc–dc power converter of the proposed solar power generation system, this degrades the power efficiency of the proposed solar power generation system. However, the power transferred by the transformer is less than one third of the solar output power in the proposed dc–dc power converter, and the energy stored in the magnetizing inductance of the transformer is transferred forward to the output capacitor. Hence, the degradation of power efficiency caused by use of the transformer in the proposed solar power generation system is not serious.

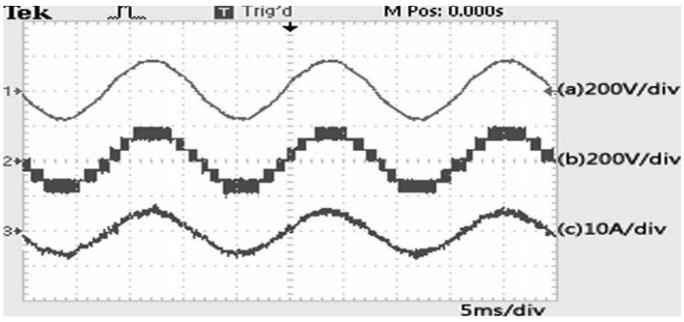


Fig. 9. Experimental results for the ac side of the seven-level inverter:

(a) utility voltage, (b) output voltage of seven-level inverter, and (c) output current of the seven-level inverter.

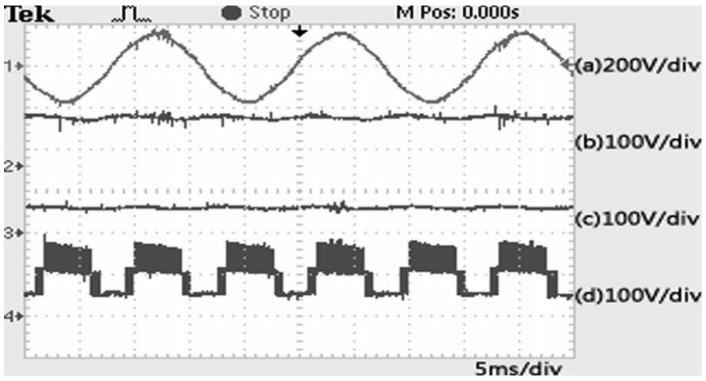


Fig. 10. Experimental results for the dc side of the seven-level inverter: (a) utility voltage, (b) voltage of capacitor C2, (c) voltage of capacitor C1, and (d) output voltage of the capacitor selection circuit.

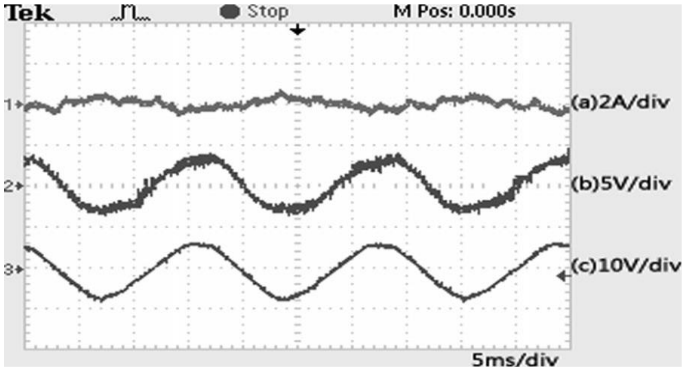


Fig. 11. Experimental results of the dc–dc power converter: (a) ripple current of inductor, (b) ripple voltage of capacitor C2, and (c) ripple voltage of capacitorC1

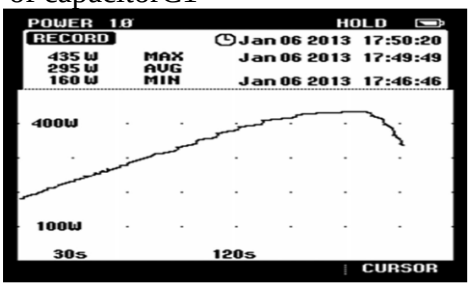


Fig. 12. Output power scan of the solar cell array.

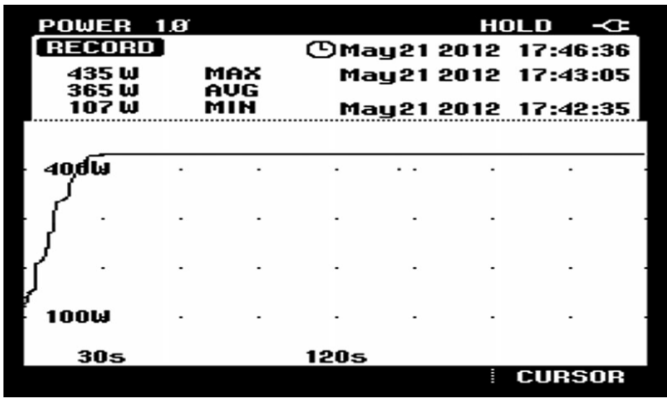
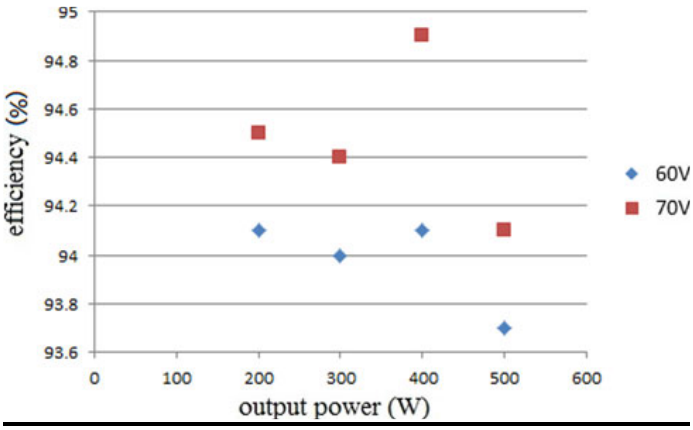


Fig. 13. Experimental results for the MPPT performance of the proposed solar power generation system

Fig. 14. Experimental results for the power efficiency of the proposed solar power generation system.



VII. CONCLUSION

This paper proposes a solar power generation system to convert the dc energy generated by a solar cell array into ac energy that is fed into the utility. The proposed solar power generation system is composed of a dc–dc power converter and a sevenlevel inverter. The seven-level inverter contains only six power electronic switches, which simplifies the circuit configuration. Furthermore, only one power electronic switch is switched at high frequency at any time to generate the seven-level output voltage. This reduces the switching power loss and improves the power efficiency. The voltages of the two dc capacitors in the proposed seven-level inverter are balanced automatically, so the control circuit is simplified. Experimental results show that the proposed solar power generation system generates a seven-level output voltage and outputs a sinusoidal current that is in phase with the utility voltage, yielding a power factor of unity. In addition, the proposed solar power generation system can effectively trace the maximum power of solar cell array.

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