

## Design And Implementation of A High-Speed Cost-Efficient Quantum Reversible Pipelined Carry Select Adder

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**Abstract:** Compared to classical computing implementations, reversible arithmetic adders offer a valuable platform for implementing quantum computation models in digital systems and specific applications, such as cryptography and natural language processing. Reversible logic efficiently prevents energy wastage through thermal dissipation. This study presents a comprehensive exploration introducing new carry-select adders (CSLA) based on quantum and reversible logic. Five reversible CSLA designs are proposed and compared, evaluating various criteria, including speed, quantum cost, and area, compared to previously published schemes. These comparative metrics are formulated for arbitrary n-bit size blocks. Each design type is described generically, capable of implementing carry-select adders of any size..

**Introduction:** one of the critical factors in designing VLSI circuits and digital systems is power consumption and energy dissipation. Energy dissipation increases due to many transistors in circuits, shrinking the feature size. In the early 1960s, Landauer introduced a novel power dissipation principle in digital circuits. He issued his theory about power dissipation based on information loss during computation in digital systems. From his perspective, designing digital and logical circuits based on conventional logic, also known as irreversible logic, leads to inevitable power dissipation. The motive is that digital circuits designed based on irreversible logic contain more input lines

### Fundamentals And Literature Review:

A logical gate is named a reversible gate if it fulfils two necessary conditions: first, it has N input lines and N output lines; in other words, an equal number of input and output signals must be met. Secondly, a one-to-one correspondence between its input and

output vectors must exist. Each input pattern maps to an individual output pattern in reversible logic gates. As a result, each input pattern value can be recovered through its corresponding output pattern value and vice versa. Many reversible gates in the literature have been proposed in low-power digital and quantum computational systems, some of whose block diagrams and equivalent quantum circuits are depicted in Figure 1. Peres Gate and F2G Gate with 4 and 2 quantum costs can implement AND, and XOR logical function, respectively; also, Fredkin and COG gate can work as 2:1 multiplexer having 5 and 4 quantum cost and 5 and 4 delays, respectively. HNG gate operates as a one-bit full adder with quantum cost and delay equal to. All the constituent logical gates used in the structure must be reversible to construct a reversible logic circuit.

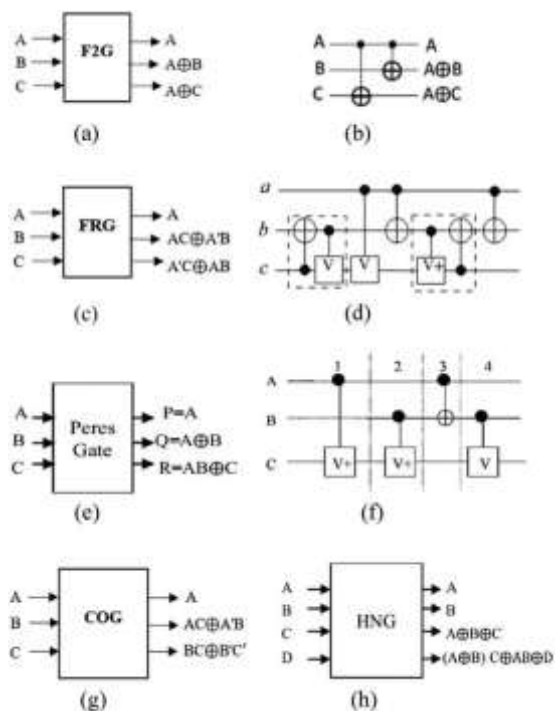


Fig 1. The clock diagram and quantum representation of basic reversible gates: (a) and (b) F2G gate, (c) and (d) Fredkin Gate, (e) and (f) Peres Gate, (g) COG Gate, and (h) HNG Gate.

- Minimum number of constant inputs
- Minimum number of garbage outputs
- Minimum delay
- Minimum quantum cost

**Proposed Method:** Five designs of reversible CSLA circuits are proposed in this section.

1. Conventional reversible carry select adder:

The diagram represents a Conventional Reversible Carry Select Adder (CRCSLA) designed using reversible logic gates, mainly HNG gate and COG gate. In this structure, the HNG gate performs the function of a reversible full adder by generating sum and carry outputs for given inputs A, B, and carry input. The first stage of the circuit takes inputs A0

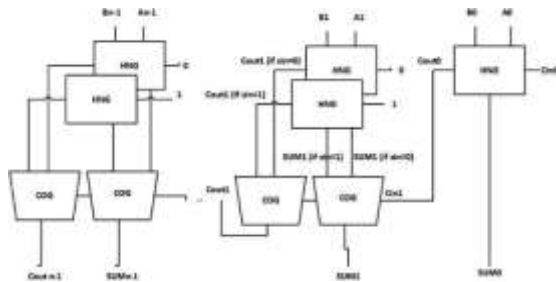


Fig1: Conventional reversible carry select adder

and B0, produces SUM0, and generates the first carry output Cout0. In the next stage, two HNG gates operate in parallel, one assuming carry input = 0 and the other assuming carry input = 1, producing two possible sum outputs. The COG gates then select the correct sum and carry based on the carry received from the previous stage. This same process continues for higher-order bits up to An-1 and Bn-1.

2. Conditional reversible CSLA:

The diagram illustrates an improved reversible carry select adder structure that uses HNG gate, Peres gate, F2G gate, and COG gate to perform binary addition efficiently. In the first stage, the HNG gate receives inputs A0 and B0 along with the carry input Cin0, producing the initial sum output SUM0 and carry output Cout0. In the next stages, the Peres gate generates intermediate outputs such as A⊕B, while the F2G gate duplicates signals and helps produce terms like A+B and AB required for carry generation. These outputs are then applied to the COG gates, which generate the required carry and

sum outputs for each bit position. The structure computes the next carry value (Cin1, Cin n-1) and corresponding sums (SUM1, SUM n-1) for higher-order bits. This design reduces the number of reversible gates compared with the conventional method by avoiding duplicate full-adder blocks for carry assumptions 0 and 1. As a result, the circuit

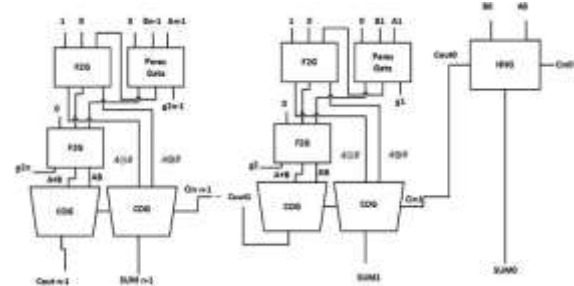


fig 2: Proposed reversible conditional CSLA with single-bit adder blocks

lowers quantum cost, garbage outputs, and delay while maintaining high-speed operation in reversible arithmetic systems.

3. Fixed size reversible RCA CSLA:

The diagram represents a square-root based reversible carry select adder architecture in which the n-bit addition is divided into two equal parts for faster computation. The right-side block contains an n/2-bit Ripple Carry Adder (RCA) implemented using the HNG gate, which processes the lower half inputs A[0:n/2-1] and B[0:n/2-1] along with the initial carry input Cin0. This block produces the lower half sum outputs SUM[0:n/2-1] and generates an intermediate carry output Cout n/2-1. The left-side section computes the upper half inputs A[n/2: n-1] and B[n/2: n-1] using two parallel n/2-bit RCA blocks, one assuming carry input 0 and the other assuming carry input 1.

Fig: Proposed Fixed-size RCA CSLA with n/2 bits adder blocks

These two parallel adders generate two possible sum outputs for the upper half. The COG gate blocks

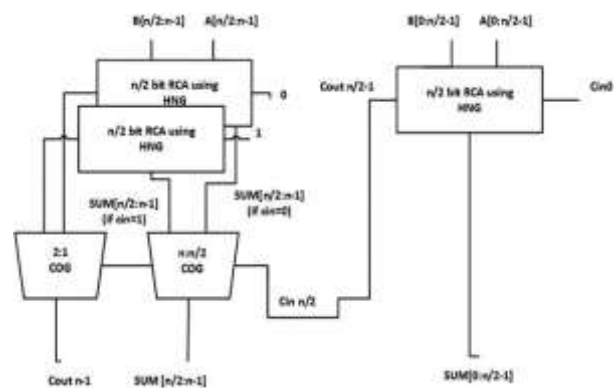


Fig 3: Proposed Fixed-size RCA CSLA with  $n/2$  bits adder blocks

then select the correct sum and final carry output based on the actual carry coming from the lower half section. The selected outputs become  $SUM[n/2:n-1]$  and  $Cout\ n-1$ . This arrangement improves speed because the upper-half sums are precomputed before the actual carry arrives, reducing propagation delay compared with a full ripple carry structure.

4. RCA square root reversible CSLA:

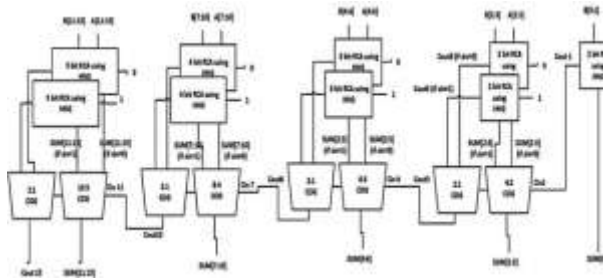


Fig 4: 16-bits reversible square root RCA CSLA with variable adder block sizes.

The diagram shows the RCA Square Root Reversible Carry Select Adder (SQRT CSLA), which is designed by dividing the adder into several groups of different bit sizes such as 2-bit, 3-bit, 4-bit, and 5-bit blocks. Each block uses Ripple Carry Adders (RCA) to calculate two possible outputs in parallel: one assuming carry input is 0 and another assuming carry input is 1. After the actual carry from the previous stage is known, a reversible multiplexer (MUX) selects the correct sum and carry output.

In this structure, the first block usually works as a simple RCA because no previous carry selection is required. The following blocks increase gradually in size, which forms the square root arrangement, helping to reduce delay compared to a regular carry select adder. The reversible design ensures that every input can be uniquely recovered from the outputs, which is important in low-power and quantum computing applications. This method improves speed because carry propagation is shortened, while also reducing hardware complexity compared with conventional reversible CSLA.

5. QBEC Square Root reversible CSLA: The diagram represents the QBEC Square Root

Reversible Carry Select Adder (CSLA), where QBEC (Quantum Binary Excess-1 Converter) is used instead of one of the duplicate ripple carry adders to reduce hardware cost. In each block, a Ripple Carry Adder (RCA) first computes the sum assuming carry input is 0, and the QBEC circuit generates the corresponding output for carry input 1

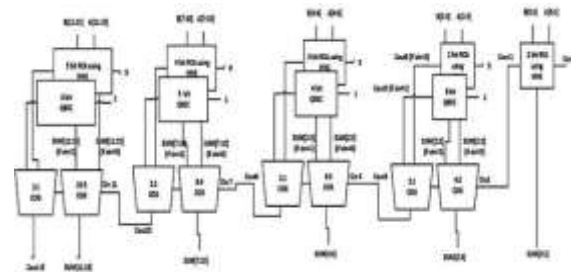


Fig.5:16-bit reversible QBEC square root CSLA with variable adder block size by adding one to the previous result. This removes the need for a second RCA and therefore reduces area, delay, and quantum cost.

Fig:16-bit reversible QBEC square root CSLA with variable adder block size

The structure follows the square root arrangement, where bit groups increase gradually such as 2-bit, 3-bit, 4-bit, and 5-bit sections. Each section uses a 2:1 reversible multiplexer or control gate (COG) to choose the correct output depending on the carry generated from the previous stage. The first block begins with a small RCA, and later blocks combine RCA and QBEC circuits to speed up carry selection. Because QBEC replaces one full RCA in each stage, this design is more efficient than RCA Square Root Reversible CSLA. It provides lower delay, reduced gate count, fewer garbage outputs, and better quantum efficiency, which makes it highly suitable for reversible computing and quantum arithmetic circuits.

Results And Discussions:

The results of “Design and Implementation of a High-Speed Cost-Efficient Quantum Reversible Pipelined Carry Select Adder” show that the proposed pipelined reversible CSLA improves arithmetic performance by reducing delay, quantum cost, and hardware complexity compared with earlier reversible adder designs. In the proposed architecture, pipelining divides the addition process into stages, so multiple operations can be processed simultaneously, which increases speed and shortens the critical path.

The design mainly uses optimized reversible gates such as HNG gate, Peres gate, and control selection blocks to minimize redundant computations. Because of this, the circuit produces fewer garbage

outputs and requires fewer constant inputs, which are important performance measures in reversible computing.

Compared with conventional reversible CSLA structures such as RCA-based square root CSLA and QBEC-based square root CSLA, the pipelined version achieves better throughput because each stage works independently and the carry propagation delay is reduced. The paper reports that the proposed method gives a better balance between speed and cost efficiency, making it suitable for quantum arithmetic units, reversible processors, and low-

Fig 7 : Power utilization

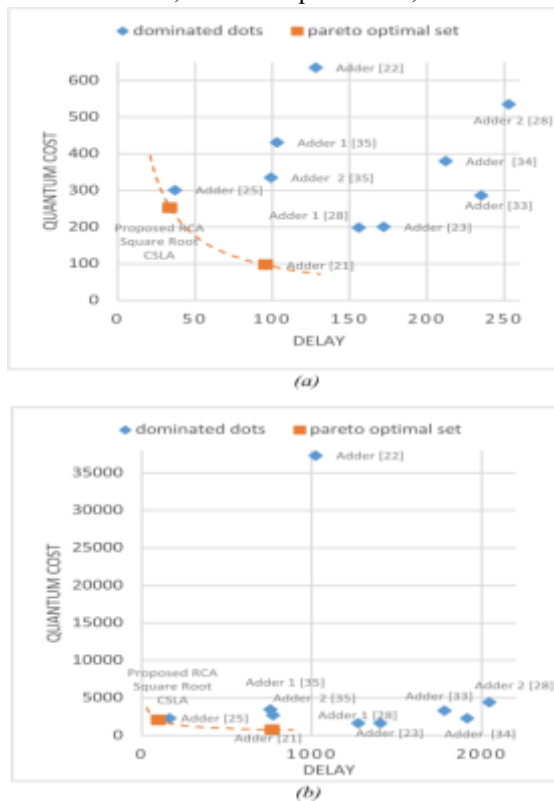


Fig 6 : Area utilization

Name	Slice LUTs (134600)	Slice Registers (269200)	Bonded IOB (400)	BUFGCTRL (32)
Extension	16	49	52	1



**CONCLUSION:** This study proposes and implements five new CSLA circuits in reversible logic. This study aims to achieve a very high-speed optimization in the addition operation. To do so, we proposed a reversible and quantum adder structure that can balance the trade-off between different criteria and increasing speed. Furthermore, a reversible quantum binary to excess one circuit has been proposed, ultimately a novel structure in reversible logic. The delay and quantum cost of all five proposed approaches are formalized, compared to each other and their existing counterparts. Comparative results show that the optimized scheme for designing a cost and delay-efficient reversible and quantum CSLA structure is multi-bit variable-sized carry select addition stages, which can realize the combination of RCA blocks and square root approach. The proposed high-speed quantum reversible adder structure can develop large-scale nanotechnology and massive qubit computational quantum systems.

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