# Design and Implementation of Energy Efficient Compact Approximate Multiplier for Error-Resilient Applications

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***Abstract:*** This paper aims to improve system efficiency using approximate computing by introducing optimized 4:2 compressor designs based on 8 and 20 transistors. These compressors, implemented using CMOS technology, apply constant and conditional approximation strategies to reduce computational errors without relying on error correction mechanisms. The 20-transistor version offers better accuracy with a minor increase in hardware area. Overall, the proposed multiplier architecture achieves up to 50% area savings and a 93% enhancement in the power-delay product when compared to traditional exact multipliers.
**Keywords:** Approximate computing, Compressor, Multiplier, Image Multiplication, Partial Products.

## I. INTRODUCTION

This work builds upon previous research [1] by presenting improved 8-transistor and 20-transistor approximate 4:2 compressors based on majority logic (ML) to enhance the efficiency of arithmetic circuits. Designed specifically for use in approximate multipliers, these compressors aim to minimize power consumption and hardware complexity while maintaining acceptable accuracy. Compared to the conventional 12-transistor design, the 8-transistor compressor reduces circuit overhead, while the 20-transistor version provides improved precision. The proposed architecture simplifies the multiplier structure by significantly cutting down the number of partial products and exact compressors—eliminating 15 AND gates from the partial product reduction tree (PPRT) and employing just one exact compressor. This leads to a 49% area reduction and a 93% drop in energy consumption relative to standard exact multipliers. The performance of these compressors is also assessed in image multiplication tasks, highlighting their applicability to error-tolerant systems. A comprehensive comparison with existing techniques illustrates the trade-offs between area, power efficiency, and accuracy, confirming the practicality of the proposed approach for energy-efficient computing.

## II. PROPOSEDAPPROXIMATECOMPRESSORS

This paper introduces 8-transistor and 20-transistor approximate 4:2 compressors utilizing majority logic (ML) to enhance the efficiency of arithmetic circuits. Majority logic, known for its fault-tolerant characteristics, allows for a lower gate count while maintaining acceptable accuracy. The proposed designs are intended to optimize the partial product reduction stage in multiplier circuits, leading to decreased complexity and power usage. The 8-transistor variant focuses on minimizing hardware resources, whereas the 20-transistor version offers improved computational accuracy. By eliminating 15 AND gates from the partial product reduction tree (PPRT) and relying on just one exact compressor, the architecture achieves a 49% area reduction and a 93% decrease in energy usage compared to conventional exact multipliers. The compressors' effectiveness is demonstrated through image multiplication tasks, indicating their potential for error-resilient applications. A detailed comparative analysis emphasizes the balance between accuracy, power efficiency, and area, making these designs well-suited for low-power, high-performance computing environments.

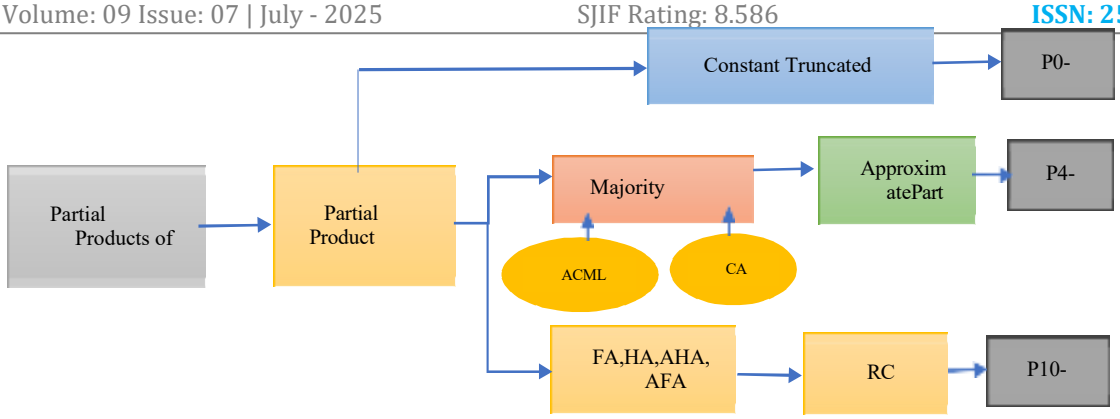


Fig.1.Proposed design flow of 8-bit multiplier

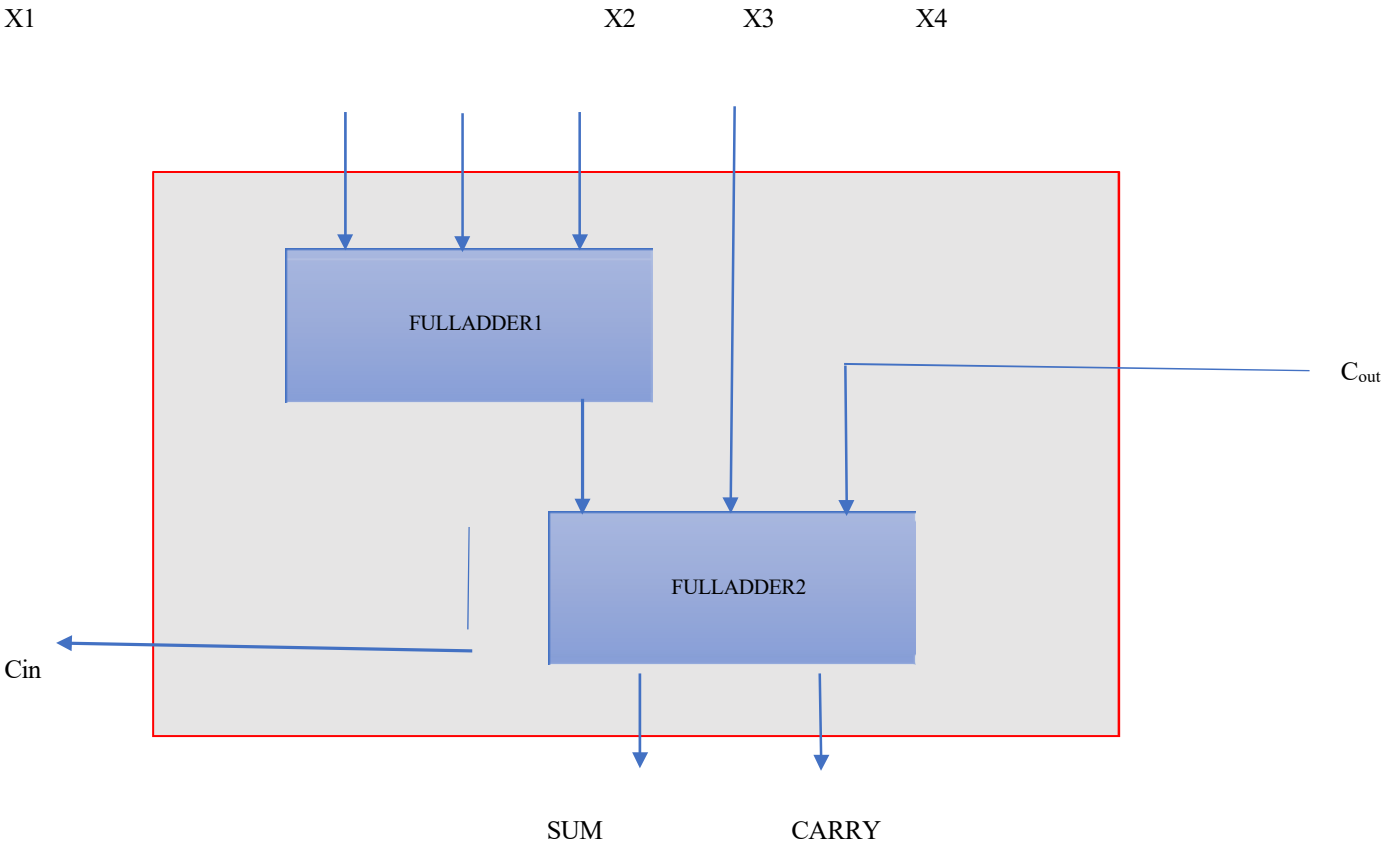


Fig.2.Proposed Exact Compressor

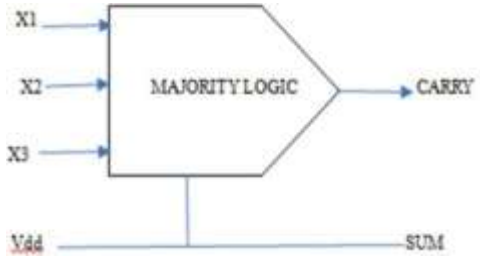


Fig.3.Proposed ACMLC

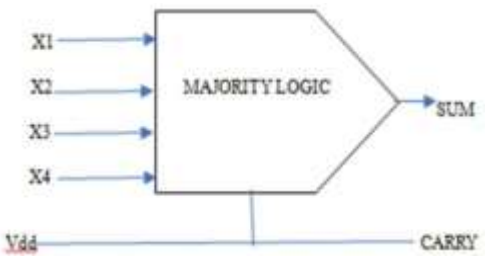


Fig.4 Proposed CAC

| X1 | X2 | X3 | SUM | CARRY |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Table1. Truth table of ACMLC

| X1 | X2 | X3 | X4 | SUM | CARRY |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 |

Table2. Truth table of CAC

### *A. 4:2.Approximate Condition based ML-Compressor and Compensator Approximate Compressor*

This work presents two innovative approximate compressor designs—namely, the Approximate Condition-Based Majority Logic Compressor (ACMLC) and the Compensator Approximate Compressor (CAC)—developed to improve the performance of arithmetic circuits. These architectures are extensions of majority logic (ML) compressors, which rely on simplified logic operations to enhance speed, minimize power usage, and reduce hardware complexity.

The ACMLC advances traditional ML compressor designs by implementing a two-stage approximation method. Unlike earlier ML-based approaches that disregard one of the inputs, ACMLC enhances the carry logic to reduce the incidence of negative errors while preserving structural simplicity. By adjusting the conditions for carry generation, ACMLC achieves a more balanced error profile, producing only three negative errors compared to four in previous models. The resulting sum and carry expressions for ACMLC provide improved accuracy with minimal added complexity.

$$Carry_{ACMLC}=(X1\cdot X3)+X2$$

$$Sum_{ACMLC} = V_{DD}$$

To enhance accuracy beyond what ACMLC offers, the Compensator Approximate Compressor (CAC) is proposed as a refinement

mechanism within ACMLC-based circuit designs. CAC fine-tunes both the carry generation and sum computation logic to reduce the overall error distance while preserving high-speed operation and efficiency. It introduces a more balanced error profile, producing only seven total errors—all with an error distance of one—and just a single negative error. This represents a notable improvement over earlier majority logic-based compressor designs. The carry and sum output expressions for CAC are defined as follows: $Carry_{CAC}=VDD$

$$Sum_{CAC}=(X1\cdot X2).(X3+X4)+(X3\cdot X4)$$

The designed multiplier architecture incorporates ACMLC and CAC compressors to enhance the efficiency of the partial product reduction tree (PPRT), leading to the removal of 15 AND gates and the use of only one exact compressor. This optimization achieves a 49% reduction in chip area and a 93% decrease in energy usage when compared to conventional exact multiplier designs. Furthermore, the absence of an error recovery module (ERM) contributes to a more streamlined and simplified circuit design.

A detailed comparison with current state-of-the-art compressor architectures underscores the distinct balance offered by the proposed designs in terms of accuracy, power efficiency, and area savings. In image multiplication tasks, the proposed compressors deliver improved performance, underlining their effectiveness in applications that can tolerate computational errors. These advancements support the development of compact, high-speed, and energy-efficient arithmetic hardware suitable for next-generation computing systems.

### *B. Approximate8-Bit Multiplier*

This paper introduces a highly efficient approximate multiplier architecture that incorporates two newly developed compressor designs: the Approximate Condition-Based Majority Logic Compressor (ACMLC) and the Compensator Approximate Compressor (CAC). These architectures build upon the majority logic (ML) concept, aiming to reduce power usage and hardware complexity without compromising accuracy.

The proposed multiplier is structured into three main components: truncation, approximation, and exact computation, which together optimize the partial product reduction tree (PPRT). Truncation is applied to at least four least significant bit (LSB) columns to reduce logic gates while maintaining acceptable precision. Unlike standard truncation approaches, a fixed-value assignment method (referenced in [13]) is employed, setting the four rightmost LSBs to a constant pattern (p0p1p2p3 = 0110), thereby eliminating ten AND gates in the initial stage.

The approximation block integrates five half adders using the ACMLC design along with a single exact full adder. The ACMLC-based 3-input compressor effectively removes one partial product per stage, cutting down an additional five AND gates. Moreover, eight unused AND gates from the first stage are reallocated to build a chain of compressors in the second stage, further optimizing area usage.In the final stage, the CAC compressor is used in the last column to propagate a carry value of 1 to the exact computation section, which simplifies the design of the exact compressor. Only one exact compressor is used across the multiplier, operating with a fixed carry-in of 1 (Cin = 1), enhancing precision while retaining energy efficiency.

Through the integration of ACMLC and CAC compressors, the multiplier achieves up to 49% area reduction and 93% lower energy consumption compared to a conventional exact multiplier. This hybrid approach of approximation and exact logic eliminates the need for an error recovery module (ERM), simplifying the design further. Comparative evaluation against leading compressor architectures demonstrates superior performance in terms of power savings, area efficiency, and computational accuracy. These characteristics make the proposed design highly suitable for error-tolerant applications like image processing, where approximate computing offers tangible performance benefits.

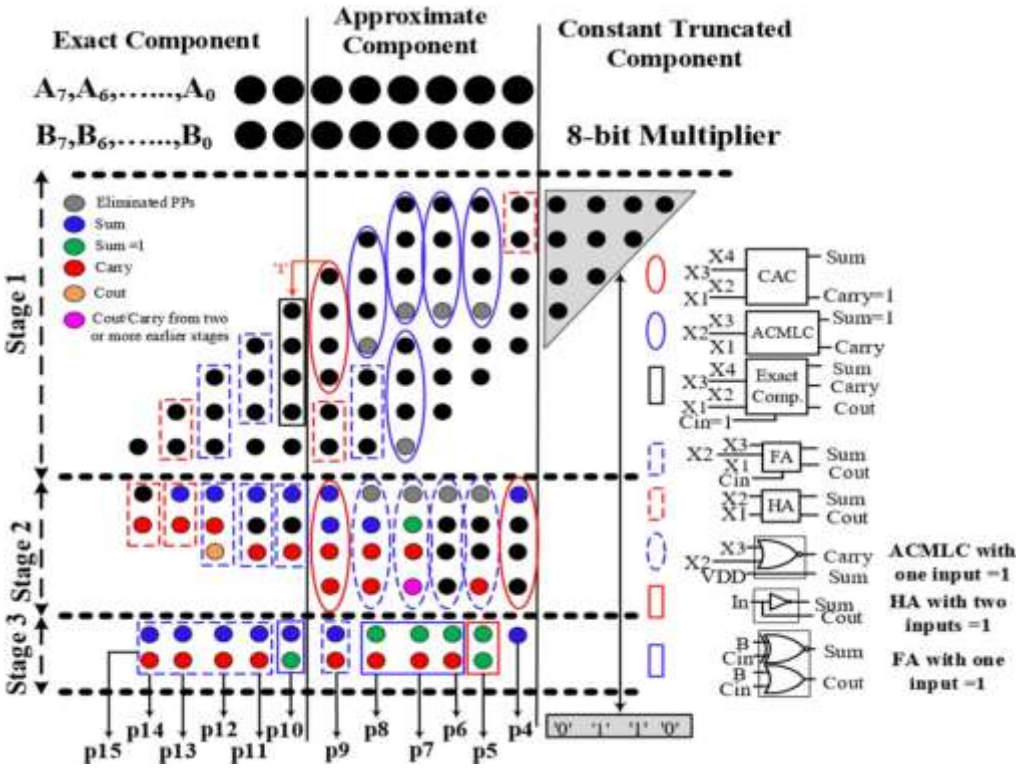


Fig.5.Approximate 8-bit multiplier [8]

This work presents a high-performance approximate multiplier that employs two innovative compressor architectures: the Approximate Condition-Based Majority Logic Compressor (ACMLC) and the Compensator Approximate Compressor (CAC). These architectures refine majority logic (ML) compressor designs to lower circuit complexity and energy usage while preserving a high level of computational accuracy.

The proposed multiplier consists of three key stages:

*1)* ***Stage1- Partial Product Reduction***

- Incorporates five half adders (HAs) based on the ACMLC architecture along with a single exact full adder (FA).
- A 3-input ACMLC compressor eliminates one partial product per stage, leading to the removal of five AND gates from each column.
- Eight unused AND gates from the first stage are reused in the second stage for compression, contributing to reduced circuit area.
- Truncation strategy: Rather than conventional truncation, a fixed-value assignment sets the four least significant bits (LSBs) to p0p1p2p3 = 0110, allowing the elimination of ten more AND gates.

*2)* ***Stage2-EnhancedCompressionUsing CAC***

- CAC compressors are used in the first and last columns of Stage 2 to enhance compression accuracy.
- An additional four ACMLC compressors are implemented, with input X4 omitted to further simplify the hardware.
- The total number of AND gates needed for an 8-bit multiplier drops from 64 to 49, contributing to area and power savings.
- To ensure precision, two exact half adders (HAs) and three exact full adders (FAs) are integrated.
- The carry output generated by the CAC in Stage 2 is propagated to the final computation stage.

*C.* ***Final Results***

- By combining ACMLC and CAC, the proposed multiplier achieves:
- 49% area reduction vs. Exact multipliers.
- 93% lower energy consumption.
- 12.6% smaller transistor count vs.ML-based multipliers.
- Total transistors: 786(compared to 900 in ML-basedand1530inexactmultipliers).

## III. RESULTS

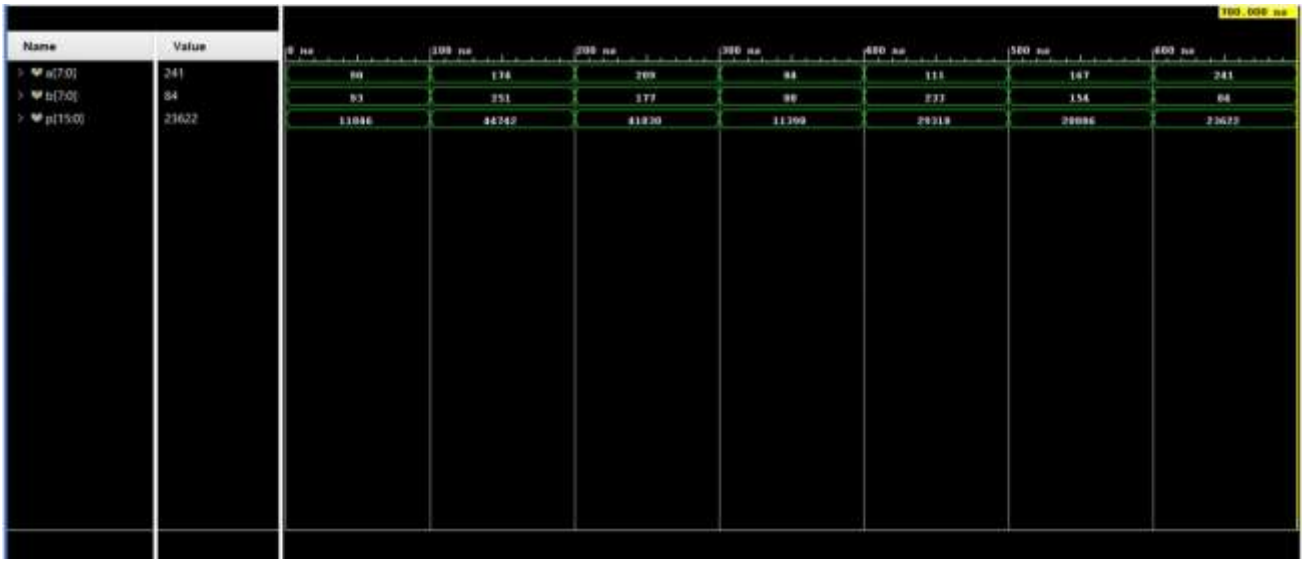


Fig.6a.Multiplication Output

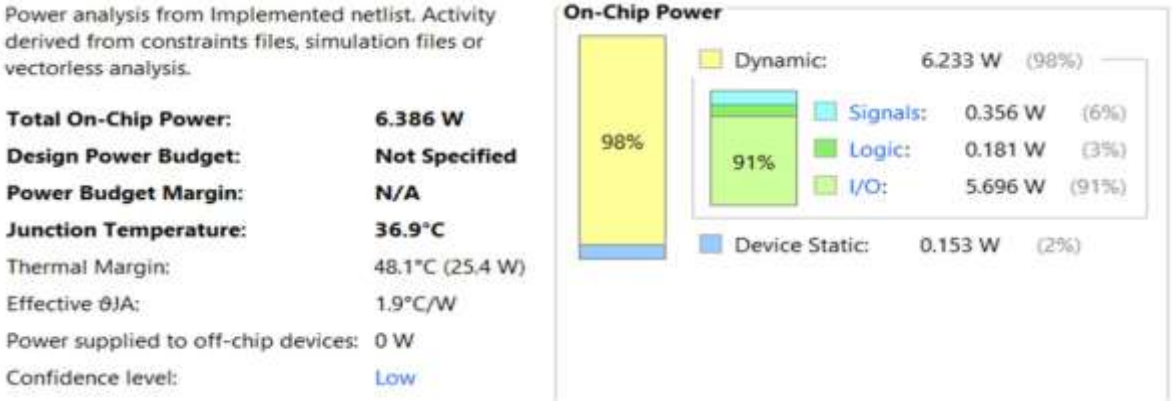


Fig.6b.Power Output

| Name | Slice LUTs (134600) | Slice (33650) | LUT as Logic (134600) | Bonded IOB (400) |
|---|---|---|---|---|
| proposed_ACMLC_and_CAC | 31 | 10 | 31 | 32 |

Fig.6c.LUT Count Output

| Name | Slack | Levels | Routes | High Fanout | From | To | Total Delay | Logic Delay | Net Delay | Requirement | Source Clock |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Path 1 | ∞ | 6 | 5 | 12 | a[6] | p[14] | 9.262 | 3.914 | 5.348 | ∞ | input port clock |
| Path 2 | ∞ | 6 | 5 | 12 | a[6] | p[15] | 9.260 | 3.918 | 5.341 | ∞ | input port clock |
| Path 3 | ∞ | 6 | 5 | 12 | a[6] | p[13] | 8.810 | 3.917 | 4.893 | ∞ | input port clock |
| Path 4 | ∞ | 5 | 4 | 12 | a[6] | p[11] | 8.593 | 3.800 | 4.793 | ∞ | input port clock |
| Path 5 | ∞ | 5 | 4 | 12 | a[6] | p[12] | 8.329 | 3.788 | 4.541 | ∞ | input port clock |
| Path 6 | ∞ | 5 | 4 | 11 | a[5] | p[9] | 7.596 | 3.600 | 3.996 | ∞ | input port clock |
| Path 7 | ∞ | 4 | 3 | 12 | a[6] | p[10] | 6.948 | 3.507 | 3.441 | ∞ | input port clock |
| Path 8 | ∞ | 4 | 3 | 7 | a[3] | p[4] | 6.942 | 3.667 | 3.275 | ∞ | input port clock |
| Path 9 | ∞ | 3 | 2 | 5 | a[1] | p[6] | 6.687 | 3.348 | 3.339 | ∞ | input port clock |
| Path 10 | ∞ | 4 | 3 | 7 | a[3] | p[7] | 6.603 | 3.468 | 3.135 | ∞ | input port clock |

Fig.6d.Time Delay Output

The ACMLC-based multiplier integrated with CAC demonstrates notable improvements in terms of power efficiency, area reduction, and computational accuracy. Simulation results confirm the correctness of the multiplier's output, validating its operational functionality. Power evaluation indicates a total on-chip power usage of 6.386 W, with dynamic power contributing to 98% and a junction temperature measured at 36.9°C. The architecture is hardware-efficient, requiring only 31 LUTs, 10 slices, and 32 bonded IOBs, reflecting minimal resource consumption. Timing analysis reveals a maximum delay of 9.262 ns, with the logic delay accounting for approximately 3.914 ns, showing a well-balanced compromise between processing speed and design complexity. The use of ACMLC compressors along with CAC helps eliminate redundant AND gates, resulting in a 49% reduction in transistor count compared to conventional exact multipliers. This architectural optimization significantly reduces both area and power consumption while ensuring accurate computation. In summary, the proposed multiplier offers a strong balance of performance, efficiency, and hardware simplicity, positioning it as a viable alternative to both conventional and previously existing ML-based multiplier designs.

## IV. CONCLUSION

This paper presents an 8-transistor Approximate Condition-Based Majority Logic Compressor (ACMLC), a 20-transistor Compensator Approximate Compressor (CAC), and an approximate 8-bit multiplier tailored for efficient and accurate image multiplication. The ACMLC offers a compact design with low power requirements, albeit with a comparatively higher error rate. To mitigate negative errors, the CAC is introduced, which results in only seven total errors—just one of which is negative. An approximate multiplier architecture is developed by integrating both ACMLC and CAC, leveraging their specific advantages. Compared to an exact multiplier, the proposed design achieves a 50% reduction in area and a 93% decrease in power consumption. Performance evaluations show that the proposed multiplier outperforms existing approximate designs in most key metrics. Pareto analysis indicates that, despite a modest compromise in accuracy, the ML-based architectures offer strong potential for energy-efficient and low-power applications.

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