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Design and Implementation of High Speed Hybrid Full Adder Using 16nm Technology Through Mentor Graphics

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***Abstract*—Using Pass Transistors (PTs), Transmission Gates (TGs), and Conventional Complementary Metal Oxide Semiconductor (CCMOS) logic, a new hybrid full adder architecture is given. The Mentor Graphics toolset has been used to analyse the circuit's performance. Twenty current FA circuits have been examined using the performance parameters for comparative analysis. In order to verify the scalability of the proposed FA, word lengths up to 64 bits have been included. Only the proposed FA and five of the current designs can function at expanded to 64 bits without using a buffer in between phases. The suggested design exhibits noteworthy performance in power consumption and delay, which accounted for low power delay product, according to simulation findings.According to the simulation findings, the suggested hybrid FA circuit is a compelling option for the data route design of contemporary high-speed Central Processing Units.**

Keywords: Hybrid Adder, Full Adder, Transmission Gate, Pass Transistor.

I. INTRODUCTION

The amount of research being done on low-power design of microelectronic circuits has dramatically increased due to the fast expansion of transistor scaling. Microelectronic circuits with high performance designs are in high demand as a result [1].

Modern applications such as image and video processing, digital signal processing (DSP) chips, microprocessors, and many others call for large-scale arithmetic operations [2]. The addition operation, one of the most basic in mathematics, is often and extensively employed in contemporary computing applications. Since it serves as the primary building block for creating large word-length adders, a 1-bit Full Adder (FA) is regarded as the core of binary addition [3–4]. Therefore, improving FA performance is essential for improving the performance of the microprocessors' Arithmetic and Logic Unit (ALU). This study suggests a novel hybrid FA that makes use of PTs, TGs, and static CMOS logic. With the use of Mentor Graphics tools, the FA was implemented in 16 nm technology. A comparison of the proposed design's performance characteristics with 20 already-existing FA devices with supply voltages ranging from 0.4 V to 1.2 V was done in order to assess the design's dependability. In order to verify the FAs' performance characteristics in large-scale circuits, they have also been expanded to wide word length adders. In comparison to the current FAs, the suggested FA demonstrated exceptional performance in both single cell and extended form.

II. RELATED WORK

Single logic style is used for FA implementation in Complementary Pass Transistor Logic (CPL) based FA [5], 12 Transistor (12-T) FA [6], and Conventional CMOS (C-CMOS) logic based FA [7]. CPL logic needs extra buffers to restore the signal to supply voltage level because of voltage deterioration. Voltage deterioration is an issue unrelated to C-CMOS FA. Large input impedance, however, is a significant issue with C-CMOS FA.

Today's researchers frequently employ a hybrid design strategy that makes use of the advantages of many logic models inside a single FA cell. TGs are used in the design of TG Adders (TGA) in [8], [9], and Transmission Function Adders (TFA) in [10]. Although TGA and TFA FA do not experience voltage deterioration, their low capability is a significant issue.

Multiple logic style is also used for FA implementation in cells with 24 transistors (24-T) [11], 14 transistors (14-T) [12], and 10 transistors (10-T) [13]. Instead of cascading two distinct 2 input XOR gates, the 24-T FA employs a 3 input XOR gate to calculate the total. In 14-T and 10-T FA, input bits are initially passed into an XOR gate. The output of the XOR gate is used to create the final output, acting as an intermediary node. Less surface area is caused by the 14-T and 10-T FAs' extremely low transistor counts. In [14], Hybrid Pass Static CMOS (HPSC) FA generates XOR and XNOR signals in intermediary nodes using Pass Transistor Logic (PTL). C-CMOS logic on the output side generates full-swing outputs. The number of transistors and capacitance increase with the use of CCMOS logic, though.

The AND-OR and XOR-XNOR signals produced by the Double Pass transistor logic (DPL) and Swing Restored CPL (SRCPL) Hybrid FAs described in [15] are used to compute output carry and the sum output. The choose bit of TG-based

multiplexers (MUX) uses input carry to create outputs from intermediate AND-OR and XOR-XNOR nodes. The hybrid FA in [16] uses inverter in the output side of the adder and utilized CPL and TG logic in the input side. The idea of using C-CMOS logic-based inverter in output side is to provide good driving capacity. In [17–21], more Hybrid FAs are reported. Three FA designs (referred to as GDI D1, GDI D2, and GDI D2 in this study) have been disclosed in [22] based on the Gate Diffusion Input (GDI) approach. The poor output signal of GDI adders is a significant issue.

III. Proposed Full Adder Design Approach

Design approach of the proposed FA is shown in Fig. 1. The design of the proposed FA is divided into four major modules: two modules for carry generation and the other two for sum. Schematic of the proposed design is represented by Fig. 2. The design methods and detailed description of the modules are provided in the following sub-sections.

A. Carry Generation

From the truth table of a FA, it can be observed that

If, $C_{in} = 0$ then C_{out} = AND function and
if, $C_{in} = 1$ then C_{out} = OR function

Therefore, the proposed carry generation part consists of a novel AND-OR module (module 1) based on TG and CPL logic. Within the AND-OR module, implementation of AND and OR gates are quite similar, except the fact that nMOS and pMOS transistors are interchanged. The conditions required to design the proposed AND gate are as follows:

If $A = 0$, then $output = 0$ and (1)
If $A = 1$, then $output = B$ (2)

The first condition for AND gate design in (1) is carried out by the pass transistor N_2 and TG_1, respectively. The later condition (2) is carried out by TG_1. In the same way, conditions for designing OR gate are:

If $A = 1$, then $output = 1$ and (3)
If $A = 0$, then $output = B$ (4)

Here, conditions (3) and (4) are carried out by pass transistor P_2 and TG_2, respectively. A TG based 2:1 MUX (module 2: consists of TG_3 and TG_4) is used to select the appropriate carry-out signal from AND-OR module depending on input carry C_{in}.

B. Sum Generation

The sum output of the proposed FA is generated by cascading two XOR modules (module 3 and 4). The XOR gates have exactly the same structure and are implemented using TGs and PTs. The conditions for designing the XOR gate for module 3 are:

If $A = 0$, then $output = B$ (5)
If $A = 1$ and $B = 0$, then $output = \overline{A}$ (6)

The pass transistor P_3 in module 3 (XOR gate) implements condition (6) and the pass transistor N_3 implements condition (7). Employing exactly the same method, XOR gate for module 4 has been designed using C_{in} and A⊕B (output of module 3) as inputs. For this case, the conditions are:

If $C_{in} = 0$, then $output = A \oplus B$ (8)
If $C_{in} = 1$ and $A \oplus B = 0$, then $output = C_{in}$ (9)
If $C_{in} = 1$ and $A \oplus B = 1$, then $output = \overline{C_{in}}$ (10)
If $A = 1$ and $B = 1$,then $output = A$ (7)In

this case, condition (5) has been implemented using TG_5. In this case, the conditions (8), (9) and (10) have been implemented by TG_6, P_4 and N_4, respectively.

IV. Simulation Result and Discussion

To analyze various performance parameters, simulation has been conducted in GPDK 45 nm technology node using Cadence simulation tools. Buffers are added in the input and output side for simulation test bench. The output side also consisted a load capacitance of 6 fF. In this way, the circuit experiences significant signal distortion unlike realistic environment. Input frequency has been set to 100 MHz. For optimized transistor sizing, particle swarm optimization algorithm has been utilized for implementation of FAs [23]-[24]. For transistor sizing using swarm algorithm, we initialize a vector $\overrightarrow{W_{mn}}$ where m is the transistor count and n is the number of particles. Each particle has 3 sorts of movement tendency in the search space: (a) tendency due to its own inertia (b)

particle, then the current PDP is set as the particle's best PDP. In the same way, if the best PDP for current simulation run < the best PDPvalue so far found in the entire search space, then the team's best value is updated with the current value. In this way, after completing the desired number of iterations, the team's best value of PDP is chosen as the optimal PDP and the corresponding transistor widths are chosen for circuit implementation.

A. Performance of FA cells for various supply voltage

The post-layout simulation results on delay, power and Power Delay Product (PDP) for the supply voltage 0.4 V (minimum voltage in order to avoid sub-threshold operation), 0.8 V (mid-point voltage between 0.4 V and 1.2 V) and 1.2 V (normal operating voltage) are represented using Fig. 3 and Table I. The results (Fig. 3) demonstrate that proposed FA obtained superior performance in case of delay and PDP. Although the proposed design does not obtain best performance in power (Fig. 3b), still the value is low enough for practical utilization in modern processors. The least technology node in which 10-T FA [13] could operate is 180 nm technology with a least supply voltage of 1.8 V. Hence, to maintain uniform environment for comparison, performance parameters (15.03 µW power and 129.48 ps delay) of 10-T FA are not added in Table I.

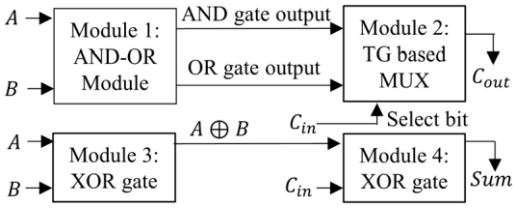

Fig. 1. Block diagram of proposed full adder.

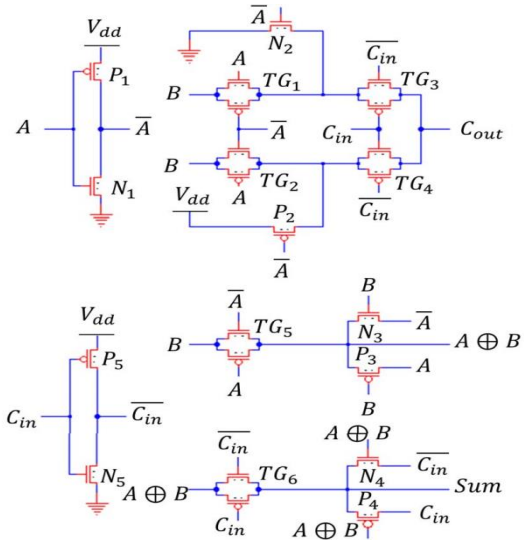

Fig. 2 Schematic of the proposed FA.

12-T [6], 14-T [12], HPSC [14] and Hybrid 2 [18] FAs could not operate flawlessly while simulated with 0.4 V supply voltage. Hence, performance parameters of these FAs for 0.4 V could not be obtained for presenting in Table I and Fig. 3. To figure out the least operating voltages of these FAs, further simulation has been conducted using 0.45 V-0.75 V supply voltage. The least supply voltage required for 12-T [6], 14-T [12], HPSC [14] and Hybrid 2 [18] FAs are 0.75 V, 0.7 V, 0.7 V and 0.5 V respectively. It has been also observed that delays of FA cells start increasing quite drastically while operating below 0.8 V supply voltage.

As technology scales down, interconnect performance depends more on the resistance rather than the capacitance [24]. To achieve the best performance, the interconnect resistance and capacitances need to be re-optimized. For 5nm node, as demonstrated by Pan et al. [24], increasing the interconnect width beyond half pitch without changing the interconnect pitch yields 55% improvement in energy-delay product for vertical field-effect transistor (VFET) circuits. Therefore, for more aggressive technologies, the interconnect width should be a target optimization parameter to achieve desired performance.

B. Performance of FAs operating in cascade

To inspect scalability, FAs are extended into 4, 8, 16, 32 and 64 bits in Ripple Carry Adder style as depicted in Fig. 4 [18]. No intermediate buffer has been added while cascading FAs. Simulation results on performance parameters are listedin Table II. It was observed that only 5 out of 20 existing FAsand the proposed design can operate when extended to 64-bits.As per Fig. 3, Hybrid 2 [18], Hybrid 6 [21] and GDI D1 [22] FAs showed promising performance as single cell. However, they can be only extended to maximum 8-bits. This limitation happens due to the decline of signal strength (voltage) while propagating through several stages.

Due to having CCMOS based logic style in the output terminals, the output signals come from V_{dd} and Gnd for CCMOS [7] and 24-T [11] FAs. As a result, the voltage gets replenished in each stage for which CCMOS [7] and 24-T [11] FAs do not face the problem of voltage deterioration in long carry chains.

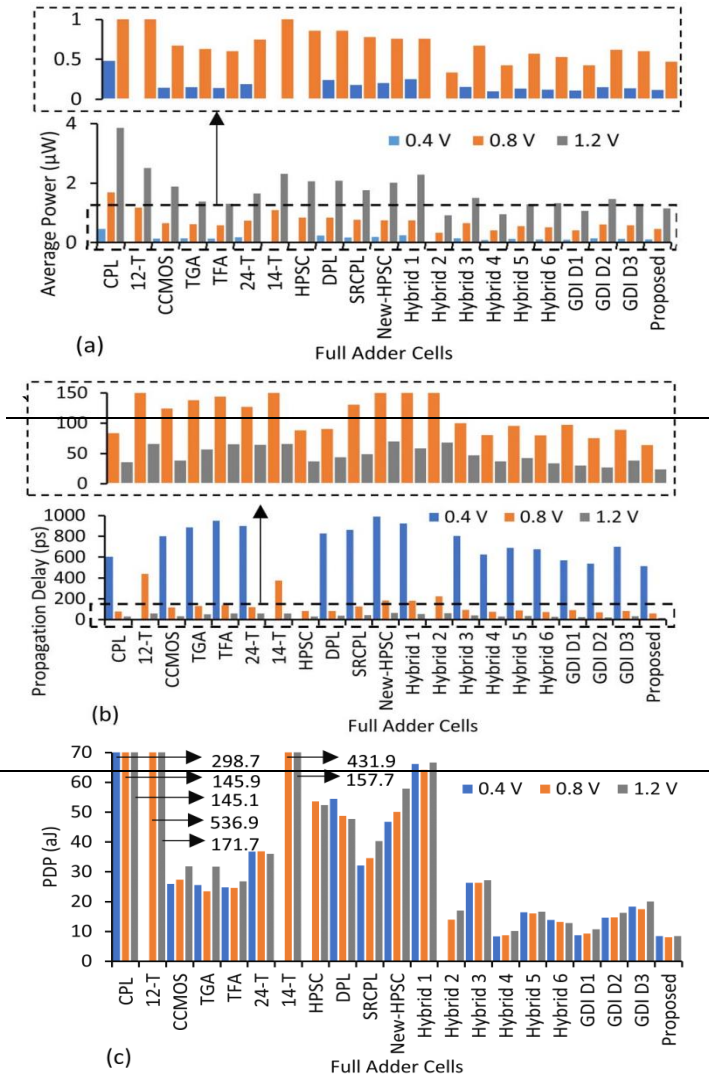

Fig. 3. Performance of FA cells (a) average power (b) propagation delay (c) PDP.

TABLE I
PERFORMANCE OF FULL ADDER CELLS UNDER VARIOUS SUPPLY VOLTAGE

TC: Transistor Count, AP: Average Power, DP: Dynamic Power (Switching Power + Short-Circuit Power), PDP: Power Delay Product, SP: Static Power, F: Failed to Operate, PR: Performance Ratio (Proposed FA Value: Best Value Obtained by Other FAs)																	
Full Adder	**Ref. no**	**TC**	**Power (AP in µW, DP and SP in nW)**									**Delay (ps)**			**PDP (aJ)**		
			0.4 V			**0.8 V**			**1.2 V**			**0.4 V**	**0.8 V**	**1.2 V**	**0.4 V**	**0.8 V**	**1.2 V**
			AP	**DP**	**SP**	**AP**	**DP**	**SP**	**AP**	**DP**	**SP**						
CPL	[5]	32	0.488	458.2	29.8	1.72	1612.8	107.3	3.89	3634.1	255.9	612.1	84.8	37.3	298.7	145.9	145.1
12-T	[6]	12	F	F	F	1.2	1158.4	41.6	2.54	2423.4	116.6	F	447.4	67.6	F	536.9	171.7
CCMOS	[7]	28	0.159	149.1	9.9	0.68	660.3	19.7	1.91	1841.6	68.4	809.3	125.8	39.7	145.7	85.5	75.8
TGA	[8]	20	0.163	158.8	8.2	0.64	617.4	22.6	1.41	1365.8	44.2	893.4	139.7	58.3	151.9	89.4	82.2
TFA	[10]	16	0.155	150.9	8.1	0.61	586.5	23.5	1.33	1288.7	41.7	957.5	145.6	66.8	155.1	88.8	88.8
24-T	[11]	24	0.202	189.9	12.1	0.76	724.8	35.2	1.68	1628.8	51.2	908.3	128.4	65.9	183.5	97.6	110.7
14-T	[12]	14	F	F	F	1.12	1059.7	60.3	2.34	2202.7	137.3	F	385.6	67.4	F	431.9	157.7
HPSC	[14]	22	F	F	F	0.89	844.5	45.5	2.09	1979.5	110.5	F	89.7	38.6	F	78	80.7
DPL	[15]	22	0.256	240.1	15.9	0.87	833.3	36.7	2.11	1986.3	123.7	835.6	91.9	45.6	213.9	79.9	96.2
SRCPL	[15]	20	0.193	182.8	10.2	0.7	759.8	31.1	1.79	1726	64	869.6	132.3	50.4	167.8	104.5	90.2
New-HPSC	[16]	24	0.217	205.3	11.7	0.77	739.8	30.2	2.04	1931.6	108.4	998.5	193.6	71.5	216.7	149.1	145.9
Hybrid 1	[17]	24	0.267	258.8	16.2	0.78	749.3	30.7	2.31	2176.4	133.6	932.4	189.1	60.2	248.9	145.6	139
Hybrid 2	[18]	16	F	F	F	**0.35**	**339.7**	**10.3**	**0.94**	**912.8**	**27.2**	F	231.4	69.6	F	81	65.4
Hybrid 3	[19]	22	0.169	162.6	6.4	0.68	661.1	18.9	1.53	1473.5	56.5	811.8	101.3	48.6	146.9	68.9	74.4
Hybrid 4	[20]	16	**0.113**	**106.9**	**6.1**	0.44	428.2	11.8	0.98	951.3	28.7	675.3	81.6	38.7	76.3	35.9	37.9
Hybrid 5	[21]	21	0.146	136.9	9.1	0.58	561.1	18.9	1.31	1270.4	39.6	697.5	96.8	43.9	108.1	56.1	57.5
Hybrid 6	[21]	23	0.133	125.3	7.7	0.54	522.5	17.5	1.35	1304.1	45.9	683.4	81.4	35.1	98.4	43.9	47.4
GDI D1	[22]	18	0.127	144.8	7.2	0.46	446.7	13.3	1.09	1054.7	35.3	599.8	98.8	31.8	76.17	43.5	34.7
GDI D2	[22]	22	0.165	155.6	9.4	0.63	604.6	25.4	1.49	1437.5	52.5	547.6	77.3	28.6	90.4	48.7	42.6
GDI D3	[22]	21	0.152	116.6	8.5	0.61	586.3	23.7	1.32	1277.6	42.4	708.3	90.53	39.7	114.7	55.2	52.4
Proposed	-----	22	0.129	122.2	6.8	0.48	466.6	13.4	1.17	1135.7	34.3	**523.8**	**65.7**	**25.3**	**67.6**	**31.5**	**29.6**
Performance Ratio (PR)			1.14:1	1.14:1	1.11:1	1.37:1	1.37:1	1.3:1	1.24:1	1.24:1	1.26:1	1:1.04	1:1.17	1:1.13	1:1,13	1:1.14	1:1.17

TABLE II
PERFORMANCE COMPARISON OF FULL ADDER CELLS OPERATING IN CASCADE

Supply voltage: 0.8 V, F: Failed to Operate, PR: Performance Ratio (Proposed FA Value: Best Value Obtained by Other FAs)																
Full Adder	**Ref. no**	**Power (µW)**					**Delay (ps)**					**PDP (fJ)**				
		4 bit	**8 bit**	**16 bit**	**32 bit**	**64 bit**	**4 bit**	**8 bit**	**16 bit**	**32 bit**	**64 bit**	**4 bit**	**8 bit**	**16 bit**	**32 bit**	**64 bit**
CPL	[5]	6.47	13.46	F	F	F	1256.7	4484.9	F	F	F	8.13	60.36	F	F	F
12-T	[6]	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
CCMOS	[7]	2.42	4.68	9.48	20.79	44.2	510.6	1042.5	2105.8	4233.2	8490.5	1.24	4.88	19.96	88.01	373.3
TGA	[8]	2.45	5.33	F	F	F	709.1	2145.7	F	F	F	1.74	11.44	F	F	F
TFA	[10]	2.5	4.45	F	F	F	478.7	2444.5	F	F	F	1.196	10.88	F	F	F
24-T	[11]	2.83	5.56	10.95	22.06	46.31	521.2	1078.5	2183.9	4389.6	8867.1	1.47	5.996	23.91	96.83	410.6
14-T	[12]	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
HPSC	[14]	3.24	6.3	12.45	25.98	F	561.8	1214.3	2520.2	5131.7	F	1.82	7.65	31.38	133.3	F
DPL	[15]	3.62	7.92	F	F	F	1467.6	4814.4	F	F	F	5.31	38.13	F	F	F
SRCPL	[15]	3.59	F	F	F	F	1934.3	F	F	F	F	6.94	F	F	F	F
New HPSC	[16]	2.84	5.57	11.11	22.75	F	945.5	2024.6	4203.5	8581.2	F	2.69	11.28	46.7	195.2	F
Hybrid 1	[17]	2.81	5.47	10.77	22.69	F	767.8	1552.5	3485.4	7057.8	F	2.16	8.49	37.54	160.1	F
Hybrid 2	[18]	**1.67**	**3.65**	F	F	F	1683.9	6436.7	F	F	F	2.81	23.49	F	F	F
Hybrid 3	[19]	2.53	5.41	11.69	25.45	55.94	413.3	881.6	1782.4	3572.5	7976.7	1.06	4.77	20.83	90.92	446.2
Hybrid 4	[20]	1.83	3.99	F	F	F	475.7	2487.6	F	F	F	0.87	9.93	F	F	F
Hybrid 5	[21]	2.39	5.23	F	F	F	539.6	3094.6	F	F	F	1.29	16.18	F	F	F
Hybrid 6	[21]	2.41	5.28	F	F	F	498.6	2986.3	F	F	F	1.2	15.77	F	F	F
GDI D1	[22]	1.93	4.27	F	F	F	500.3	2493.6	F	F	F	0.97	10.65	F	F	F
GDI D2	[22]	2.08	4.38	9.4	20.16	43.23	345.9	743.6	1621.2	3550.6	7985.1	0.72	3.26	15.24	71.58	345.2
GDI D3	[22]	2.57	5.56	11.86	25.94	56.87	410.7	883.1	1924.2	4290.8	9826.4	1.05	4.91	22.82	111.3	558.8
Proposed	-----	1.95	4.19	**9.01**	**19.11**	**40.19**	**285.6**	**613.8**	**1326.5**	**2946.7**	**6725.9**	**0.56**	**2.57**	**11.95**	**56.3**	**270.3**
Performance Ratio (PR)		1.17:1	1.15:1	1:1.04	1:1.05	1:1.08	1:1.21	1:1.21	1:1.22	1:1.2	1:1.19	1:1.28	1:1.27	1:1.28	1:1.27	1:1.28

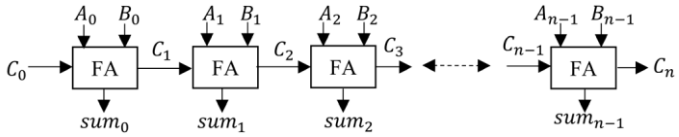

Fig. 4. Implementation of n-bit adder using 1-bit FA.

HPSC [14] and New-HPSC [16] FAs despite having CCMOS logic in the output terminals failed to operate in 64-bits. It occurred since their delays were extremely high to comply with the input frequency (100 MHz).

Hybrid 3 [19], GDI D2 [22], GDI D3 [22] FAs and the proposed design do not incorporate CCMOS logic in the output terminals. Still, they managed to operate up to 64-bits

due to their internal design structures. With careful inspection of Fig. 4, it can be observed that in each stage, A_n and B_n terms are inserted as fresh inputs. The carry term needs to propagate through several stages. In the proposed design (Fig. 2), since the input carry term C_{in} is used as gate control of the TGs, the possible signals which might appear at the output terminal (C_{out} terminal) are V_{dd}, Gnd or B. If we consider only B (since V_{dd} and Gnd will be provided as fresh inputs in each stage), for n=0, B_0 will appear in the output terminal (C_1 output terminal) whereas for n=1, B_1 will appear in output terminal (C_2 output terminal). Hence, the same signal does not propagate through n=0 to n=63 for which the design is not subjected to voltage degradation when extended to wide adder.

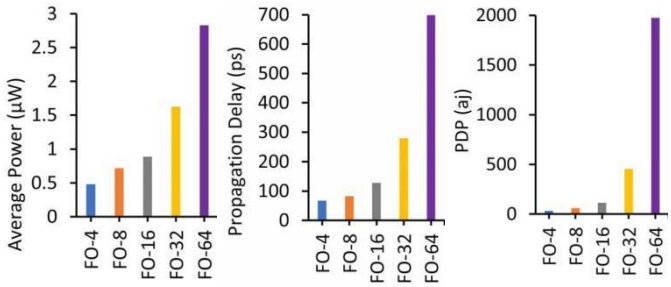

Fig. 5. Performance of proposed design under various loads with 0.8 V supply voltage.

C. Driving capability test of the proposed design

To test drive capability of the proposed FA design, a wide range of output loads from fan-out of 4 unit-size inverters (FO-4) to fan-out of 64 unit-size inverters (FO-64) have been applied. The supply voltage for this case was set to 0.8 V. Simulation data are illustrated using Fig. 5.

With careful observation of Fig. 5, it can be noticed that delay, AP and PDP are extremely high for FO-32 and FO-64. Hence, the most favorable fan-out load condition for the proposed design would be up to FO-16.

V. CONCLUSION

In this research, a novel hybrid FA design showing markedly improved performance has been proposed. Characteristics of the proposed design have been compared with twenty existing FAs. For performance analysis, simulation was conducted using Cadence toolset. As per simulation results, the proposed FA demonstrates superior performance in speed and PDP while operated as a single cell. Moreover, the FAs have been extended up to a word length of 64-bits in order to test scalability. Only the proposed FA and five of the existing designs have the ability to operate without utilizing buffers in intermediate stages while extended to 64-bits. In the cascade mode, the performance parameters point out that the proposed design is comparatively more suitable for wider word-length adder implementation which is the trend in modern computing systems where high-speed and efficient computation while consuming low power is essential.

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