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Implementation of UART using Verilog HDL and FPGA

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Abstract -

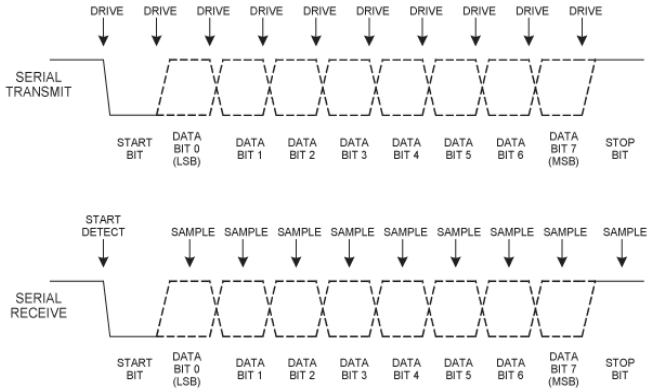
This study presents a hardware-based implementation of Universal Asynchronous Receiver Transmitter (UART) communication on the Nexys A7-100T Field Programmable Gate Array (FPGA) platform using Verilog HDL and Vivado Design Suite. UART serves as a fundamental serial communication protocol, widely adopted due to its simplicity and effectiveness. The work details the design methodology, including clock division, baud rate generation, and serial data transmission, while demonstrating successful communication between FPGA and PC. Experimental results confirm reliable and low-power serial data exchange, making this implementation ideal for embedded and communication systems.

Keywords

UART, FPGA, Serial Communication, Verilog HDL, Nexys A7-100T, Vivado, VLSI, Clock Gating

1.INTRODUCTION

Serial communication protocols such as UART are pivotal in embedded systems where resource-efficient and reliable data exchange is essential. Unlike parallel transmission, UART utilizes a minimal number of data lines, making it highly suitable for FPGA-based systems. This paper focuses on the design and implementation of UART protocol on the Digilent Nexys A7-100T FPGA board using Xilinx Vivado and Verilog HDL. The approach aims to minimize hardware complexity while ensuring communication accuracy and power efficiency.



1.1 UART frame format for both transmitter and receiver

The design incorporates a UART receiver module, enabling secure communication with the processor and facilitating the exchange of authentication keys through a terminal interface, such as PuTTY.Authentication keys fetched via UART are validated by the processor's security mechanisms before granting access to its core functionalities

2. Related Work

Several studies have explored UART protocol implementations using FPGAs. Prior work has emphasized baud rate accuracy, synchronization challenges, and resource optimization. This study builds upon these efforts by integrating clock gating techniques for power reduction and by validating the system using hardware-level testing between the FPGA board and a computer terminal.

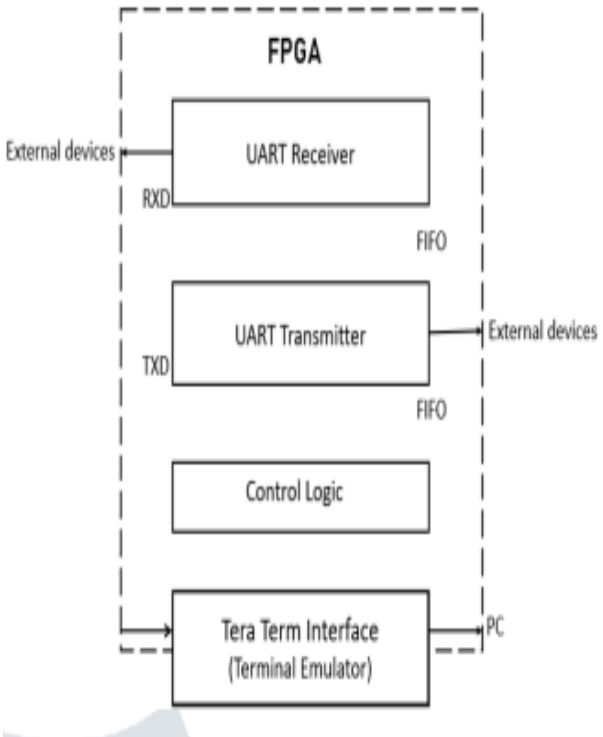
3. Methodology

The design follows a modular structure comprising:

- **Baud Rate Generator**: Divides the system clock to match the UART baud rate.
- **Transmitter (TX) Module**: Converts parallel data to serial for output.
- **Receiver (RX) Module**: Captures and reconstructs incoming serial data.
- **Clock Gating**: Employed to reduce dynamic power consumption in idle states.

Basic Features of UART Communication:

Asynchronous Communication.
Full Duplex: Simultaneous data transmission and reception.
Baud Rate: Defines the speed of communication (e.g., 9600, 19200).
Start and Stop Bits: Used to identify the beginning and end of data.
Parity Bit: Optional error checking mechanism.
Data Frame: Usually 8-bit data, but configurable depending on application.



Architecture Diagram

4. Implementation

The system was developed using Verilog HDL in the Vivado 2024.1 suite. Simulation was conducted using Vivado's built-in testbench environment to verify timing, bit accuracy, and module interaction. The design was synthesized and deployed onto the Nexys A7-100T FPGA, and connected to a PC through a USB-UART interface. Data exchange was monitored via a serial terminal program.

Advantages

Reliable performance
Compatibility with most systems.
Scalability.
Flexibility
Real-Time Monitoring with Putty

Limitations

Not suitable for long distances or very high speeds.
No default support for addressing multiple devices (unlike I2C).
Sensitive to baud rate mismatch**.**

5. Results and Discussion

The UART modules performed accurately at a baud rate of 9600 bps. Timing analysis confirmed compliance with UART communication standards. The power consumption was observed to reduce significantly when clock gating was active. Resource utilization (LUTs, Flip-Flops, etc.) remained within efficient limits, indicating scalability for larger embedded system.

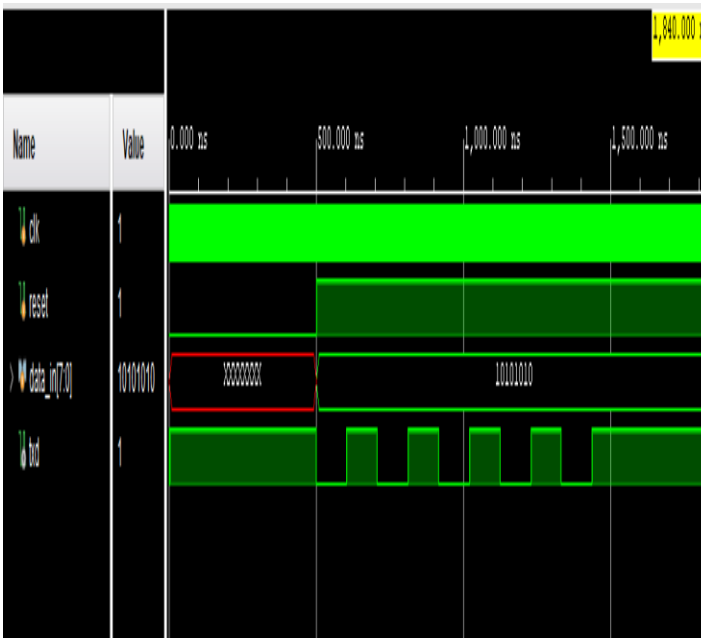


Fig1:- UART - Simulation Waveform

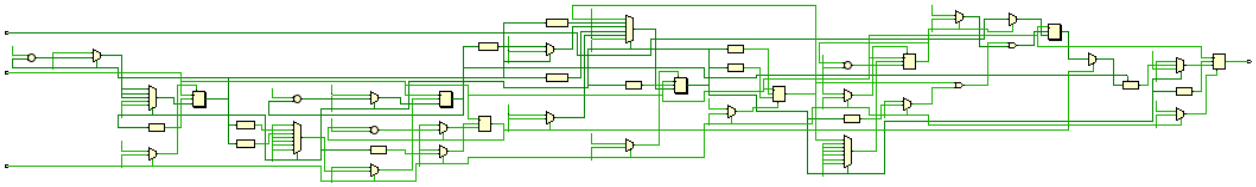


Fig2:- Schematic of UART

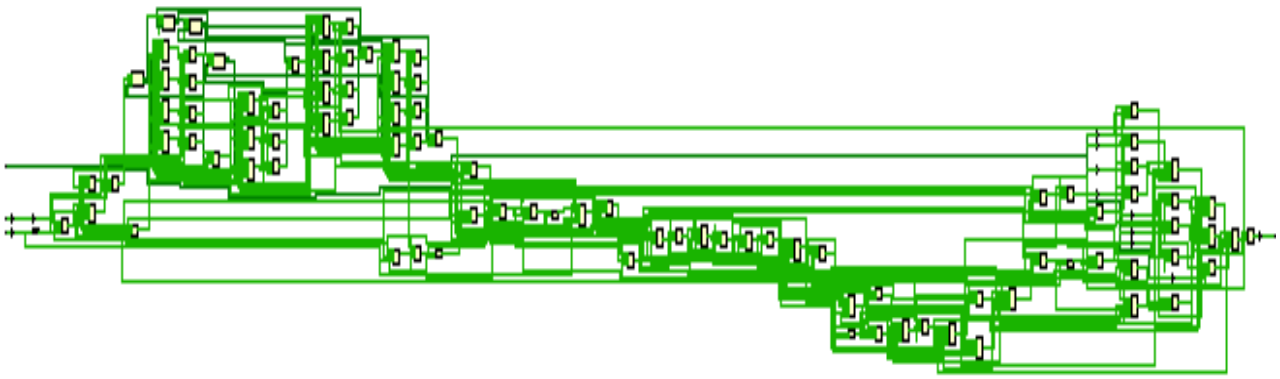


Fig3 :- Technology Schematic of UART

Hardware Interfacing and Testing with PuTTY

To validate the UART module implemented using Verilog HDL, the design was synthesized and programmed onto the **Nexys A7-100T FPGA board** using **Xilinx Vivado**. Real-time serial communication was tested through the **PuTTY terminal**, a widely used serial communication tool.

Connecting with PuTTY

- Open **PuTTY** and select **Serial** as the connection type.
- Set the **COM port** detected by your USB-to-UART (you can find it in Device Manager on Windows).
- Set **Baud rate** to 19200, **Data bits** to 8, **Stop bits** to 1, **Parity** to None, and **Flow control** to None..

Procedure

- Load the bitstream onto the Nexys A7 via Vivado.
- Open PuTTY and press the reset button on the board.
- Use the DIP switches to set an 8-bit value.
- Observe the corresponding character appear on the PuTTY terminal

Verification

The testbench was verified using simulation, and hardware functionality was validated by checking:

- Correct character display on PuTTY.
- Real-time transmission at the set baud rate.
- Stability across multiple transmissions.

Fig4: o/p Terminal

Fig5: inputs (ASCII values)

Character	ASCII (Decimal)	ASCII (Hex)	ASCII (Binary)
k	**107**	**0x6B**	**01101011**
e	**101**	**0x65**	**01100101**
y	**121**	**0x79**	**01111001**

ASCII values for K,E,Y

6. Conclusion

In this project, a Universal Asynchronous Receiver/Transmitter (UART) communication protocol was successfully designed and implemented using Verilog HDL, with real-time validation carried out on an FPGA platform. The system was composed of two key modules: a transmitter for converting parallel data into serial form with proper framing, and a receiver for capturing the serial data, verifying its integrity, and converting it back to parallel form. A baud rate generator operating at a predefined speed of 19200 baud ensured accurate timing and synchronization between the transmitter and receiver, enabling reliable data transmission. This work demonstrates a reliable and low-power UART implementation on an FPGA platform. Through modular design and clock gating, the system balances performance with energy efficiency. The design is suitable for integration into broader SoC communication systems, with potential for further expansion into high-speed or multi-UART architectures.

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