

# DESIGN AND INTEGRATION OF QUANTUM IMAGE SENSING AND QUANTUM ALU

JAYANDH SAJEEV<sup>[1]</sup>

jayandhsajeev.ei22@rvce.edu.in

K.B. RAMESH<sup>[2]</sup> kbramesh@rvce.edu.in

1. 2<sup>nd</sup> Year, Electronics and Instrumentation Engineering, R.V. College of Engineering, Bengaluru-59.

2. Associate Professor, Electronics and Instrumentation Engineering, R.V. College of Engineering, Bengaluru-59

#### ABSTRACT

The discovery and development of CMOS image sensors (CIS) are briefly reviewed in this study. The research focuses on a potential replacement called the Quantum Image Sensor (also known as QIS) made of quantum dots, a semiconducting material, which acts much differently from its bulk counterpart which is the traditional CIS[2] and when combined with Q-ALU how the speed increments.

**INDEX TERMS** Adder, arithmetic logic unit (ALU), CMOS, Quantum Dots, Image sensors

#### **INTRODUCTION**

Image sensors serve as the backbone of embedded vision applications, playing a pivotal role in capturing visual data essential for image processing and computer vision algorithms. Over the years, there has been a remarkable evolution in image sensor technology, with CMOS (Complementary Metal-Oxide-Semiconductor) sensors emerging as the dominant choice in consumer electronics. However, recent advancements, particularly in the realm of quantum dots and quantum computing, have sparked a paradigm shift in the field. This article explores the journey of image sensor technology, from the reign of CMOS to the emergence of quantum dots and the impending impact of quantum computing.

#### The Rise of CMOS Sensors:

CMOS sensors revolutionized the landscape of image sensing with their low-cost and low-power attributes, supplanting CCD (Charge-Coupled Device) sensors as the preferred choice in consumer electronics. Offering a versatile platform for capturing optical images and converting them into electrical signals, CMOS sensors quickly gained widespread adoption across various applications, including digital cameras, smartphones, and

surveillance systems. The inherent advantages of CMOS technology, such as higher integration density, lower

power consumption, and faster readout speeds, propelled its dominance in the market for nearly a decade.

### Quantum Dots: A New Frontier in Image Sensing:

While CMOS sensors reigned supreme, researchers delved into alternative approaches to image sensing, leading to the emergence of quantum dots as a promising candidate. Quantum dots, nanoscale semiconductor particles, exhibit unique optical and electrical properties, making them ideal candidates for enhancing the performance of image sensors. By leveraging quantum dot technology, researchers aimed to overcome the limitations of conventional CMOS sensors, including spectral sensitivity, dynamic range, and signal-to-noise ratio.

The utilization of quantum dots in image sensors offers several distinct advantages. Firstly, quantum dots possess tunable optical properties, allowing for precise control over their absorption and emission spectra. This tunability enables the customization of image sensors to match specific application requirements, such as multispectral imaging and lowlight sensitivity. Additionally, quantum dots exhibit exceptional quantum efficiency, enabling the efficient conversion of photons into electrical signals, thereby enhancing the overall sensitivity of the image sensor. Moreover, quantum dots demonstrate superior photochemical stability and resistance to photobleaching compared to organic dyes and traditional semiconductor materials. This inherent stability ensures long-term reliability and robustness, essential for applications demanding prolonged exposure to harsh environmental conditions.

Furthermore, quantum dot-based image sensors offer the potential for enhanced color reproduction and spectral fidelity. By leveraging the narrow emission spectra of quantum dots, image sensors can achieve precise color rendition and reduced crosstalk between adjacent pixels, thereby improving image quality and accuracy.

The integration of quantum dot technology into image sensors represents a significant paradigm shift in the field of image sensing, offering unprecedented capabilities and performance enhancements. However, despite the promising advancements, several challenges remain to be addressed, including scalability, manufacturing complexity, and costeffectiveness. Nevertheless, ongoing research and development efforts continue to drive the advancement of quantum dot-based image sensors, paving the way for their widespread adoption across diverse applications.

# **Quantum Computing: A Disruptive Force in Image Sensing:**

While quantum dots offer significant advancements in image sensor technology, the disruptive potential of quantum computing looms large over traditional binary devices like CMOS sensors. Quantum computing harnesses the principles of quantum mechanics to perform computations exponentially faster than classical computers, enabling the solution of complex problems that are currently intractable.

The impact of quantum computing on image sensing extends beyond traditional algorithms and processing techniques. Quantum computers have the potential to revolutionize image analysis and pattern recognition tasks by leveraging quantum algorithms, such as quantum machine learning and quantum image processing. These algorithms exploit the intrinsic properties of quantum

systems, such as superposition and entanglement, to achieve unprecedented levels of computational efficiency and accuracy.

Moreover, quantum computing offers transformative capabilities in image reconstruction and enhancement, enabling the synthesis of high-resolution images from sparse or noisy data. Quantum algorithms for image reconstruction leverage advanced optimization techniques and quantum Fourier transforms to recover detailed information from incomplete or degraded images, thereby overcoming the limitations of traditional methods.

# METHODOLOGY

In contemporary imaging devices, such as those found in smartphones, the journey of light begins with its passage through an intricate arrangement of red, green, and blue filters, as well as various lenses. These components collectively facilitate the modulation of light before it reaches the sensor pixel on the silicon CMOS chip. This pixel, often referred to as a photosite, serves as the fundamental unit for photon collection. The color recorded by each photo-site is determined by the specific filters it encounters during this process.

One of the distinguishing features that sets CMOS image sensors apart from their CCD counterparts lies in their ability to integrate multiple processing and control functions directly into the sensor-integrated circuit. Beyond the primary task of photon collection, CMOS sensors incorporate a range of functionalities, including timing logic, exposure control, analog-todigital conversion, shuttering, white balance adjustment, gain modification, and initial image processing algorithms. This integration is facilitated by an architectural design that resembles that of a random-access memory cell, enabling efficient execution of diverse tasks within a compact framework.

The operational principles of cameras equipped with quantum-dot-based detectors closely mirror those of their silicon CMOS counterparts. When a quantum dot within a photosite absorbs a photon, an electron is released from its localized bond.

In the realm of infrared imaging, contemporary infrared cameras exhibit functionality akin to visiblelight cameras, albeit with significant differences in the materials employed for light absorption. Traditional

infrared cameras rely on semiconductors characterized by a narrow bandgap, such as Lead Selenide (PbSe) and Indium Antimonide (InSb). Notably, these materials necessitate separate fabrication from the silicon CMOS circuits responsible for current measurement and image generation. Subsequently, the detector array and circuitry must be interconnected at each pixel, typically accomplished through metal-to-metal bonding.

This interconnection process, commonly referred to as hybridization, is inherently time-intensive. It involves the application of small indium bumps to every pixel of both the detector array and the CMOS circuitry. Subsequently, specialized manufacturing equipment aligns and presses the two components together, followed by a brief melting of the indium to establish electrical connections. The intricacies of hybridization constrain the feasible array sizes, pixel dimensions, and sensor resolutions, contributing to its reputation as a low-throughput and costly procedure.

However, quantum dots exhibit remarkable potential in revolutionizing infrared imaging technology. Quantum dots, which possess comparable sensitivity to infrared light as traditional materials, can be synthesized using cost-effective, large-scale chemical processing techniques. Moreover, infrared-absorbing quantum dots can be effortlessly applied to chips after the completion of silicon circuitry, obviating the need for hybridization. By eliminating the hybridization step, infrared cameras can achieve higher resolution and pixel density, facilitated by smaller pixel sizes that no longer necessitate accommodation for indium bumps.

The absence of hybridization not only enhances resolution but also facilitates the development of smaller sensor dimensions. This, in turn, enables the production of infrared cameras with reduced form factors and enhanced portability, all at a fraction of the cost associated with traditional manufacturing methods. Moreover, quantum dots offer superior light absorption efficiency compared to silicon, particularly in specific wavelengths contingent upon their size. Manufacturers can leverage this tunability to engineer sensors with heightened sensitivity across a broader spectrum of light, resulting in an expanded colour gamut and enhanced imaging capabilities.

# Quantum Metrology:

Quantum metrology has garnered significant attention among physicists for its utility, notably exemplified by its application in groundbreaking projects like the

| Chirality | Diameter<br>of<br>CNT(nm) | Threshold Voltage<br>of N-CNTFET(V) | Threshold Voltage<br>of P-CNTFET(V) |
|-----------|---------------------------|-------------------------------------|-------------------------------------|
| (19,0)    | 1.487                     | 0.289                               | -0.289                              |
| (13, 0)   | 1.018                     | 0.428                               | -0.428                              |
| (10, 0)   | 0.783                     | 0.559                               | -0.559                              |

Laser Interferometer Gravitational-Wave Observatory (LIGO), which led to the detection of gravitational waves and earned the Nobel Prize in Physics. Leveraging the principles of quantum mechanics, quantum metrology offers profound advancements in measurement and parameter estimation for various systems. In essence, quantum metrology enables a substantial enhancement in measurement accuracy and precision compared to classical methods.

# LOW POWERED TERNARY ARITHMETIC LOGIC CIRCUITS

Our Ternary Arithmetic Logic Circuit can do nine different things. These include three arithmetic operations (like addition and subtraction) and six logical operations (like AND, OR, and XOR). Each operation is Conventionally, when conducting N-independent samples to estimate a signal embedded in additive white Gaussian noise, the estimation error diminishes proportionally to  $1/\sqrt{N}$ . However, the judicious utilization of quantum entanglement allows for a reduction in estimation error proportional to 1/N, resulting in a remarkable improvement equivalent to a gain of  $\sqrt{N}$ . This capability holds immense promise in diverse domains such as signal processing, remote sensing, localization, and navigation.

Illustrated in Figure 1 are parallel estimation strategies employing quantum metrology, with green blocks denoting the incorporation of quantum entanglement. Four distinct strategies are delineated, with the first letter indicating whether classical (C) or quantumentangled (Q) realization is employed at the transmitter end, and the second letter indicating a similar distinction at the receiver end. Generally, the deployment of quantum entanglement at the receiver end proves more advantageous, contributing to enhanced measurement precision and accuracy.

In practical terms, the integration of quantum entanglement into measurement protocols offers unprecedented opportunities for advancing scientific endeavors and technological applications. By harnessing the unique properties of entangled quantum states, researchers can surpass the limitations of classical measurement techniques, thereby unlocking new frontiers in precision measurement and parameter estimation.

determined by the values on the S0 and S1 lines. You can see the complete list of operations in Table 2.

Table 2: Logic operational Truth table for proposed LP-TALC

| <b>S</b> 0 | <b>S1</b> | Function           |
|------------|-----------|--------------------|
| 0          | 0         | Ternary Buffer     |
| 0          | 1         | Ternary Inverter   |
| 0          | 2         | Ternary NAND       |
| 1          | 0         | Ternary NOR        |
| 1          | 1         | Ternary XOR        |
| 1          | 2         | Ternary XNOR       |
| 2          | 0         | Ternary Adder      |
| 2          | 1         | Ternary Subtractor |
| 2          | 2         | Ternary Comparator |

The regular design for Ternary Arithmetic Logic Circuits involves decoders for choosing functions, functional modules for performing operations, and multiplexers for selecting outputs (shown in Fig 4). Typically, transmission gates are used as control circuits to enable corresponding functional modules. Some designs use equal 4-bit transmission gates to minimize area and control transistors efficiently. However, despite efforts to reduce power leakage, there are still issues, especially when dealing with a higher number of transistors. The more transistors, the higher the chance



## Quantum-dot Cellular Automata (QCA) ALU:

In recent times, several structures have been introduced to enhance the efficiency of Arithmetic Logic Unit (ALU) components. However, there are only a limited number of structures proposed for Quantum-dot Cellular Automata (QCA) ALU, which include full adders, multiplexers, and various logic gates integrated into a cohesive structure, each with detailed designs. of static power dissipation. Even though Carbon Nanotube Field-Effect Transistor (CNTFET) transistors have minimal leakage, having many transistors could lead to power loss. The area-wise reports of the 1-bit Multilayer ALU are presented in Fig. 16. It can be inferred

from this figure the proposed design of 1-bit Multilayer ALU occupies 304 cells, whereas the previous many designs in between (330- 430) cells, from which it can be concluded that the overall cell count has been reduced.



Fig. 4 Existing TALU Architectural design [13]

The QCA full adder is a crucial component in arithmetic units as it plays a key role in multiplication and subtraction operations. Multiplication often involves successive sum operations, while subtraction utilizes two's complement operations. There have been diverse designs for QCA full adders, which can be categorized into single-layer schemes[3]and multiple-layer schemes.

Design of a QCA Full Adder[7]

Ι



In simple terms, a Full Adder (FA) is a fundamental component extensively used in arithmetic operations. It's not only involved in addition but also plays a role in other operations like multiplication, division, and subtraction. The FA is a digital circuit with three inputs: two digits (A and B) and one bit (Cin) representing the carry from the previous adder. It produces two outputs, namely Sum (S) and Carry Out (Cout).

In the proposed FA, the Sum output is determined by the direct interactions between Quantum-dot Cellular Automata (QCA) cells, while the Carry output is generated based on a majority voting mechanism. The mathematical expressions for Carry Out and Sum are defined by equations (1) and (2), respectively.

Carry Out = a\*b + a\*c + b\*c = M(a, b, c)

Sum=  $a \wedge b \wedge c$ 

Here, M represents a majority gate. The proposed FA structure, as illustrated in Figure 1, consists of two main components: a majority voter and a three-input XOR gate. Notably, this structure utilizes only 26 cells and is implemented in a single layer. In the visual representation of QCA designs, different colored cells (green, purple, blue, and yellow) indicate distinct clock zones (0, 1, 2, and 3, respectively).

The arithmetic and logic operations on binary codes are used when performing Interbase transformations in the structure of multi-base processors. Therefore, with 128-2048bit's processors, a particularly important scientific problem

is the significant improvement of ALU components in the

Rademacher TNB according to the criterion of maximum speed.



Fig. 1. Proposed QCA full adder structures (a) Logical diagram (b) QCA layout.

B. Design of a QCA Multiplexer for Arithmetic Unit[8]

the proposed Quantum-dot Cellular Automata (QCA) Arithmetic Logic Unit (ALU) has a set of arithmetic and bitwise logical operations, as detailed in Table I. Notably, all eight arithmetic functions involve a fixed sum operation, making it easy to perform these operations using the proposed full adder.

The arithmetic operations have distinct features. In four cases where Cin (input carry) is '0', the corresponding operations involve adding '0'. In other operations where Cin is '1', the sum with '1' is fixed. Operand 'A' and addition with the input carry (Cin) are constants in all eight arithmetic operations, allowing them to be directly connected to the full adder.

International Journal of Scientific Research in Engineering and Management (IJSREM)

Volume: 08 Issue: 05 | May - 2024

SJIF Rating: 8.448

ISSN: 2582-3930

| TABLE I           |    |     |          |     |     |  |  |  |
|-------------------|----|-----|----------|-----|-----|--|--|--|
| <b>OPERATIONS</b> | OF | THE | PROPOSED | QCA | ALU |  |  |  |

| Operations | Mode | <b>S</b> 1 | S0 | Cin | OUT                             |
|------------|------|------------|----|-----|---------------------------------|
|            | 0    | 0          | 0  | ×   | $A \oplus B$                    |
| Logical    | 0    | 0          | 1  | ×   | $\mathbf{A}^{\wedge}\mathbf{B}$ |
|            | 0    | 1          | 0  | ×   | $A {\vee} \; B$                 |
|            | 0    | 1          | 1  | ×   | A'                              |
|            | 1    | 0          | 0  | 0   | А                               |
| Arithmetic | 1    | 0          | 0  | 1   | A+1                             |
|            | 1    | 0          | 1  | 0   | A-1                             |
|            | 1    | 0          | 1  | 1   | А                               |
|            | 1    | 1          | 0  | 0   | A+B                             |
|            | 1    | 1          | 0  | 1   | A+B+1                           |
|            | 1    | 1          | 1  | 0   | A+B'                            |
|            | 1    | 1          | 1  | 1   | A-B                             |





To simplify the input conditions for the full adder, certain values are omitted, such as operand 'A', "addition with '0", and "addition with '1". The remaining values, including '0', '1', 'B', and 'B', are entered into the full adder under various circumstances. Table II illustrates the inputs of the full adder in different situations along with the corresponding Karnaugh map.

F = AS0S1 + BS'0S1 + CS0S'1 + DS'0S'1 =S0(AS1 + CS'1) + S'0(BS1 + DS'1) = S0(AS1 + (C' + S1)') + S'0(BS1 + (D' + S1)')



Fig. 2. (a) QCA layout (b) Logical diagram, of the proposed applicationspecific QCA 4:1 multiplexer.

## C. Design of a QCA Multiplexer for Logical Unit[9]

The logical unit must able to carry out the XOR, AND, OR, and NOT operations. This unit is designed based on the cell interaction. This unit is shown in Fig. 3 and it generates Z1 as output,

Z1=S1'S0'(A^B)+S1'S0(A+B)+S1S0(A')

The implementation of such a structure is based on the formation of input data by a pair-phase input that correspond to the qubits of quantum processors.

The basic element of such a binary adder is a one-bit adder,

what was proposed by authors and the structure of which is

presented

## **PROPOSED METHODOLOGY**

The integration of quantum image sensing and quantum arithmetic logic units (ALUs) aims to revolutionize image processing and computation[6]. This involves creating a unified quantum computing platform where quantum image data can be efficiently transferred between modules, pre-processed, and subjected to arithmetic and logical operations directly within the quantum domain. By leveraging hybrid quantumclassical processing[8], feedback mechanisms, and optimization techniques, the integrated system strives for enhanced performance, scalability, and resource Through continuous utilization. research and development, this approach promises groundbreaking



advancements in applications such as medical imaging, remote sensing, and computer vision

## CONCLUSION

Quantum image sensing and quantum arithmetic logic units (ALUs) represent cutting-edge innovations poised to redefine image processing and computation. Quantum sensing entails image capturing and representing images using quantum principles, potentially offering advantages in data representation and processing efficiency. On the other hand, quantum ALUs are designed to perform arithmetic and logical operations quantum data. directly on promising exponential speedup for certain computational tasks. The integration of these technologies holds immense potential for accelerating image processing tasks, enabling applications such as image quantum-enhanced compression, encryption, and pattern recognition. As research progresses and quantum computing capabilities advance, quantum image sensing coupled with quantum ALUs is expected to unlock new frontiers in computational imaging and beyond, revolutionizing industries reliant on vast amounts of visual data.

#### REFERENCES

[1] A. Kumar, S. K. Gupta and P. Kota, "4-trit CNFET-based Arithmetic Logic Unit," 2023 International Conference on Device Intelligence, Computing and Communication Technologies, (DICCT), Dehradun, India, 2023, pp. 34-38, doi: 10.1109/DICCT56244.2023.10110209.

[2] K. Swetha, K. L. Krishna, J. V. S. Sowmya, D. S. Reddy, G. Pravallika and G. A. Kumar, "Area Efficient Multilayer Arithmetic Logic Unit Implementation in Quantum-dot Cellular Automata," 2021 Third International Conference on Intelligent Communication Technologies and Virtual *Mobile Networks (ICICV)*, Tirunelveli, India, 2021, pp. 584-589, doi: 10.1109/ICICV50876.2021.9388584.

[3] W. Shi et al., "Arithmetic and Logic Circuits Based on ITO-Stabilized ZnO TFT for Transparent Electronics," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 69, no. 1, pp. 356-365, Jan. 2022, doi: 10.1109/TCSI.2021.3100138.

[4] R. Samanth, A. Amin and S. G. Nayak, "Design and Implementation of 32-bit Functional Unit for RISC architecture applications," 2020 5th International Conference on Devices, Circuits and Systems (ICDCS), Coimbatore, India, 2020, pp. 46-48, doi: 10.1109/ICDCS48716.2020.243545.

[5] M. Essam, A. Shalaby and M. Taher, "Design and Implementation of Low Power Posit Arithmetic Unit for Efficient Hardware Accelerators," 2022 10th International Japan-Africa Conference on Electronics, Communications, and Computations (JAC-ECC), Alexandria, Egypt, 2022, pp. 68-71, doi: 10.1109

[6] D. Bhuvana Suganthi, M. Shivaramaiah, A. Punitha, M. K Vidhyalakshmi and S. Thaiyalnayaki, "Design of 64-bit Floating-Point Arithmetic and Logical Complex Operation for High-Speed Processing," 2023 International Conference on Intelligent and Innovative Technologies in Computing, Electrical and Electronics (IITCEE), Bengaluru, India, 2023, pp. 928-931, doi: 10.1109/IITCEE57236.2023.10091011.

[7] S. Sengupta, P. Sarkar and A. Dastidar, "Design of a 4 Bit Arithmetic & Logic Unit, Evaluation of Its Performance Metrics & its Implementation in a Processor," 2020 International Conference for Emerging Technology (INCET), Belgaum, India, 2020, pp. 1-8, doi: 10.1109/INCET49848.2020.9154017.

[8] S. Babaie, A. Sadoghifar and A. N. Bahar, "Design of an Efficient Multilayer Arithmetic Logic Unit in Quantum-Dot Cellular Automata (QCA)," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 66, no. 6, pp. 963-967, June 2019, doi: 10.1109/TCSII.2018.2873797.

[9] A. A. Purohit, M. R. Ahmed and R. V. S. Reddy, "Design of Area Optimized Arithmetic and Logical Unit for Microcontroller," 2020 IEEE VLSI DEVICE



CIRCUIT AND SYSTEM (VLSI DCS), Kolkata, India, 2020, pp. 335-339, doi: 10.1109/VLSIDCS47293.2020.9179942.

[10] J. Kralev, "Design of Floating-Point Arithmetic Unit for FPGA with Simulink®," IEEE EUROCON 2019 -18th International Conference on Smart Technologies, Novi Sad, Serbia, 2019, pp. 1-5, doi: 10.1109/EUROCON.2019.8861860.