International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 10 Issue: 10 | Oct - 2026 SJIF Rating: 8.659 ISSN: 2582-3930

Design and Performance Analysis of a Reduced-Capacitance H-9 Five-Level Switched-Boost Capacitor Transformer Less Inverter

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Abstract— This paper examines a single-stage, single-phase H-9 transformerless inverter integrating a switched-boost (SB) cell, switched-capacitor (SC) network and polarity-generation bridge for photovoltaic energy conversion. The architecture uses nine semiconductor switches and synthesizes five output levels while reducing the need for large energy-storage capacitors. The study reorganizes the supplied design documentation, switching relations, Simulink plots and reported experimental observations. For a 40 V input and a duty ratio of 0.6, the ideal capacitor voltage is 100 V and the maximum pole-voltage magnitude is 200 V. The supplied documentation reports leakage currents of 10 mA and 12.8 mA at 50 and 30 ohm loads, respectively, and a filtered-voltage THD of 1.29% in a cited prototype study. Source simulation traces are reproduced and distinguished from those experimental reports. Practical limitations, including capacitor startup transients and grid-interface verification, are discussed.

Index Terms— H-9 inverter, five-level conversion, photovoltaic, switched boost, switched capacitor, leakage current, transformer-less inverter.

I. INTRODUCTION

Transformerless photovoltaic (PV) converters eliminate the line-frequency transformer, improving power density and reducing size. Their principal challenges include parasitic ground leakage, switching ripple, capacitor stress and the limited dc-link voltage available from low-voltage sources. Multilevel conversion distributes voltage steps and can reduce filter demands, but may increase the semiconductor count or require large floating capacitors.

The H-9 configuration considered here combines boost energy transfer and capacitor-based level generation in a single conversion stage. A virtual-ground filtering path is intended to redirect high-frequency common-mode current away from PV-to-ground parasitic capacitances. The objective of this paper is to present a compact, traceable account of the source design and its reported waveforms without treating secondary prototype data as independently reproduced measurements.

II. TOPOLOGY AND POWER FLOW

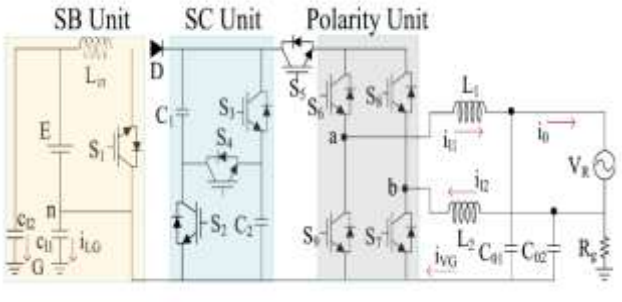


Fig. 1. Source topology: switched-boost, switched-capacitor and polarity stages.

The SB cell consists of input inductor Lin, switch S1 and diode D. Capacitors C1 and C2, with switches S2–S5, participate in voltage synthesis; S6–S9 control polarity. Two output filter inductors and capacitors provide a virtual-ground high-frequency bypass path.

III. OPERATING PRINCIPLE

The boost switch periodically stores energy in Lin and transfers it through D to the SC network. Capacitor charging and discharging occur over successive switching states. The polarity stage maps the available positive voltage steps to positive and negative output half-cycles.

$$VC1 = VC2 = VC = E / (1 - D) \quad (1)$$

$$Vmax = 2E / (1 - D) \quad (2)$$

$$VIo,1 = maVmax \quad (3)$$

Here E is the input dc voltage, D is the nominal boost duty ratio and ma is the modulation index. Equations (1)–(3) are ideal steady-state expressions; losses, dead time, parasitics and control saturation can reduce practical gain.

TABLE I
SWITCHING STATE OF THE PROPOSED FIVE-LEVEL INVERTER

States	v_0	ON State Switches	C_1, C_2, L_{in}	v_{an}, v_{bn}
$2V_C$ (a)	$\frac{2E}{1-D}$	S_1, S_4, S_5, S_6, S_7	$\downarrow,\downarrow,\uparrow$	$\frac{2E}{1-D}, 0$
V_C (b)	$\frac{E}{1-D}$	$D, S_2, S_3, S_5, S_6, S_7$	$\uparrow,\uparrow,\downarrow$	$\frac{E}{1-D}, 0$
V_C (c)	$\frac{E}{(1-D)}$	S_1, S_2, S_5, S_6, S_7	$\downarrow,\downarrow,\uparrow$	$\frac{E}{(1-D)}, 0$
0.0 (d)	0	S_2, S_3, S_6, S_8	$\uparrow,\uparrow,\downarrow$	$\frac{E}{2(1-D)}, \frac{E}{2(1-D)}$
$-V_C$	$\frac{-E}{(1-D)}$	S_1, S_2, S_5, S_8, S_9	$\downarrow,\downarrow,\uparrow$	$0, \frac{E}{(1-D)}$
$-V_C$	$\frac{-E}{1-D}$	$D, S_2, S_3, S_5, S_8, S_9$	$\uparrow,\uparrow,\downarrow$	$0, \frac{E}{1-D}$
$-2V_C$	$\frac{-2E}{1-D}$	S_1, S_4, S_5, S_8, S_9	$\downarrow,\downarrow,\uparrow$	$0, \frac{2E}{1-D}$

↑, ↓ indicate the charging and discharging state of the capacitors and inductor.

Fig. 2. Switching-state table reproduced from the supplied documentation.

A. Five-level voltage synthesis

The output sequence is +2VC, +VC, 0, −VC and −2VC. Positive and negative sequences use corresponding polarity-switch combinations. During the zero state, current may circulate through a selected freewheeling path while the input energy-storage cell continues its cycle.

B. Modulation and capacitor balancing

The source describes constant-frequency operation of the SB switches with level-shifted multicarrier PWM applied to the level-selection switches. Repeated charge/discharge intervals provide a natural balancing mechanism under the documented nominal conditions. Balance should nevertheless be checked during startup, irradiance transients and unbalanced loading.

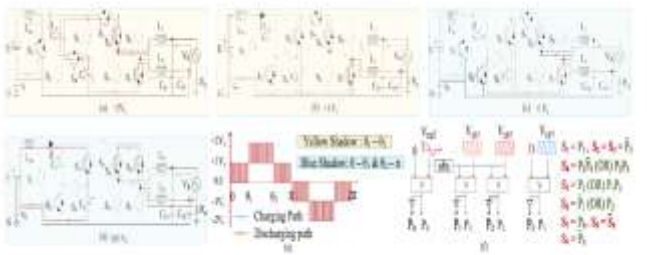


Fig. 3. Source operating states and carrier-based modulation schematic.

IV. DESIGN AND FILTER CONSIDERATIONS

Input inductance is selected from allowable switching-frequency current ripple, while C1 and C2 are chosen from permissible voltage ripple and charge-transfer demand. For an idealized boost interval, the first-order design relationships are:

$$\Delta iL \approx E\, D / (Lin\, fsw) \quad (4)$$

$$\Delta vC \approx \Delta Q / C \quad (5)$$

The filter inductors L1 and L2 attenuate high-frequency differential-mode ripple. The paired output capacitors also provide a return path for switching-frequency displacement current, reducing current through the PV stray capacitance. This mechanism is not galvanic isolation and requires compliance-oriented leakage-current assessment.

$$C_{01} = C_{02} = C_f = \frac{i_{VG} C_P}{2 i_{LG}} \quad (5)$$

$$L_1 = L_2 = L = \frac{1}{\omega_{sw} \hat{i}_{01}} \left\{ \frac{i_{LG}}{\omega_0 C_P} - \hat{v}_{01} \right\} \quad (6)$$

Fig. 4. Source leakage-current paths and parasitic-capacitor observations.

A. Source parameter set

The source describes a 40 V dc input, 50 Hz ac output, 10 kHz switching frequency and a duty ratio of 0.6. Its reported prototype parameter table includes 330 µF/200 V switched capacitors, a 5 mH input inductor and filter inductors. These values are transcribed from the source; no new hardware design optimization is claimed.

TABLE III
SPECIFICATIONS OF THE PROPOSED SYSTEM

Parameter	Value
Input Voltage (E)	40V
IGBT, Diode	CT60AM-18F, MUR1560
DSP Microcontroller, Gate Driver	F28379D, TLP250
Load (Z_1, Z_2)	50Ω, 30Ω
Capacitors (C_1, C_2), Input Inductor (L_{in})	330μF/200V, 330μF/200V, .5mH
Filter Parameter (C_{01}, C_{02}, L_1, L_2)	2μF, 2μF, 1.5mH, 1.5mH
Parasitic Capacitors (C_{11}, C_{12})	100nF, 100nF
Output freq (f_0), Carrier freq (f_{sw})	50Hz, 10kHz
Modulation Index (m_a), Duty Cycle (D)	0.8, 0.6

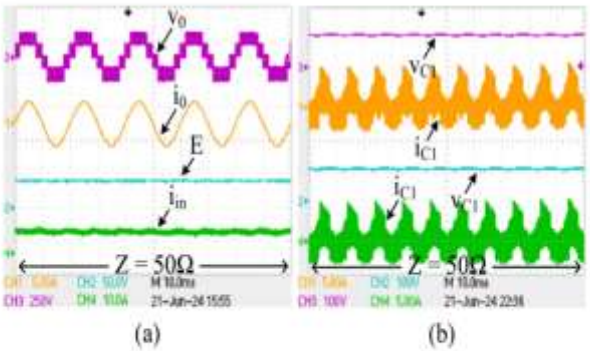


Fig. 6. Experimental results for a 50Ω load: (a) output voltage (v_0), current (i_0), input voltage (E), and current (i_{in}); and (b) capacitor voltages (V_{C1}, V_{C2}) and currents (i_{C1}, i_{C2}).

Fig. 5. Source prototype specifications and 50-ohm experimental traces.

B. Expected voltage levels

Substituting E = 40 V and D = 0.6 into (1) gives VC = 100 V. Equation (2) then gives Vmax = 200 V, consistent with the five nominal levels ±200 V, ±100 V and 0 V described in the source.

V. SIMULATION MODEL AND WAVEFORMS

The uploaded documentation contains a MATLAB/Simulink schematic and plots for a one-second time window. The plots below are source images, not newly executed simulations. Their axes and interpretations are retained; the absence of the original .slx model and numeric traces limits independent reproduction.

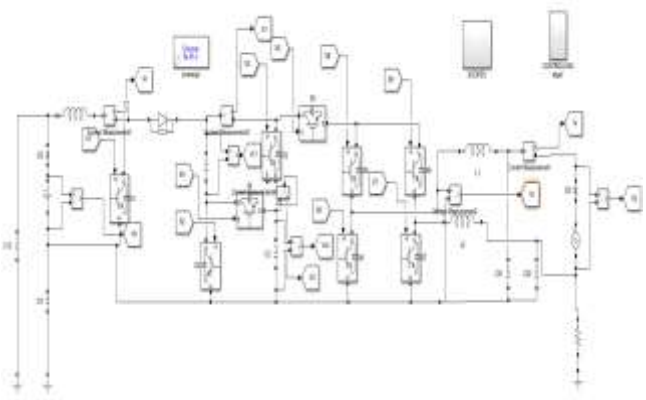


Fig. 6. MATLAB/Simulink inverter schematic from the supplied documentation.

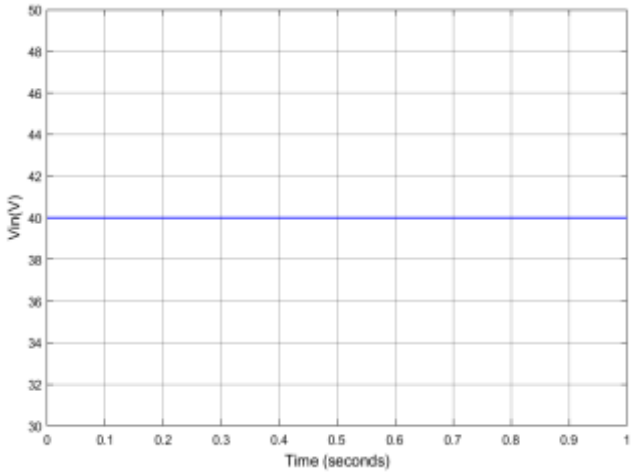


Fig. 7. Simulated dc input voltage, held at 40 V over 0–1 s.

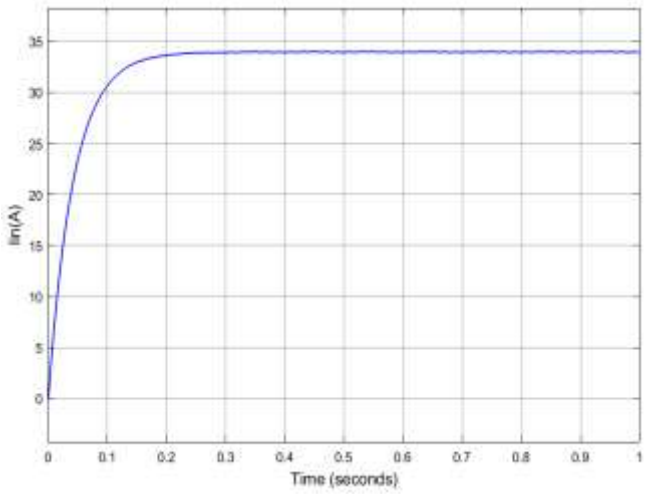


Fig. 8. Simulated input-current startup transient, settling near 34 A.

The source plots show a regulated 40 V input and an initial current transient followed by approximately steady current. The near-34 A current is read visually from the supplied graph, not recalculated from raw simulation samples. The simulation model and experimental setup should not be assumed to have identical operating points.

VI. AC OUTPUT AND CAPACITOR RESPONSE

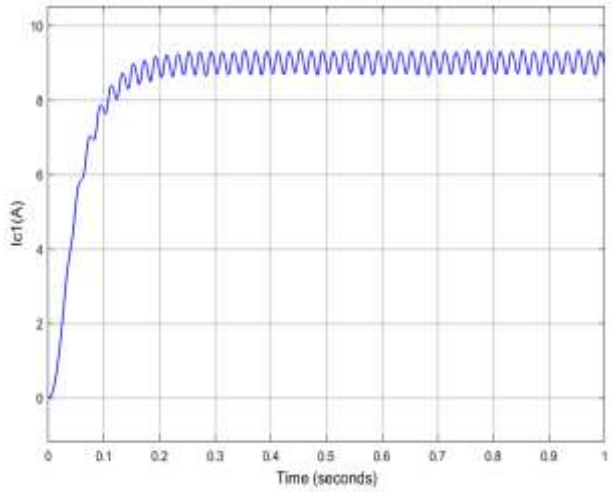


Fig.8. Source simulation: capacitor-current startup and steady ripple.

The source model presents a sinusoidal grid-voltage trace with a peak close to 100 V and a load-current trace with a peak near 9 A. The source does not provide a synchronized numerical dataset, so phase angle, power factor and measured THD cannot be independently extracted from these pictures.

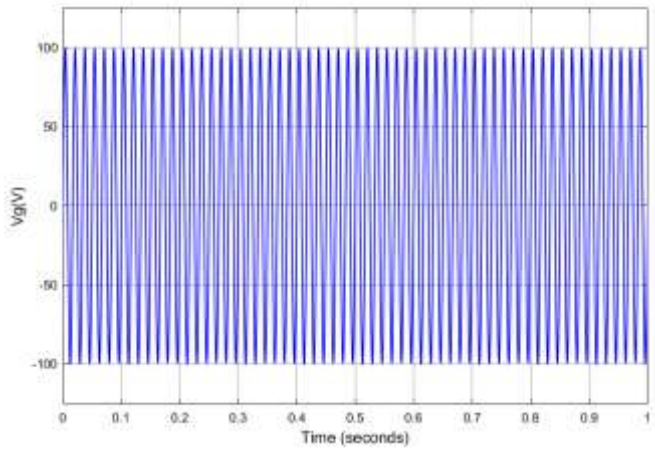


Fig. 9. Source simulation: sinusoidal grid voltage (approximately ±100 V).

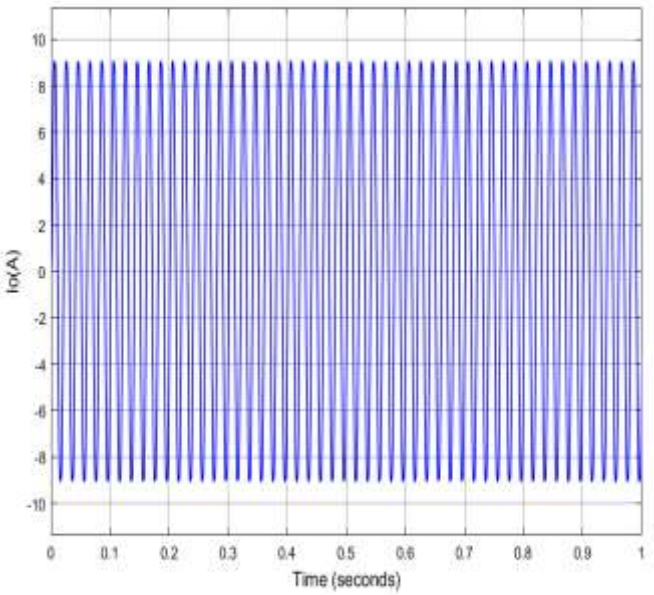


Fig. 10. Source simulation: load current (approximately ±9 A).

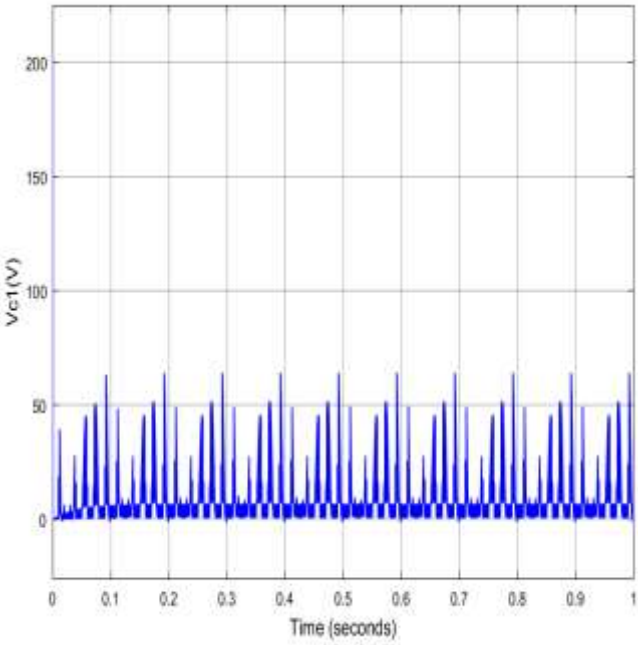


Fig. 11. Source simulation: capacitor C1 voltage with periodic spikes.

The C1 trace exhibits repeated switching-related excursions. This observation should not be confused with proof of tight capacitor-voltage regulation: the source plot includes sharp peaks, and an averaged capacitor-voltage plot or raw data would be needed to quantify ripple and balance. The available simulation also includes a capacitor-current response (Fig. 12).

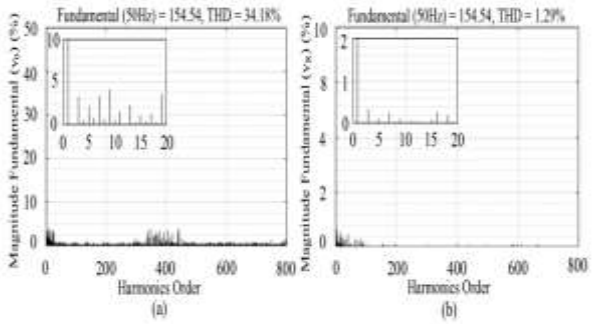


Fig. 12. Experimental Harmonic Spectrum Analysis: (a) Pole Voltage and (b) Resistive Load Voltage.

For a 40 V input, the reported pole voltage exhibits five levels (−200, −100, 0, 100 and 200 V). The source states that the rms leakage current is 10 mA for 50 ohm and 12.8 mA for 30 ohm loading. It also reports a pole-voltage THD of 34.18% and a filtered resistive-load-voltage THD of 1.29%, with a fundamental magnitude of 154.54 V. These figures are not independently recomputed.

A. Interpretation and limitations

The difference between pole and filtered-voltage THD demonstrates the importance of filter placement when reporting harmonic quality. Leakage performance depends on grounding, stray capacitance, switching transitions and measurement bandwidth. The supplied documentation does not provide sufficient raw files to independently verify compliance, uncertainty or loss breakdown.

VIII. DONCUSSION

The main architectural benefit is the integration of boosting and five-level voltage synthesis without a line-frequency transformer. Nine switches provide polarity and level control, while the paired SC capacitors permit intermediate voltage steps. The source reports a continuously conducting input-inductor path and a virtual-ground filtering approach intended to reduce PV leakage.

Important engineering tradeoffs remain. The voltage gain depends on duty ratio and nonideal losses; large startup charging spikes can stress capacitors and devices. A complete design should measure the average and peak capacitor voltages, inductor ripple, semiconductor junction temperatures, leakage under varying PV stray capacitance and power quality across irradiance and load changes.

IX. CONCLUSION

A seven-page technical synthesis of the reduced-capacitance H-9 five-level switched-boost capacitor transformer-less inverter has been presented using the uploaded Aruna documentation. The ideal voltage relations predict a 100 V switched-capacitor voltage and ±200 V peak level at 40 V input and D = 0.6. The supplied simulation figures illustrate input-voltage regulation, current startup, ac waveforms and capacitor behavior. Separately, source-reported prototype measurements describe low leakage currents and 1.29% filtered-voltage THD. Reproduction of these experimental claims requires the original circuit files, control implementation and measurement records.

X. FUTURE WORK

Recommended extensions are soft-start capacitor pre-charging, closed-loop balancing under irradiance variation, detailed switching-loss and thermal modeling, verified grid synchronization, and hardware-in-the-loop tests. Any publication claiming a new improvement should add a distinct control or topology contribution and compare it experimentally against the documented baseline.

REFERENCES

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