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Design and Performance Analysis of a Sigma-Delta Modulator

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ABSTRACT

Analog and digital signals are essential concepts in contemporary electrical engineering. Analog signals are primarily disadvantaged by their inherent susceptibility to noise and distortion, which degrade signal quality during transmission and processing. This vulnerability necessitates their conversion into a more robust digital form before computation and secure storage. This critical conversion is executed by an Analog-to-Digital Converter (ADC). An ADC samples a continuous analog input, typically a voltage or current, and encodes it as a discrete, multi-bit digital value. The precision of this digital output is determined by the resolution of the ADC, which is based on the number of bits used during the conversion process. This project focuses on the design and testing of a sigma-delta analog-to-digital converter. It will analyze the function of each component within the system, detail the testing methods employed, and present the results from both individual component tests and the overall system performance. Sigma-delta converters have gained popularity as an ADC architecture due to their relatively simple design and capability to deliver high-resolution, low-noise conversions. By designing and simulating a basic sigma-delta converter, this project explores key concepts in integrated circuit design, signal processing, and ADC functionality. For an OSR of 512, we obtained a SINAD of 69.78 dB and an ENOB of 11.3.

Keywords: Sigma-Delta Converter, Oversampling Ratio (OSR), Signal-to-Noise and Distortion Ratio (SINAD), Effective Number of Bits (ENOB), Analog Signal Processing, Digital Signal Conversion, High-Resolution ADC, Low-Noise Conversion

1. INTRODUCTION

The process of converting continuous analog signals to discrete digital signals is a central aspect of contemporary electronics, allowing digital systems to handle real-world information. The accuracy of a conversion process carried out by an Analog-to-Digital Converter (ADC) affects the overall functionality of a system directly. Two main operations are involved in a process of this type: sampling and quantization. During the sampling operation, the continuous input signal is sampled at discrete regular time intervals. Then, the quantization operation maps the amplitude of a sample to the closest digital value available.

The sampling rate also establishes the highest signal bandwidth that can be properly recreated, while the resolution, or number of bits, determines the degree of the digital approximation. More resolution means higher fidelity but also requires more memory and processing.

Types of Nyquist rate converters are :

- Flash ADC
- Digital Ramp ADC
- Successive Approximation ADC
- Tracking ADC
- Pipeline ADC

Flash ADC

Flash ADCs, also known as parallel ADCs, use a parallel design that makes them the fastest type of ADC available, which is why they're well-suited for high-bandwidth applications. However, they require a large number of resistor specifically 2^N resistors—which leads to higher power consumption and limits their resolution. This also makes them expensive when used in high- resolution scenarios. Flash ADCs are commonly found in high-frequency applications and often serve as building blocks within other ADC designs like multi-bit sigma-delta and pipeline ADCs. Typical uses for flash ADCs include satellite communication systems, radar signal processing, data acquisition setups, sampling oscilloscopes, and high-density disk drives.

Pipelined ADC

Among the many architectures of data converters, pipelined analog-to-digital converters (ADCs) are a very popular architecture. They are implemented to have resolutions that normally range from 8 to 16 bits, and sampling from a few million samples per second (MSPS) to several hundred MSPS. This mix of high-speed performance and decent accuracy makes the pipelined ADC architecture very efficient for critical applications. Thus, these converters are used extensively in fields such as advanced communications and medical instrumentation, where both of these aspects are critical to system performance. You'll often see pipelined ADCs used in applications such as CCD cameras, digital receivers, ultrasound imaging, base stations, digital video, DSL, cable modems, and fast Ethernet. While pipelined ADCs excel in balancing speed, precision, power use, and overall performance, other types like SAR and integrating ADCs still serve well in scenarios where slower sampling rates are sufficient. For extremely high-speed needs—such as sampling rates around 1 GHz—flash ADCs remain the go-to solution.

Successive Approximation ADC

One of the major benefits of SAR converters is that they have very low power consumption and small die area. Both of these aspects make them very well-suited for power-constrained and space- restricted applications. As a result, they are often used in battery-operated equipment, hand-held instruments, pen digitizers, industrial control units, and data acquisition hardware.
The conversion process of a SAR ADC is similar to a binary search algorithm. It works by comparing the analog i/p voltage to a sequence of internally stored ref voltages in order to produce each bit of the digital output, starting from MSB to LSB. Although this serial operation can be clocked in several megahertz, its serial nature inherently restricts the converter's total throughput as compared to parallel structures such as flash ADCs.

Dual-Slope ADC

Single-slope ADC has a ramp generator, a comparator, and a digital counter. The ramp signal is connected to integrator, which produces a linear rising voltage over time. The last numerical value stored by the counter is proportional to the time it took for the ramp to become equal to the input level and hence it is a digital equivalent of the magnitude of input voltage.In a dual-slope ADC, the input voltage (VIN) is integrated over a set time (TINT), then the process reverses by integrating a known reference voltage (REFV) for a variable period (TDE-INT).

Incorporating analog-to-digital converters (ADCs), e.g., the dual-slope ADC, present unique benefits compared to other time-domain conversion techniques like the digital ramp ADC.

Sigma-Delta ADC

A Sigma-Delta ADC (SDADC) comes under type of oversampling . This oversampling frequency, fN, is given by fN=k2F,where *k* is the oversampling ratio defined as K=fn/F. In this specific implementation, the modulator samples the analog input signal at a frequency that is dictated by the oversampling factor. This procedure converts the analog signal to a pulse density modulated (PDM) output. This PDM signal preserves the original signal information but is also infused with quantization noise outside the desired frequency band.

In order to remove the unwanted noise and recover the clean signal, the modulator output is processed with a decimation filter to eliminate the unwanted noise. The modulator and the decimator are both operated in synchronized mode using the same oversampling clock. The modulator itself is typically a first-order system with a 1-bit quantizer and thus produces a single-bit data stream. Subsequent to filtering and down sampling action of the decimator, this high-rate, 1-bit stream is transformed into a final N-bit digital output. Resolution of this output, represented by N, is directly determined by the oversampling ratio employed in the system.

The following sections briefly explain key ideas like quantization noise, signal sampling, and noise shaping, all of which play an important role in understanding sigma-delta converters.

Quantization Noise

An analog signal can have any value, but when it is changed to digital with n bits, it can only be shown in 2^n steps. The small gap between the real value and the digital value is called quantization noise. This error adds a little distortion and shows how close the digital output is to the actual signal.

Signal Sampling

Oversampling means taking more samples than the Nyquist rate. This helps reduce quantization noise in the range we care about. The sampling theorem says the signal can be rebuilt properly if the sampling rate is at least twice the highest input frequency.

Noise Shaping

Sigma-delta ADCs use feedback to improve performance. The modulator acts like a high-pass filter for noise and a low-pass filter for the input signal. With oversampling, the noise spreads out over a bigger range. The total noise is the same, but the noise in the useful band is much smaller**.**

In a sigma-delta ADC, the input is sampled really fast by the modulator. After that, the signal goes through a digital filter (called a decimator). This filter cuts down noise and removes signals we don't need, so the final output stays clear in the frequency range we want.

Problem Statement

ADCs are used to change real signals into digital form. Normal Nyquist ADCs can struggle with power use, complexity, and resolution, especially for low or mid-band signals like in audio, medical, or communication systems.

Sigma-Delta (ΣΔ) modulators help with this by using oversampling and noise shaping. A first-order ΣΔ modulator gives some noise reduction, but not always enough. A second-order ΣΔ works better since it moves more noise away from the signal, which improves SNR, dynamic range, and overall performance.

Nyquist rate converters face challenges in power & resolution for low band applications , designing a second order sigma delta modulator gives improved snr & performance.

Objectives

To design and implement a difference amplifier, integrator, comparator, and DAC using Cadence. To design the sigma-delta modulator using the designed sub blocks.
To verify the performance parameter.

2. LITERATURE SURVEY

The authors, R. Ganesh Raj, A. Karmakar, and S. C. Bose, present a comprehensive approach to designing a second-order Sigma-Delta modulator tailored specifically for audio ADC applications. Their work emphasizes achieving a high resolution of 16 bits over a 22.05 kHz bandwidth, meeting CD-quality standards. They adopt a top-down design methodology, beginning with behavioral modelling to assess signal ranges before gradually introducing real-world non-idealities such as finite operational amplifier gain, latency, and comparator offset. This careful analysis helps set realistic specifications for each sub-block of the modulator. The individual components are then implemented in 0.35 µm CMOS technology, and the integrated design undergoes rigorous SPICE simulation, which is validated against MATLAB results. The authors highlight that their method allows for a clearer understanding of how various imperfections affect the overall system, rather than relying solely on iterative circuit-level simulations. Their findings indicate that the Sigma-Delta modulator achieves required performance with less demanding design constraints compared to traditional pipeline ADCs, making it a promising candidate for audio front-ends in CODECs and hearing aids. Moreover, the design's scalability suggests potential extensions into higher-order modulators suitable for precise instrumentation applications[1].

The authors Archana Parutabadia and Channakka L. have explored the development of a Sigma- Delta modulator using 0.18µm CMOS process technology for efficient analog-to-digital conversion. This project is about building a first-order, 1-bit sigma-delta modulator. The design was made and tested in Cadence software using a 1.8 V supply. The results show that this type of modulator can be more stable and energy-efficient than regular ADCs. Because it uses oversampling and noise shaping, the circuit stays simple but still gives accurate signal conversion. The simulations also show low power use and a small chip area, which makes it a good fit for modern integrated circuits. The modulator works well at around 2 MHz, so it can be used in audio processing, communication systems, and digital signal processing [2].

The authors P. Shivani and Md. Misbahuddin has put forward a design methodology for low-pass continuous-time Sigma-Delta modulators, highlighting their importance in improving analog-to-digital conversion for systems. As the demand for high-speed and high-resolution ADCs grows in advanced digital signal processing applications, this research tackles the challenges posed by limited dynamic range in scaled technologies. The suggested continuous-time Sigma-Delta modulator presents an effective solution by leveraging oversampling and noise shaping to achieve impressive accuracy while relying less on exact analog components. This study introduces a fresh perspective on analyzing and synthesizing modulators through discrete-time approximations, which helps steer the design of continuous-time implementations. It explores various orders of modulators—from first to fifth—deriving transfer functions like STF and NTF for each to ensure optimal frequency response and signal integrity. A first-order low-pass modulator with a 20 kHz bandwidth was validated through thorough simulations using MATLAB and Cadence tools. The research places special emphasis on system-level parameters and loop filter design, which are recognized as critical constraints in these architectures. Overall, this study offers valuable insights into the practical development of low-power, high-performance ADCs that are well-suited for embedded and communication systems [3].

The authors M. Kavitha, S. Akhila, and Anand Kannan suggested a high-resolution continuous-time sigma-delta modulator (CT-ΣΔM) which is particularly intended for high-resolution ECG signal acquisition. The authors' research focuses on the urgent requirement of low-power but highly accurate analog front-end circuits used in contemporary devices for constant patient monitoring. An 180 nm CMOS technology-based Cascade of Integrators Feed-Forward (CIFF) architecture was adopted that utilized a single-bit quantizer to achieve decreased power usage and design complexity. The suggested modulator efficiently realized an outstanding Effective Number of Bits (ENOB) of 17.06 and a Signal-to-Noise and Distortion Ratio (SINAD) of 104.5 dB. In contrast to traditional solutions that may

sacrifice performance for power, this design achieved a significant 10% improvement in important metrics and utilized a mere 24µW of power. This achievement demonstrates the strength of applying active-RC integrators and a resistive feedback DAC in order to suppress noise and reduce power dissipation all at once. The research emphases that a sequential design flow, ranging from theoretical coefficient generation to pragmatic circuit-level scaling, is crucial for the achievement of high-performance data converters. Finally, their research offers a strong framework for designing energy-efficient modulators appropriate for high-end biomedical applications [4].

Sumit Kale presents a thoughtful design of a first-order Sigma-Delta modulator aimed at delivering high-resolution analog-to-digital conversion while keeping power usage low. Built using 0.5-micron CMOS technology and designed with the Tanner suite, the modulator features a two-stage operational amplifier with a strong DC gain of 70 dB. Operating with an oversampling ratio of 256 and powered by a ±2.5 V dual supply, it achieves a resolution of 10 bits, making it suitable for precise signal processing tasks. Important parts of the design include a 1-bit DAC made with transmission gates and resistors, along with a positive edge-triggered D flip-flop, which together help maintain simplicity and reliable operation. Simulations carried out with S-Edit and W-Edit tools show the design reaching an SNR of 86.04 dB while consuming only 6.8 mW of power, highlighting its energy efficiency. The op-amp in the integrator stage is especially power-conscious, drawing just 0.685 mW, which makes this modulator well-suited for portable and embedded applications. This project shows that by tweaking the analog parts and adjusting the power supply, it's possible to build an ADC that works well without using too much power. In simple terms, the design gives a useful way for engineers to get both accuracy and energy savings in mixed-signal circuits [5].

Jayendra Sikarwar and R. C. Gurjar worked on a low-cost design for a first-order Sigma-Delta modulator, mainly for biomedical sensors. The circuit is built using 0.18 µm CMOS technology and is meant to handle weak body signals that normal ADCs often struggle with. It has a narrowband design, runs on a 1.8 V supply, and was developed and tested in Cadence. Using a 1-bit quantizer, the system stays stable and reliable, making it a good fit for low-frequency biomedical signals. It operates at an input signal frequency of 1 kHz with an oversampling frequency of 250 kHz, achieving an oversampling ratio (OSR) of 250. The simulation results indicate a signal-to-noise ratio (SNR) of 68.79 dB, which supports its effectiveness in high-resolution signal acquisition. Compared to traditional ADCs, the Sigma-Delta architecture showed superior performance in capturing weak analog inputs without significant noise interference. This work highlights the potential of low-cost, high-accuracy Σ-Δ modulators in portable health monitoring systems and other low-power applications [6].

Thiago Brito Bezerra, Mauro Lopes de Freitas, and Waldir Sabino da Silva Júnior have explored the functional advantages and architectural simplicity of Sigma-Delta analog-to-digital converters (ADCs) in the context of modern VLSI applications. Their study addresses the limitations of conventional ADCs, which often demand highly precise analog components and are more susceptible to noise and circuit non-idealities. Sigma-Delta converters, by contrast, offer an effective alternative due to their tolerance to imperfections and the ease of digital implementation. The authors analyze the internal working of Sigma-Delta ADCs through both theoretical discussion and simulation results using Simulink and Multisim platforms. Their findings confirm that these converters achieve improved signal-to-noise ratios and faster analog-to-digital conversion speeds, even in the presence of hardware limitations. Emphasis is

placed on the rising significance of Sigma- Delta architectures with the evolution of VLSI technologies, which now allow for their compact and efficient integration into digital systems. The paper highlights how the renewed interest in Sigma-Delta modulation is aligned with the broader industry shift toward high-resolution and noise-resilient data acquisition. Overall, this work reinforces the relevance of Sigma-Delta ADCs in modern electronic design, especially where accuracy and simplicity are critical [7].

Saurabh Chandra Pandey, Pritesh Mishra, Rahul Roy, and Amit Kant Pandit propose a two-stage CMOS operational amplifier (op-amp) tailored for integration within Sigma-Delta analog-to-digital converters. Crafted with 180 nm CMOS technology and powered by a ±1.8 V supply, this amplifier is designed to meet the high-performance needs of precision ADC applications. It features Miller compensation to maintain stability and a broad bandwidth, achieving an impressive unity-gain frequency of 18.2 MHz and an open-loop gain of 71.27 dB. Developed and tested using the Cadence Custom IC design suite, this op-amp demonstrates excellent results in terms of gain-bandwidth product and power efficiency. Throughout the design process, the authors carefully considered key factors like transistor sizing, bias currents, and compensation strategies to fine-tune the amplifier's performance. They conducted thorough simulations and aspect ratio analyses to ensure the circuit performs well under various operating conditions. This study sheds light on how deliberate architectural decisions and process-level adjustments can significantly enhance analog front-end performance. In the end, this work presents a solid op-amp design that's perfectly suited for low- power, high-accuracy Sigma-Delta ADC systems [8].

The authors Nadeem Tariq Beigh et al. proposed a system-level simulation and design of a second- order sigma-delta modulator. Their work was specifically aimed at designing a high-resolution converter for low-power and low-frequency applications, including the recording of brain wave signals. With the aid of the Delta Sigma Toolbox in Simulink, the team emphasized optimizing and scaling the modulator coefficients to optimize overall performance. The ensuing block-level design was able to realize an astonishing Effective Number of Bits (ENOB) of about 16 bits and a Signal- to-Noise-and-Distortion Ratio (SNDR) of 96 dB.Compared to a direct circuit-level implementation, the proposed high-level modeling methodology facilitates easy optimization of the system's basic parameters prior to physical design. This achievement proves the value of simulation tools in creating a solid framework and predicting the performance of the ultimate integrated circuit. The work is confirmed by the research to be an excellent choice for precision biomedical devices that process signals in an extremely low bandwidth. Finally, the work gives a fundamental and verified basis, specifying the capacitor ratios required for a following switched-capacitor implementation on 0.18µm CMOS technology [9].

Dr. Sreelal S. and Jose J. Edathala worked on a simulation method to test how a first-order Sigma- Delta ADC performs. Their design handles signals up to 24 kHz, with an oversampling ratio of 64 and a sampling rate of 3.07 MHz. What makes their approach interesting is that they used both MATLAB and Excel to model the analog part of the modulator, while also building a custom digital backend with an FIR decimation filter. This setup gave them a clear picture of how the analog and digital parts affect the whole system. By combining these tools, they created a flexible way to check design trade-offs before moving to real hardware. They also suggest trying higher-order modulators and better digital filters in the future to improve Sigma-Delta ADC performance even more [10].

The researchers Nandini Sahu and Aparna Karwal reported the design and performance evaluation of a first-order single-bit sigma-delta modulator. Their focus was on designing a very low-power consumption and small-sized converter with a state-of-the-art 90nm CMOS process. One key aspect of their approach was to utilize a lower-gain amplifier intentionally, which was a trade-off done to minimize the total

power budget considerably. Running from a 1.2V supply, this topology was able to successfully achieve an extremely low power dissipation of 26.56 µW and an SNR value of 43 dB. As opposed to more robust differential implementations, this single-ended topology was particularly optimized for basic applications in which minimal area and power are the most significant constraints. This result clearly illustrates how relaxing amplifier gain specifications can be a very effective method for realizing significant power savings in power-constrained designs [11].

Deepak Prasad and Vijay Nath, in their paper, introduce the CMOS difference amplifier design, a key component of Sigma-Delta ADCs, aimed specifically at aerospace use. The authors highlight ultra-low power consumption as an important concern in modern-day CMOS circuits and the demand for high-gain operational amplifier to provide accurate differential amplification.The final design was realized utilizing 90nm UMC CMOS technology within Cadence Virtuoso. The circuit contains an operational amplifier that registers an open-loop gain of 48.45 dB, which is measured for operation from a ±1.3 V dual power supply. This amplifier is designed to provide an output signal that reflect the difference between its two inputs with high accuracy, which is a precondition of the correct operation of the Sigma-Delta ADC system. Simulation results show the circuit delivers stable output and reliable performance for both the operational amplifier and the difference amplifier stages. This study highlights the promise of developing efficient, stable analog building blocks for Sigma-Delta ADCs in power-sensitive aerospace applications and provides useful insights into designing low-power mixed-signal circuits [12].

3. SIGMA DELTA MODULATOR

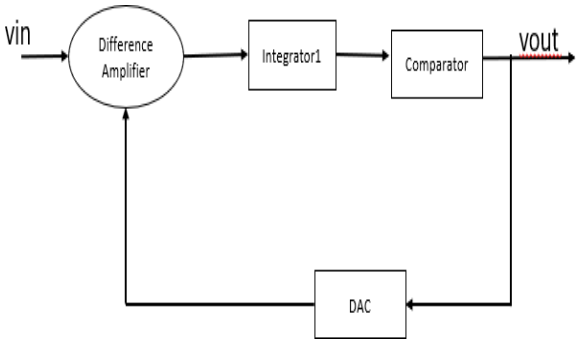

Fig 1:First order sigma delta modulator

The operation of the sigma-delta system starts with a difference amplifier, which is responsible for calculating the difference between its two inputs. In this setup, the amplifier takes the original input signal at its non-inverting terminal, while the DAC's output is connected to the inverting terminal. By subtracting the DAC feedback from the input, the amplifier produces a cleaner voltage signal, which is then passed on to the integrator stage for further processing.

After the comparator, the circuit uses a feedback loop with a 1-bit DAC. The DAC changes the comparator's digital output (0 V or 5 V) back into an analog signal and feeds it into the difference amplifier. This feedback helps cut down noise and keeps the signal steady, making the conversion more accurate and reliable.

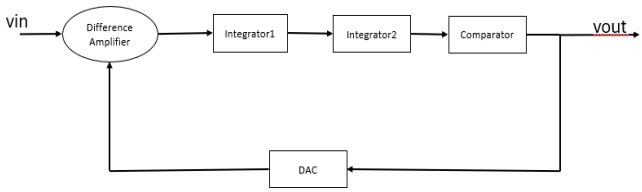

Fig 2: Second order sigma delta modulator

The process starts with the difference amplifier, which compares the input signal (Vin) with the feedback from the DAC. It give an error signal by finding the difference between them.

The error signal is then filtered through a cascade of two integrators. The initial integrator sums the error signal, beginning the noise-shaping process by reducing low-frequency signal components. Its output is then input to the second integrator, which integrates once again. This two-stage integration is essential to the second-order response of the modulator, as it

aggressively shapes the quantization noise, effectively displacing it to higher frequencies well beyond the signal band of interest.

After the stages of integration, the signal is applied to a 1-bit quantizer. The quantizer converts the signal to digital. Although this step adds heavy quantization noise, the previous integrator stages make this noise spectrally shaped.

This 1-bit digital output is subsequently digitized back into a 1-bit analog signal by a digital-to- analog converter (DAC). The analog representation is returned to the input of the difference amplifier, closing the negative feedback loop. This closed-loop system auto-adjusts in real time, compelling the average output of the quantizer to follow the average input voltage, dynamically reducing quantization error during the conversion process.

4. IMPLEMENTATION OF PROPOSED SYSTEM

The second order sigma delta modulator consists of different blocks like difference amplifier , integrator, comparator and dac. The design of each blocks is given below.

OPAMP

An Operational Amplifier (Op-Amp) is a high-gain, direct current (DC) coupled voltage amplifier that features a differential input and generally a single-ended output. Op-Amps serve as essential components in analog electronics and find extensive use in various applications, like signal amplification, filtering, voltage comparison, and carrying out arithmetic operations like addition, subtraction, integration, and differentiation.

Initially, Op-Amps were developed to conduct mathematical operations within analog computers, which is why they are referred to as "operational." Their versatility, simplicity, and capability to amplify weak signals accurately have made them vital in contemporary electronic circuits.

Difference Amplifier

The difference amplifier is a highly adaptable circuit used in Sigma delta ADCs. One terminal receives the analog input signal while the other terminal is connected to the feedback loop from the DAC output. Essentially, it functions as a difference amplifier with one resistor at the input and a network of resistors in the feedback loop. The circuit is built in 45nm technology. An input voltage of 1.8V is applied to the difference amplifier, and the output will represent the difference between the input voltage and the feedback voltage.

Integrator

The integrator utilizes a two-stage operational amplifier, designed in the Cadence Virtuoso environment with 45nm CMOS technology, and features a feedback capacitor that aids in charging the input voltage to produce an integrated output. A sinusoidal input signal is provided from the difference amplifier, which computes the difference in the input and the feedback signal, resulting in an output that corresponds to the given sinusoidal input.

Comparator

Comparator is one of the core components in the sigma delta modulator. It compares the two input signals and gives the digital output. Comparator block is created using the Verilog A code. Fig 4.5 shows the working of Verilog code of comparator .

DAC

A 1-bit digital-to-analog converter (DAC) plays a crucial role in the feedback loop of a sigma-delta converter. The sigma-delta modulator creates a high-frequency bit stream that indicates the analog input signal, while the low-resolution DAC translates this bit stream back into an analog output. This reconstructed analog signal is then compared to the original input signal by the differential amplifier. The feedback loop guarantees that the converter's output closely matches the input signal, providing high resolution and minimal distortion. The performance of the sigma-delta converter is partly influenced by

the dynamic range of the DAC, which must exhibit good linearity, low noise, and fast settling time to ensure high-speed and high-performance operation.

Sigma delta ADC

Sub blocks like difference amplifier , integrator , comparator, DAC are designed in Cadence Virtuoso, by combining all these blocks a second order sigma delta modulator is realized.

5. RESULTS

Difference Amplifier

One terminal receives the analog input signal while the other terminal is connected to the feedback loop from the DAC output. Essentially, it functions as a difference amplifier with one resistor at the input and a network of resistors in the feedback loop.

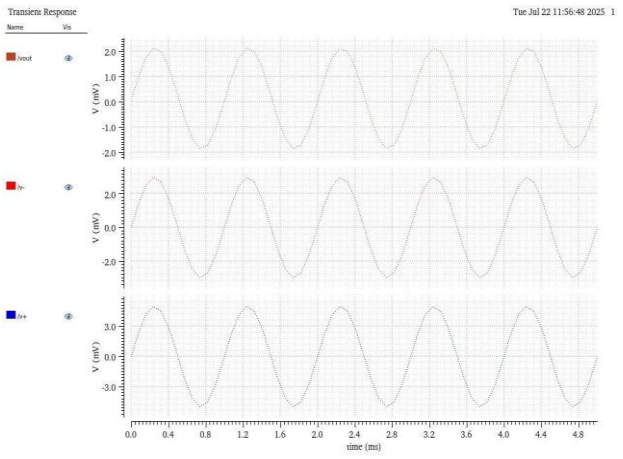

Fig 3: Simulation waveform of difference amplifier

Integrator

The integrator utilizes a two-stage operational amplifier, designed in the Cadence Virtuoso environment with 45nm CMOS technology, and features a feedback capacitor that aids in charging the input voltage to produce an integrated output. A sinusoidal input signal is provided from the difference amplifier, which computes the difference in the input and the feedback signal, resulting in an output that corresponds to the given sinusoidal input.

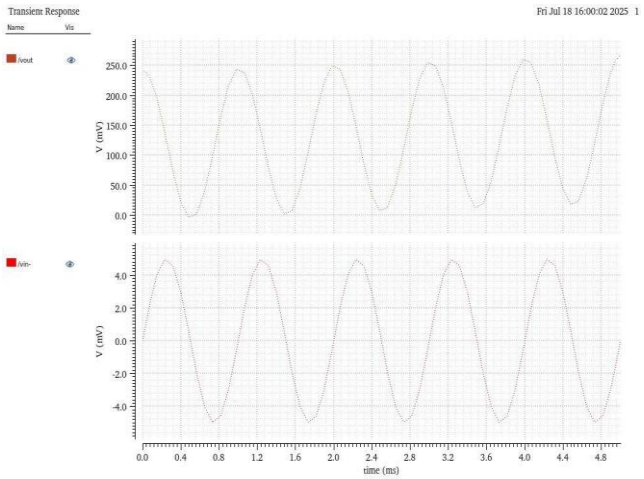

Fig 4: Simulation waveform of integrator

Comparator

Comparator compares the input signal with reference and based on that it gives the output of either 0 or 1. If input is greater than reference it gives 1 else it gives 0.

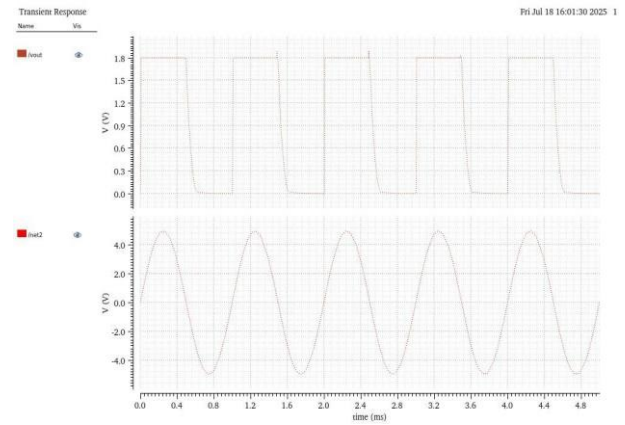

Fig 5: Simulation waveform of comparator

DAC

The sigma-delta modulator creates a high-frequency bit stream that indicates the analog input signal, while the low-resolution DAC translates this bit stream back into an analog output. This reconstructed analog signal is then compared to the original input signal by the differential amplifier. The feedback

loop guarantees that the converter's output closely matches the input signal, providing high resolution and minimal distortion.

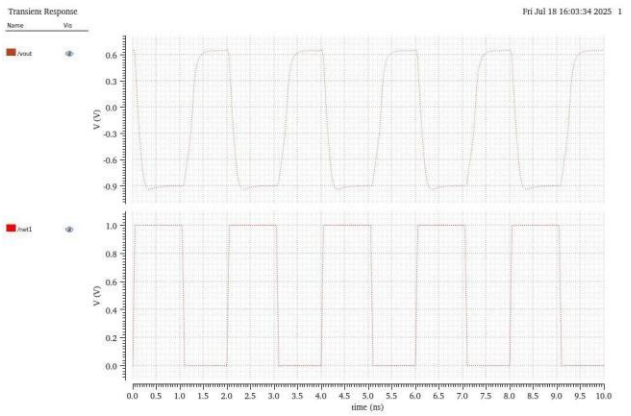

Fig 6: Simulation waveform of DAC

Sigma Delta Modulator

Difference amplifier calculates the difference between input and the dac output and gives the output

, that output is given to 2 integrators which smooths the signal, after that the output of 2nd integrator is given to comparator which converts analog signal to digital signal , this digital signal is then given to dac as input which converts it back to analog signal and given to difference amplifier.

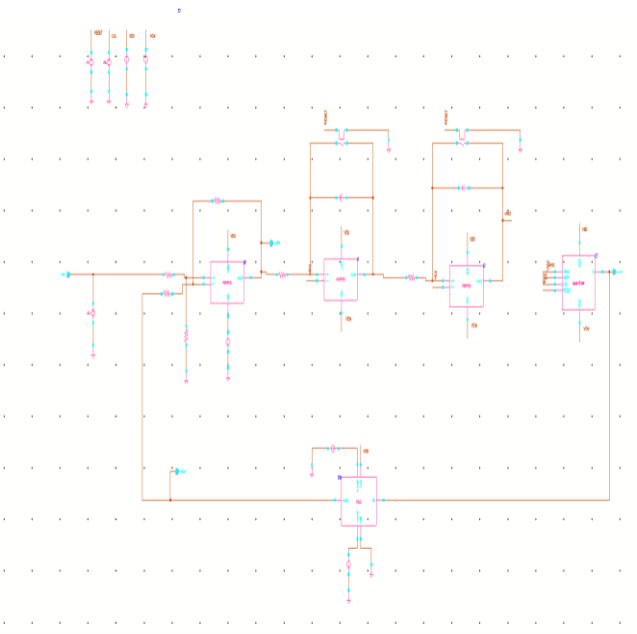

Fig7: Schematic of 2nd order sigma delta modulator

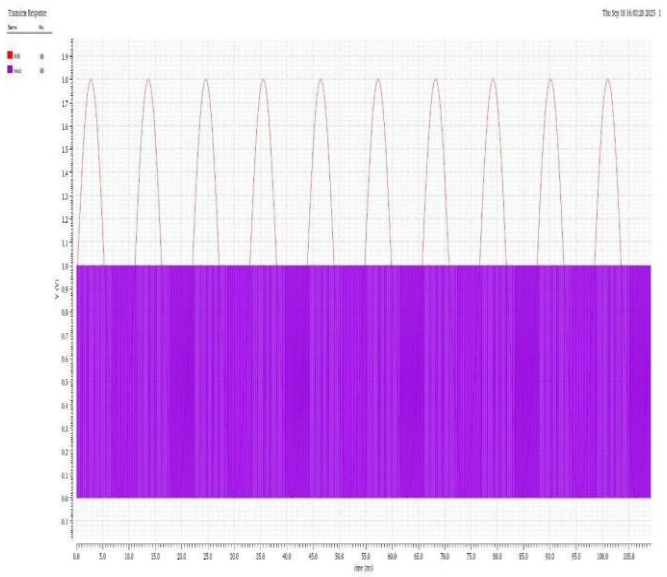

Fig 8: Simulation waveform of 2nd order sigma delta modulator

6. CONCLUSION AND FUTURE SCOPE

CONCLUSION

A second-order Sigma-Delta modulator was implemented using 45nm CMOS technology in Cadence Virtuoso. The design operates with a supply voltage of 1.8V and uses an oversampling ratio (OSR) of 512. With a signal bandwidth of 250 Hz and a sampling frequency of 256 kHz, the modulator achieves a Signal-to-Noise Ratio (SNR) of approximately 69.78 dB. This corresponds to an Effective Number of Bits (ENOB) of around 11.3.

FUTURE SCOPE

The future scope includes several key areas of development and optimization. One major direction is the design of an efficient decimation filter. Another important aspect is the layout implementation and post-layout simulations. Furthermore, the design of a multibit sigma-delta ADC presents a promising area for future research, as multibit architectures can improve resolution, reduce quantization noise, and enhance linearity while maintaining stability. Overall, these advancements can lead to higher performance, lower power consumption, and more robust sigma-delta ADC systems suitable for a wide range of precision signal processing applications.

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