International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 09 Issue: 12 | Dec - 2025 SJIF Rating: 8.586 ISSN: 2582-3930

Design and Performance Analysis of an 8-Bit Approximate Multiplier Using Single Exact Single Approximate Adders and Single Exact Dual Approximate Adders

K.S.M. Pavan[1], Attada Sridhar[2], T. Chadra Guptha[3], G.M. Peela[4]
[1]P.G Scholor, Sri Venkateswara College of Engineering & Technology, Sikakulam, India
[2,3,4] Assistant Professor, Sri Venkateswara College of Engineering & Technology, Sikakulam, India
sridhar472@gmail.com

Abstract: Adders form the core arithmetic building blocks in digital Very Large Scale Integration (VLSI) systems. In recent years, approximate adder designs have gained significant attention as an effective approach to optimize key performance metrics such as power consumption, delay, and hardware complexity. Similarly, digital multipliers are essential components in many digital signal processing (DSP) applications and typically dominate the overall computational cost. Since a wide range of DSP applications can tolerate a certain degree of computational inaccuracy, approximate multiplication emerges as a viable solution to achieve favorable trade-offs among energy efficiency, performance, and accuracy, particularly in energy-constrained computing environments. Additionally, supply voltage scaling has been demonstrated as an efficient technique to further reduce total energy consumption. In this work, a multiplexer-based approximate full adder is introduced and employed in the design of an 8-bit approximate multiplier. The proposed circuit architecture enables error-resilient multiplication while operating at a reduced supply voltage. Simulation results demonstrate that the proposed 8-bit approximate multiplier achieves the lowest energy consumption per operation while maintaining comparable computational accuracy relative to existing multiplier designs for 8-bit operands. Furthermore, the proposed design achieves a 26.7% reduction in energy–delay product (EDP) when compared with conventional exact multiplication architectures.

Keywords- Exact Adder, Approximate Adder, Hybrid Adder Architecture, Approximate Multiplier, Power Consumption, Propagation Delay

I. INTRODUCTION

Recent advances in adder circuit design have significantly improved computational efficiency, leading to enhanced performance and improved output quality [1]. Among modern design paradigms, approximate computing has emerged as an effective and resource-efficient approach [2]. This technique has been widely adopted in error-tolerant applications such as computer vision, data mining, deep neural networks, and image and video processing [3], [4]. Approximate computing deliberately relaxes computational accuracy to a controlled extent in order to satisfy stringent energy and performance constraints while maintaining acceptable output quality.

Digital multipliers are fundamental arithmetic components that strongly influence the overall performance of digital systems. A high-speed multiplier typically consists of three major stages: partial product generation, partial product reduction using a compression tree, and a final carry-propagation adder (CPA). Among these stages, the compression tree dominates the design in terms of silicon area, propagation delay, and power consumption. Consequently, the development of energy-efficient compressor structures is critical for low-power multiplier architectures. In compression trees, partial products are accumulated using two-operand adders implemented as full adders, commonly referred to SEDA. Compared to conventional full adders, approximate compressors offer higher reduction efficiency and are therefore extensively employed in partial product reduction networks.

In the context of approximate multiplier design, several 8-bit approximate compressor architectures have been proposed to improve energy efficiency [3]–[6]. For instance, the approach presented in [5] eliminates carry propagation paths between compressors at the same reduction stage, significantly reducing hardware complexity but at the cost of increased error rates and degraded computational accuracy. To address this limitation, this paper introduces a multiplexer-based approximate adder driven 4-2 compressor that incorporates a complementary error compensation strategy. The proposed design achieves reduced logic complexity while maintaining acceptable accuracy. Furthermore, the circuits are implemented using a low supply voltage to further enhance overall energy efficiency.

2. EXISTING TECHNIQUES

2.1 SESA1 ADDER

In SESA1 adder, we introduce approximation in the SUM output by making it to be equal to the complement of CARRY. As seen from Table, SESA1 adder has errors in SUM bits for input combinations 000 and 111. The CARRY output remains same irrespective of whether SESA1 adder operates in exact or approximate mode. In exact mode, the SUM output is computed using a power gated (PG) controlled inverter whose input is the complement of SUM. In approximate mode, the SUM module is PG, and the approximate output which is made equal to the complement of CARRY is generated using another PG-controlled inverter whose input is connected to the complement of CARRY as shown in Figure.

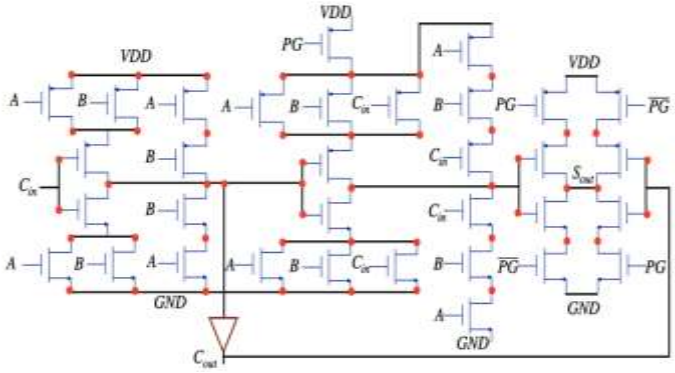

Figure 1: Circuit diagram of SESA1 adder

2.2 SESA2 ADDER

In SESA2 adder, we introduce approximation in the SUM output by making it 0 for all the input combinations as shown in Table for approximate mode.

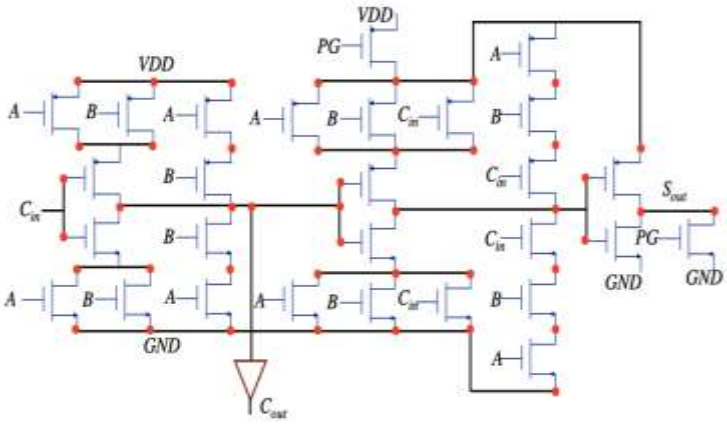

Figure 2: Circuit diagram of SESA2 adder

As a result of this, SESA2 adder has errors in SUM bits for input combinations 001, 010, 100, and 111. The CARRY output remains same irrespective of whether SESA2 adder operates in exact or approximate mode. In exact mode, the SUM output is computed using the normal SUM module. In approximate mode, the SUM module is PG and the approximate output which is equal to 0 is generated using a PG-controlled NMOS that pulls down the SUM output to a 0 as shown in Figure.

2.3 SESA3 ADDER

In SESA3 adder, we introduce approximation in the SUM output by making it 1 for all the input combinations as shown in Table II. As a result of this, SESA3 adder has errors in SUM bits for input combinations 000, 011, 101, and 110. The CARRY output remains same irrespective of whether SESA3 adder operates in exact or approximate mode. In exact mode, the SUM output is computed using the normal SUM module. In approximate mode, the SUM module is PG and the approximate output which is equal to 1 is generated using a PG-controlled NMOS that pulls down the complement of SUM to a permanent 0. Since this is connected to an inverter, we get the SUM output in approximate mode to be a 1 as shown in Figure.

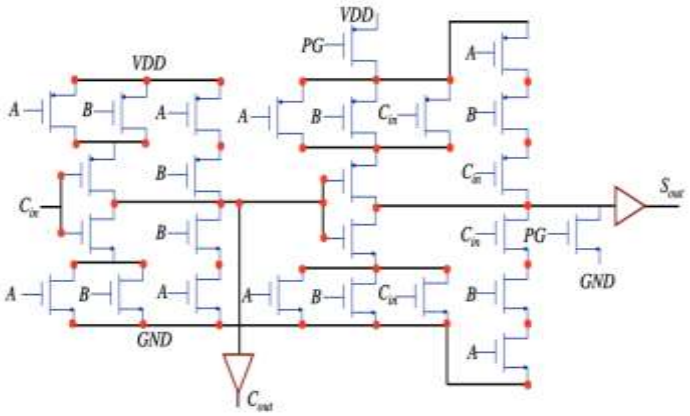

Figure 3: Circuit diagram of SESA3 adder

3. PROPOSED WORK

3.1 SEDA ADDER

The SEDA adders surpasses the SESA adder in terms of advancement. Additionally, it possesses a maximum limit on the potential inaccuracy and offers the possibility to be customized. In contrast to SESA adders, which are limited to performing only one approximate addition, SEDA adders have the capability to do two approximate additions when operating in approximation mode. In the framework of SESA, we implement power gating for the SUM module of the adder, particularly when it is used in approximation mode. This is done in order to ensure safety and efficiency. Additionally, the SUM module is utilized within the SEDA adder in order to generate an extra CARRY.

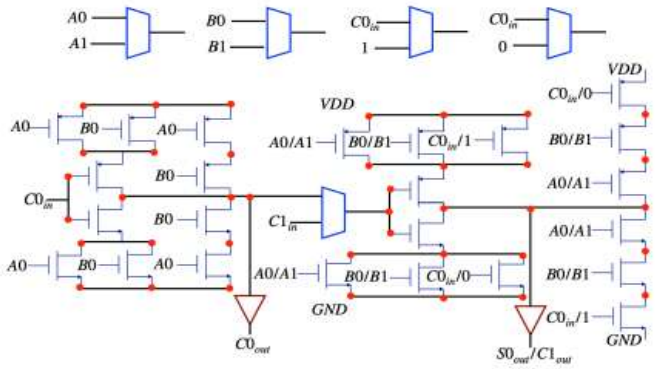

Figure 4: Circuit diagram of SEDA adder

3.2 8-Bit Approximate Multiplier

The number of stages of the proposed multiplier is one stage less than that of the former. At the last stage of the proposed multiplier, in order to obtain the summation of the three remaining rows of partial product, an especial CPA is used which was constructed by some half adders and some proposed approximate compressors. In each of the columns 2 and 15 of this CPA, a half adder is used, and in each of the columns 3 to 14, the first proposed compressor is used. Indeed, columns 3-14 of this CPA is our proposed CPA introduced in the previous sub-section which does not have the carry propagate delay problem

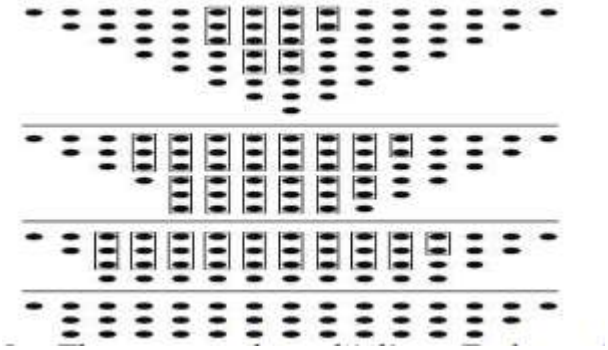

Figure 5: Approximate Multiplier

The proposed multiplier shown each rectangle represents a half adder or a full adder. Sum of the last stage's columns are computed using a CPA which is constructed by some half adders, full-adders, and proposed 4:2 compressors.

4. SIMULATION RESULTS

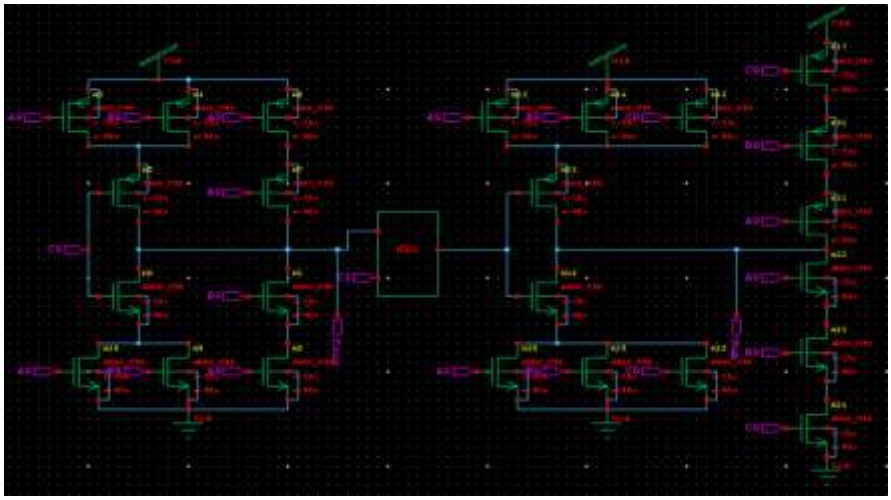

Figure 6: SEDA Schematic Diagram

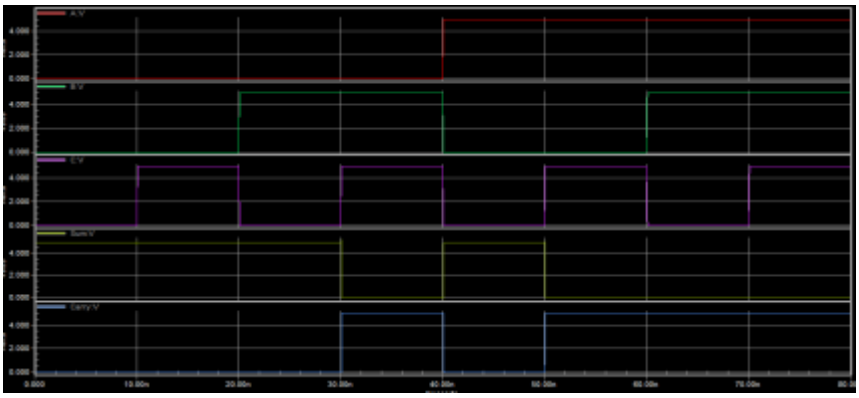

Figure 7: SEDA Output Waveform

6.2. SEDA Based Approximate Multiplier

SESA1, SESA2, SESA3, and SEDA, at a process technology of 90 nanometers, simulations were performed on three approximate mirror adders as well as the proposed multiplexer approximate adder. Specifically, the ratio of Wn to Ln was 2:1, while the ratio of Wp to Lp was 3:1. Through the use of the Tanner EDA tool, a power supply of 1V was supplied and simulated over a period of 500 nanoseconds. This was accomplished by applying the same input patterns to the complete adders. A comparison of the power and the propagation delay was made in Table 6.1, which was tabulated after being measured.

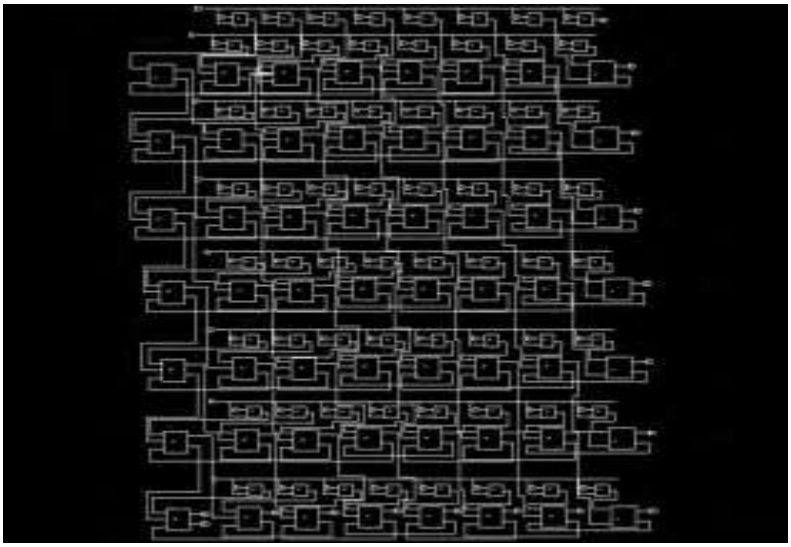

Figure 9: SEDA Based 8 Bit Approximate Multiplier Schematic Diagram

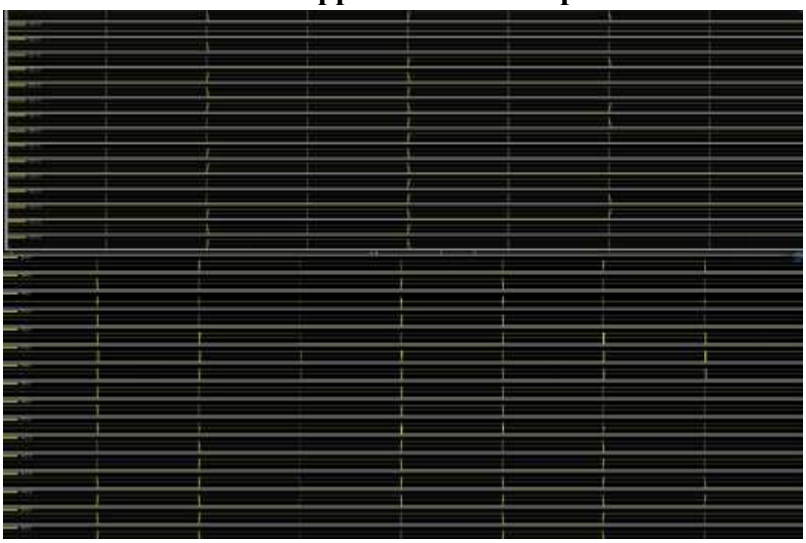

Figure 10: SEDA Based 8 Bit Approximate Multiplier Output waveform

Table 6.1 Comparison of Different Approximate Adders with SESA and SEDA

Design	Power (µW)	Delay (ps)	PDP ($Ws*10^{-18}$)	No. of Transistors
SESA 1	14.7	59.0	867.3	33
SESA 2	13.3	58.1	772.73	28
SESA 3	13.4	58.7	786.58	26
SEDA	18.7	38.4	718.08	28

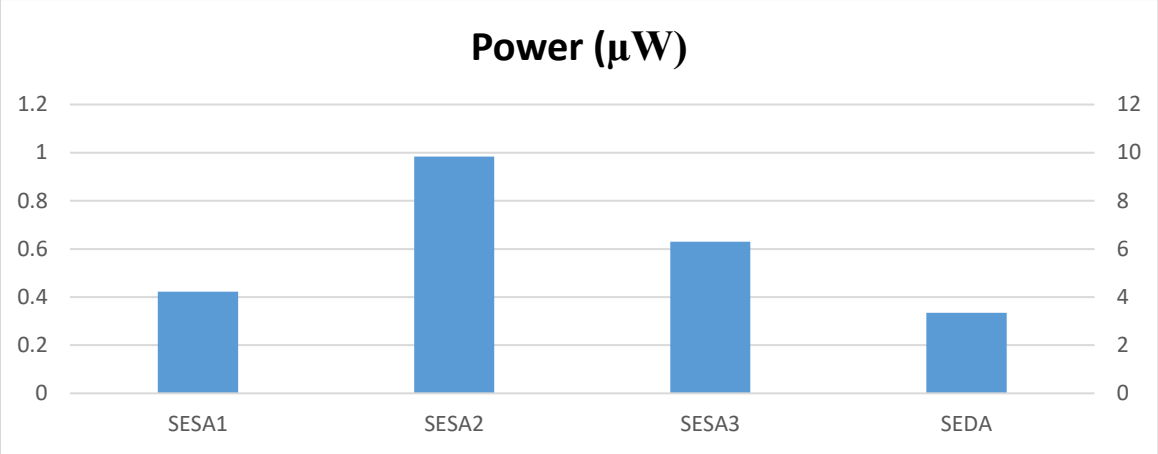

Figure 11. Power Comparison of Different Approximate Adders with SESA and SEDA

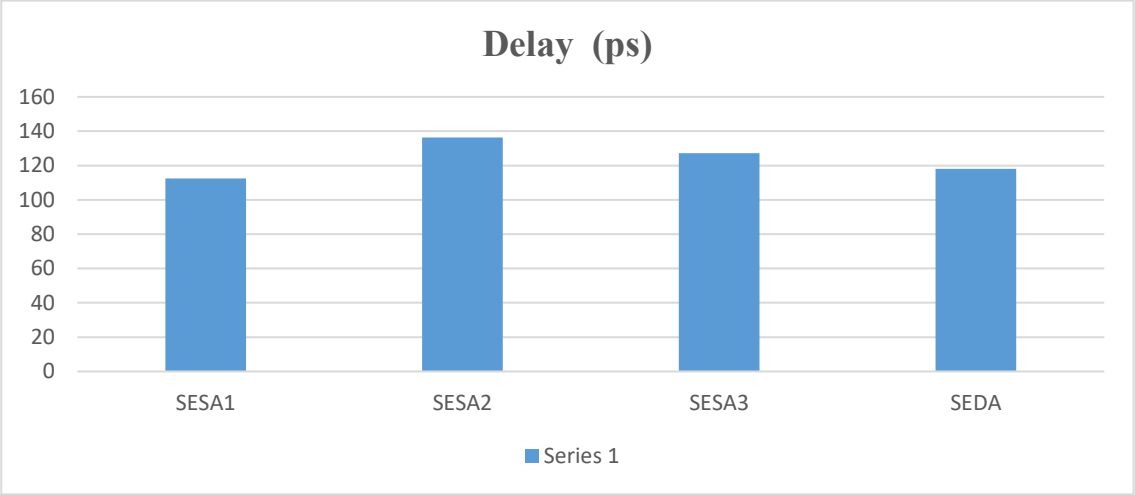

Figure 12. Delay Comparison of Different Approximate Adders with SESA and SEDA

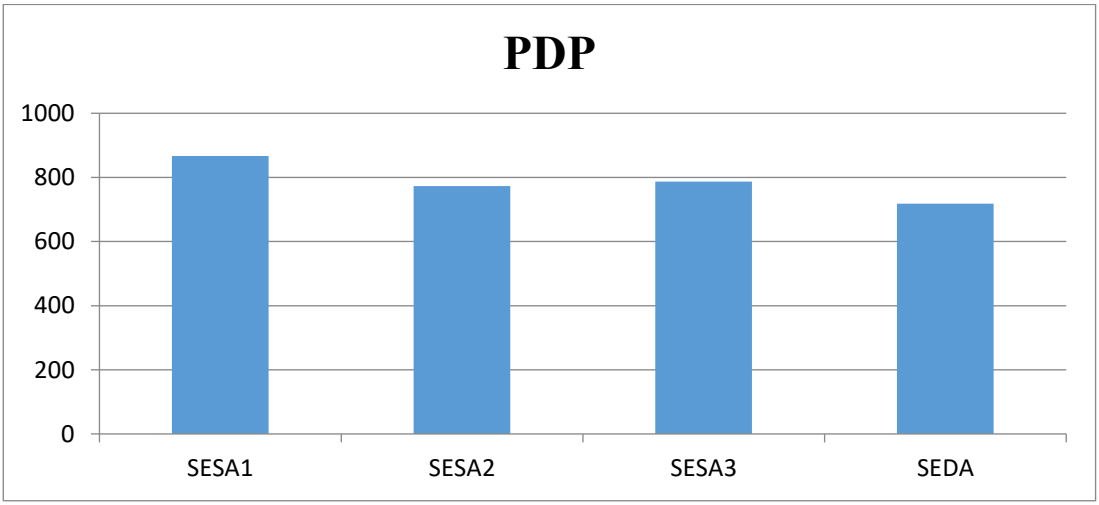

Figure 6.11 PDP Comparison of Different Approximate Adders with SESA and SEDA

5. CONCLUSION

This work presented an energy-efficient 8-bit approximate multiplier architecture based on a multiplexer-based approximate adder by using SEDA. By leveraging the inherent error tolerance of many DSP and multimedia applications, the proposed approach effectively reduces logic complexity, power consumption, and propagation delay without significantly compromising computational accuracy. The introduction of a complementary error strategy ensures that the approximation-induced errors remain within acceptable bounds while achieving

meaningful hardware simplification. Comprehensive simulation results demonstrate that the proposed approximate multiplier outperforms conventional exact and existing approximate designs in terms of energy efficiency when operating at a reduced supply voltage. In particular, the design achieves a substantial reduction in energy per operation and a 26.7% improvement in energy–delay product compared to exact multiplication, while maintaining comparable accuracy for 8-bit operands. These results confirm that the proposed architecture is well suited for error-resilient, low-power VLSI systems such as image processing, neural networks, and other approximate computing applications. Future work may extend this design

REFERENCE

1.Q. Xu, T. Mytkowicz, and N. S. Kim, “Approximate computing: A survey,” IEEE Des. Test, vol. 33, no. 1, pp. 8–22, Feb. 2016.

2.C.-H. Chang, J. Gu, and M. Zhang, “Ultra low-voltage low- power CMOS 4-2 and 5-2 compressors for fast arithmetic circuits,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 51, no. 10, pp. 1985–1997, Oct. 2004.

3.A. Momeni, J. Han, P. Montuschi and F. Lombardi. “Design and Analysis of Approximate Compressors for Multiplication,” IEEE Trans. Comput., vol.64, no.4, pp. 984-994, Apr. 2015.

4.L. Qian, C. Wang, W. Liu, F. Lombardi and J. Han, "Design and evaluation of an approximate Wallace-Booth multiplier," 2016 IEEE Int. Symp. Circuits Syst. (ISCAS), Montreal, QC, 2016, pp. 1974-1977.

5.Z. Yang, J. Han and F. Lombardi. “Approximate compressor for error resilient multiplier design,” IEEE Int. Symp. On Defect Fault Tolerance in VLSI and Nano. Syst., MA, USA, Oct. 2015.

6.S. Venkatachalam and S.-B. Ko, “Design of power and area efficient approximate multipliers,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 25, no. 5, pp. 1782–1786, May 2017.

7.J. Jun, J. Song and C. Kim, "A Near-Threshold Voltage Oriented Digital Cell Library for High-Energy Efficiency and Optimized Performance in 65nm CMOS Process," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 65, no. 5, pp. 1567-1580, May 2018.

8.M. Aliotto, “Ultra-Low Power VLSI Circuit Design Demystified and Explained: A Tutorial,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 59, no. 1, pp. 3–29, January 2012.

9.Z. Zhang, Y. He, “A Low Error Energy-Efficient Fixed-Width Booth Multiplier with Sign-Digit-Based Conditional Probability Estimation,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 65, no. 2, pp. 236–240, May. 2017.

10. V. Garofalo, N. Petra and E. Napoli, "Analytical Calculation of the Maximum Error for a Family of Truncated Multipliers Providing Minimum Mean Square Error," IEEE Trans. Comput., vol. 60, no. 9, pp. 1366-1371, Sept. 2011.) Systems, pp. 566-581, 2002.