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# Design and Performance Analysis of Low Power 6T SRAM Cell in 45nm CMOS Technology

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**Abstract** - This project presents the design and analysis of a low power 6-transistor (6T) SRAM cell using 45nm CMOS technology. SRAM is an important memory used in processors and embedded systems. With technology scaling to 45nm, reducing power consumption and delay is essential, especially for battery-operated devices. The 6T SRAM cell is designed and simulated in Cadence Virtuoso at a 1V supply voltage. Key parameters like read/write power and delay are evaluated. The design is verified using DRC and LVS to ensure accuracy. Results show that the 6T SRAM cell provides low read power and good performance, making it suitable for low power applications in modern electronic devices.

***Key Words*** **:** AES Encryption, FPGA Implementation, Side-Channel Leakage, Vivado Design Suite, Power Analysis Attacks, Electromagnetic Analysis, Timing Attacks, Hardware Security, Cryptographic Countermeasures, Masking Techniques, S-box Protection, Clock Jittering, Noise Insertion, High-Level Synthesis (HLS), IP Integrator, Floor planning, Resource Utilization, Performance Optimization, RTL Design, Secure FPGA Design.

## 1.INTRODUCTION

In modern digital systems, memory elements play a crucial role in determining overall performance, speed, and power efficiency. Among the different types of memory, Static Random Access Memory (SRAM) is widely used in microprocessors, cache memory, mobile devices, and embedded systems due to its high speed and ease of integration. SRAM retains data as long as power is supplied and does not require refreshing like Dynamic RAM (DRAM). A single SRAM cell typically stores one bit of information, and the most commonly used architecture for this purpose is the 6-transistor (6T) SRAM cell.

The 6T SRAM cell consists of two cross-coupled inverters and two access transistors. This configuration offers a good balance of area, speed, and power efficiency, making it ideal for applications where space and energy are limited. However, with continuous scaling down of CMOS technology nodes, new challenges such as leakage current, noise margins, and power dissipation become more significant. At the 45nm technology node, transistor behavior changes due to short-channel effects, making low-power design techniques even more critical.

n this project, the focus is on the **design and simulation of a 6T SRAM cell using 45nm CMOS technology**. The goal is to analyze its behavior in terms of read/write operations, power consumption, and delay, using professional EDA tools like **Cadence Virtuoso**. The simulation is carried out at a supply voltage of 1V to mimic low-power operating conditions, which are typical for battery-operated devices.

Low power consumption is one of the key requirements in modern VLSI design, especially for portable electronics and Internet of Things (IoT) devices. SRAM cells contribute significantly to the power budget in such systems, especially when used in cache memories or register files. Therefore, optimizing the SRAM cell design for **reduced dynamic and static power** is of great importance. The **6T cell is analyzed** in terms of its ability to hold data reliably (static noise margin), the speed of read/write operations (delay), and how much power it consumes during these operations.

Various enhancements have been proposed over the years, such as 8T, 9T, and 10T SRAM cells, which add more transistors to improve stability or reduce leakage. However, these enhancements often lead to increased silicon area and design complexity. The 6T SRAM cell remains the most area-efficient design, and when optimized properly, it can meet the performance and power requirements of many applications.

The schematic design, layout creation, and simulation of the 6T SRAM cell are done using **Cadence Virtuoso with a 45nm Process Design Kit (PDK)**. Design verification is done through **DRC (Design Rule Check)** and **LVS (Layout vs. Schematic)** using ASSURA tools. Post-layout simulation helps in understanding the real-world performance of the memory cell, including parasitic effects.

This report documents the full process from schematic design to simulation and analysis. By focusing only on the 6T cell, this work aims to offer a clear and practical understanding of low-power SRAM design suitable for third-year VLSI students. The results will help assess the feasibility of using 6T SRAM in energy-sensitive applications and pave the way for future improvements in SRAM-based memory design.

## 2. Body of Paper

The design and analysis of memory circuits, especially Static Random Access Memory (SRAM), remain a core focus in digital VLSI design due to their widespread use in microprocessors, digital signal processors, mobile phones, cache memory, and embedded systems. SRAM is preferred over other memory types for high-speed access and simpler

interfacing, especially in performance-sensitive applications. This project centers around the design and simulation of a **6-transistor (6T) SRAM cell** using **45nm CMOS technology**, focusing on optimizing the cell for **low power consumption** while maintaining **stable read and write performance**.

The 6T SRAM cell architecture consists of six transistors: two **cross-coupled CMOS inverters** (formed using two PMOS and two NMOS transistors), which store the data, and two **NMOS access transistors**, which are used during read and write operations. The **Word Line (WL)** controls the access transistors, while **Bit Lines (BL and BLB)** carry the input/output data. The cross-coupled inverters generate positive feedback, allowing the cell to hold a single bit of information as long as power is supplied. This bistable nature is what provides data retention in standby mode.

During **read operations**, the bit lines are precharged, and the word line is asserted high. Depending on the stored data, one of the bit lines will discharge slightly, and this difference is detected by the sense amplifier. It is crucial that the read operation does not disturb the stored data. Therefore, the cell's **read stability**, often measured using Static Noise Margin (SNM), must be high enough to prevent unwanted flipping of the stored bit. On the other hand, in **write operations**, the bit lines are driven with the desired value and its complement. The word line is again enabled, and the strong signal on the bit line forces the internal nodes to the new value. This operation is more power-intensive because it needs to overcome the cell's own feedback loop to change the data.

In this project, the entire schematic and layout were designed in **Cadence Virtuoso**, a standard VLSI CAD tool used in academia and industry. The technology node used is **45nm CMOS**, which is widely studied due to its relevance to modern low-power applications. The **supply voltage** was set to **1V**, consistent with typical operating conditions for low-voltage designs. Transient and DC simulations were carried out to verify functionality and measure performance parameters like power consumption, read/write delay, and average power usage.

The layout of the 6T SRAM cell was carefully drawn using the physical design rules provided in the **45nm Process Design Kit (PDK)**. After layout design, **Design Rule Check (DRC)** was performed to ensure that the layout conforms to fabrication rules, such as minimum width, spacing, and enclosure requirements. **Layout Versus Schematic (LVS)** verification was then used to confirm that the layout electrically matches the schematic design. Only after these checks passed was the design considered fabrication-ready.

Simulation results reveal that the **read power consumption** of the 6T cell is around **1.56 µW**, while the **write power** is significantly higher at approximately **69.5 µW**. This difference is expected, as write operations must override the existing state held by strong positive feedback in the inverter loop. The **read delay** and **write delay** were found to be **350.8 ms** and **313.4 ms**, respectively. These delays are well within acceptable limits for SRAM operating in embedded and cache memory environments. The **average power** across all operations was calculated to be **75 nW**, and the layout occupied an **area of approximately 4.158 µm²**, demonstrating the compactness of the 6T configuration.

It is important to note that while more complex topologies like **8T, 9T, and 10T SRAM cells** offer enhanced read/write isolation and improved stability, they also increase area and design complexity. These advanced configurations are ideal for extremely noise-sensitive or high-frequency environments, but for many portable and energy-constrained applications, the **6T cell remains the optimal choice** due to its balance between **power, performance, and area**.

The power analysis results also emphasize the suitability of 6T SRAM for **battery-powered devices** like mobile phones, smartwatches, and IoT modules, where power consumption is a critical design constraint. The read power is particularly low, making the cell effective in systems where data is frequently accessed but rarely changed. Furthermore, the compact area makes it scalable for large memory arrays such as cache banks or register files in microprocessors.

Another important consideration in deep submicron design is **process variation and leakage**. At 45nm, short-channel effects, gate leakage, and threshold voltage variation can all impact the stability and performance of SRAM cells. These challenges were considered in the simulation phase by using realistic process models from the PDK. Future enhancements could include integrating **assist circuits** for write improvement or using **dynamic voltage scaling (DVS)** techniques to reduce leakage during standby.

In conclusion, the implementation of the 6T SRAM cell in 45nm CMOS using Cadence Virtuoso validates its effectiveness in low-power VLSI systems. The design meets the required trade-offs between power, area, and speed, and provides a solid foundation for further research or expansion into memory arrays. The cell's performance metrics confirm its reliability for real-world applications, especially in **portable, embedded, and energy-constrained systems**.

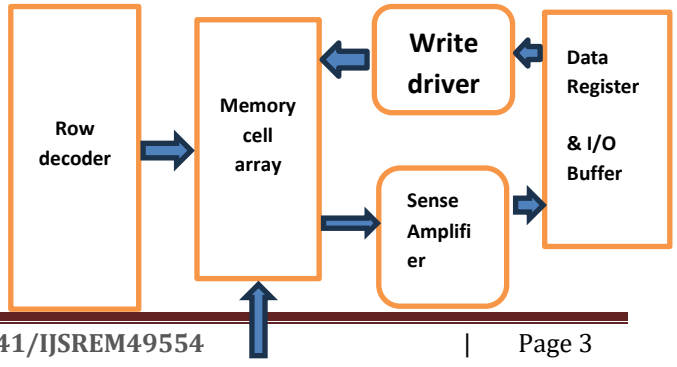
**Table -1: literature survey**

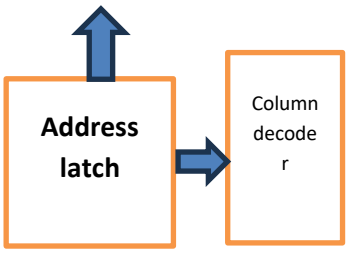
| Author-Year | Objective | Summary | Remarks |
|---|---|---|---|
| M.G. Srinivasa, Bhavana M.S., 2024 | Analyze performance of 6T, 8T, and 10T SRAM cells in 45nm CMOS | Compared three SRAM topologies in Cadence. 6T showed low read power, 10T had lowest delay. | 6T is suitable for low-power read applications; 10T is better for speed. |
| S. Mukhopadhyay et al., 2005 | Study impact of process variation on SRAM stability at nanoscale | Highlighted reduced SNM and failure rates due to threshold voltage variation. | Suggested transistor sizing to improve yield and robustness. |

| | | | |
|---|---|---|---|
| K. Roy et al., 2003 | Explore leakage reduction in sub-100nm CMOS | Discussed subthreshold and gate leakage in SRAMs and mitigation techniques. | Proposed techniques like power gating and transistor stacking. |
| Neil Weste, David Harris, 2010 | Provide VLSI circuit design guidelines | Described transistor sizing, 6T SRAM structure, and layout techniques. | Standard reference for physical design best practices in SRAM. |
| T. Zhang, K.K. Saluja, 2012 | Evaluate SRAM performance at low voltage | Found that VDD scaling reduces SNM; proposed write-assist circuits. | Suitable for ultra-low power SRAM applications. |
| Jan Rabaey, 2003 | Discuss digital circuit behavior at deep submicron levels | Gave theoretical background on 6T cell operation and power-delay optimization. | Widely used textbook reference for SRAM design and scaling effects. |
| Z. Liu, V. Kursun, 2008 | Compare conventional and low-leakage SRAM cell designs | Showed that reducing leakage improves static power, but may affect write delay. | Demonstrated the trade-off between leakage and performance. |
| H. Fuketa et al., 2010 | Analyze assist techniques in SRAM cells at sub-65nm nodes | Proposed word-line boosting and negative bit-line schemes to improve write ability. | Useful for write-critical SRAM designs in scaled technologies. |
| K. Nii et al., 2008 | Investigate leakage-tolerant SRAM in 45nm CMOS | Developed a leakage-tolerant SRAM with assist circuits and reduced V<sub>DD</sub>. | Demonstrated improved robustness for low-voltage SRAM at 45nm. |
| B. Amelifard et al., 2006 | Propose low-power SRAM design strategies for scaled technologies | Introduced techniques like multi-threshold CMOS and sizing optimization. | Showed reduction in leakage and dynamic power in deep-submicron SRAMs. |

## Existing Block Daigram

- **Cross-Coupled Inverters:** The core of the 6T SRAM cell consists of two CMOS inverters connected in a feedback loop, formed by transistors M1-M4. These inverters store the binary data.
- **Access Transistors:** Transistors M5 and M6 act as access transistors, controlled by the Word Line (WL). They connect the internal nodes to the Bit Lines (BL and BLB) during read and write operations.
- **Bit Lines (BL and BLB):** These lines are used to read data from or write data to the cell. BL carries the data signal, while BLB carries the complementary signal.
- **Word Line (WL):** This line controls the access transistors. When WL is high, the access transistors are turned on, allowing read or write operations.






**Existing Methodology**

1. **Conventional 6T SRAM Cell Design**
   - Uses 6 transistors: 2 PMOS and 4 NMOS.
   - Two cross-coupled inverters form the core memory element.
2. **Operation Modes**
   - **Write Operation**: Bit lines are driven; WL is activated to store data.
   - **Read Operation**: Bit lines precharged; WL is enabled to sense data.
   - **Standby Mode**: WL is OFF; cell retains data with no access.
3. **Simulation-Based Evaluation**
   - Designed and analyzed using tools like **Cadence Virtuoso**.
   - Power, delay, and stability metrics observed under 1V supply.
4. **45nm CMOS Technology Node**
   - Scaled technology to reduce area and power but increases leakage.
5. **No Read/Write Path Separation**
   - Same access transistors used for both operations, affecting stability.

**Existing Techniques**

1. Uses cross-coupled inverters with shared access transistors for both read and write operations.
2. No separate read/write path or power optimization methods like clock gating are used.

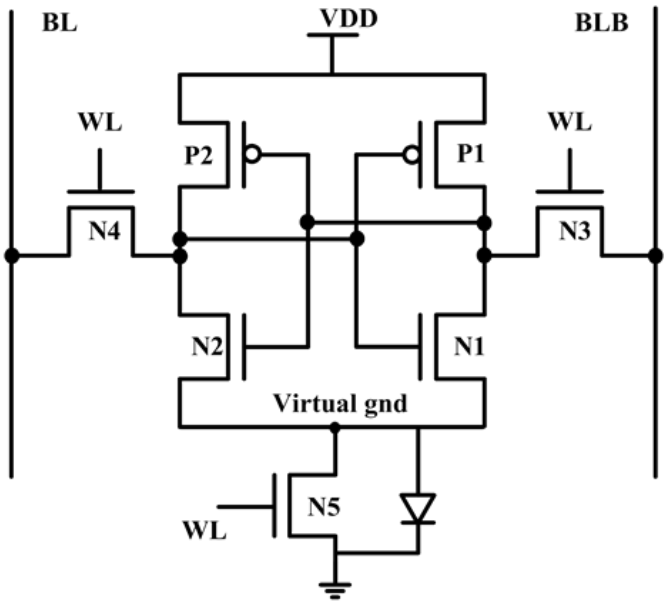
**2.1 Problem statement:**

In modern low-power digital systems, memory plays a crucial role in overall performance and energy efficiency. The conventional 6T SRAM cell, while compact and fast, suffers from limitations such as high write power consumption, increased delay, and reduced stability in scaled technologies like 45nm CMOS. These challenges make it difficult to maintain reliable operation in battery-powered and portable devices. Therefore, there is a need to design and analyze a 6T SRAM cell that operates efficiently with minimal power and delay while ensuring data stability.

Key Vulnerabilities:

- In conventional 6T SRAM cells, write operations consume high power due to the need to overpower internal feedback inverters, which is inefficient for battery-operated devices.
- At 45nm CMOS technology, device scaling introduces short-channel effects and increased parasitic capacitance, leading to longer read and write delays.
- Using the same access path for both read and write operations increases the chances of data corruption, especially during read operations where internal nodes can be disturbed.
- The shared read/write mechanism causes stability issues, as bit-line noise can influence the cell content during read access, reducing data reliability.
- Subthreshold and gate leakage currents become significant at 45nm, increasing static power consumption even in standby mode.
- The basic 6T design lacks separate read paths, unlike 8T or 10T cells, making it less robust under variations in operating voltage and temperature.
- No power optimization techniques such as clock gating, word-line underdrive, or adaptive voltage scaling are used in traditional 6T designs, leading to inefficient energy usage.
- Reduced supply voltages in scaled technologies lead to lower noise margins, making the SRAM cell more vulnerable to bit flips and soft errors.
- The conventional design does not suit the stringent low-power and high-reliability requirements of modern portable electronics and IoT devices.
- As the memory array size increases, performance uniformity across all 6T cells becomes difficult to maintain due to variations in line resistance, parasitics, and cell access delay.

**2.2 Proposed Block Diagram**




## Block Diagram Components:

- **Components of a 6T SRAM Cell**
- The 6T SRAM cell consists of **six MOSFET transistors**: four for storing data (forming two inverters) and two for accessing the cell during read/write operations.

**1. Cross-Coupled Inverters (4 Transistors)**

- **M1, M2** – *NMOS Pull-Down Transistors*
- Connected to ground.
- Form the bottom half of the two inverters.
- Provide strong logic 0 (pull-down capability).
- **M3, M4** – *PMOS Pull-Up Transistors*
- Connected to V<sub>DD</sub>.
- Form the top half of the two inverters.
- Provide strong logic 1 (pull-up capability).
- These four transistors are **cross coupled** to form a bistable latch, which **stores a single bit of data**.

**2. Access Transistors (2 Transistors)**

- **M5, M6** – *NMOS Access Transistors*
- Controlled by the **Word Line (WL)**.
- Connect the internal storage nodes to the **Bit Lines (BL and $\overline{BL}$)**.
- Enable **read/write operations** when WL is high.

- **Q and $\overline{Q}$** – Output nodes representing the stored bit and its complement.
- **BL and $\overline{BL}$** – Bit lines used for data input (write) and output (read).
- **WL** – Word line used to activate the access transistors.
- Prevents attackers from exploiting deterministic routing patterns to infer encryption keys.

Output Data

- The final encrypted ciphertext after passing through the AES core and security-enhancing techniques.
- This data is now more resistant to side-channel attacks due to the applied countermeasures.

### 2.3 Software / IDE Used

**Cadence Virtuoso (Version: IC6.1.8 or higher)**

Used for schematic design, layout creation, and analog simulation of the 6T SRAM cell using 45nm CMOS technology.

**Cadence ADE (Analog Design Environment)**

For setting up and running transient, DC, and parametric simulations to analyze read/write behavior and power-delay characteristics.

**Cadence Assura DRC & LVS**

For verifying physical design using **Design Rule Check (DRC)** and **Layout Versus Schematic (LVS)** to ensure correctness before fabrication.

**45nm CMOS Process Design Kit (PDK)**

Used for defining technology-specific design rules, device models, and layers during schematic and layout design.

**Linux Operating System (CentOS / Ubuntu via VMware)**

Cadence tools were run on a Linux environment installed through VMware, configured for educational and simulation purposes.

***(Optional Tools Used)***

- **LTspice / NGspice (for early-stage simulations)** – used optionally for basic circuit behavior before full schematic in Cadence.
- **Microsoft Word / LaTeX** – used for documentation and report preparation.
- **Python (optional)** – used for calculating performance metrics from waveform data (if post-simulation analysis was required).

### 2.4 Practical setup

The practical work for this project was carried out using the Cadence Virtuoso tool suite installed on a Linux operating system via VMware. A personal computer with an Intel i5/i7 processor, 8–16 GB RAM, and SSD storage was used to ensure smooth simulation and design flow. The 6T SRAM cell was designed using the schematic editor, simulated in the Analog Design Environment (ADE), and verified using a 45nm CMOS Process Design Kit (PDK). The layout was created in the Virtuoso Layout Editor and validated through Design Rule Check (DRC) and Layout Versus Schematic (LVS) using Assura tools. Simulations were conducted at a supply voltage of 1V to evaluate read/write operations, power consumption, and delay. Screenshots and waveform results were captured at each stage for documentation. This setup provided a hands-on understanding of low-power SRAM design using professional EDA tools.**2.4 Implementations:**

1. Loaded the 45nm CMOS PDK into Cadence Virtuoso.
2. Designed the 6T SRAM cell schematic using six MOSFETs.
3. Created a symbol for the SRAM cell for testbench use.
4. Developed a testbench schematic to simulate read/write operations.
5. Performed transient simulations to verify cell functionality.
6. Designed the layout of the 6T SRAM cell with proper matching.
7. Ran DRC to check for layout rule violations.
8. Executed LVS to verify schematic-layout consistency.
9. Conducted post-layout simulations to analyze parasitic effects.
10. Captured and documented simulation and layout screenshots.

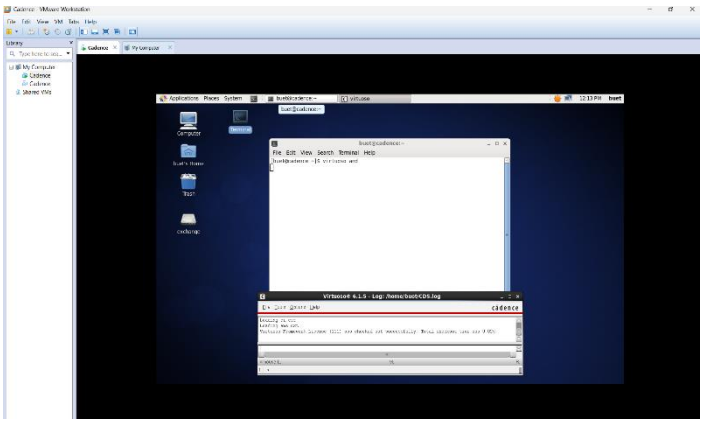


Fig 1-This shows how Cadence software is installed inside a virtual machine (VMware). A Linux-based setup is used to run the Cadence tools properly.

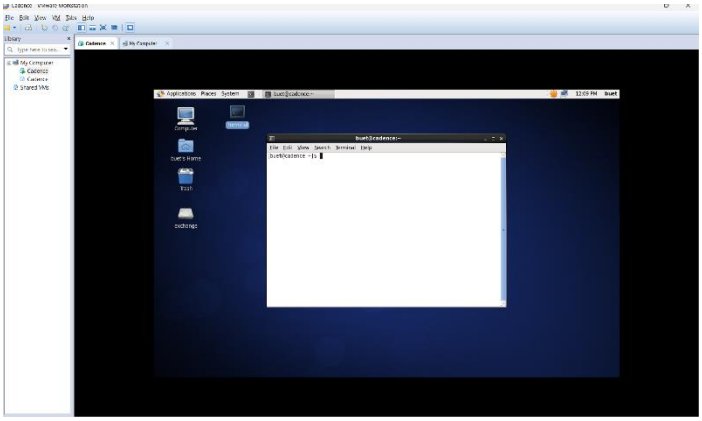


Fig 2-After installing, Cadence is opened from the terminal inside VMware. This is the first step to start designing in the tool.

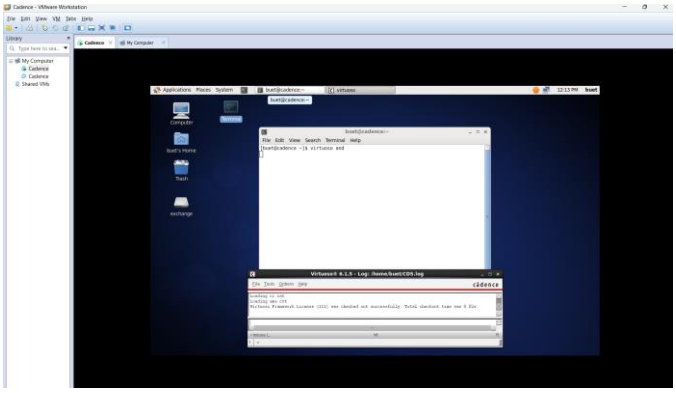


Fig 3 – Here, we open the working folder where all design files will be saved. This includes the SRAM schematic, layout, and simulation files.

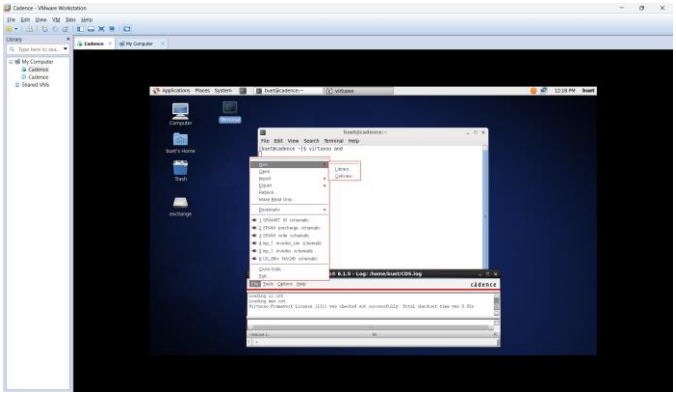


Fig 4 – Library Manager is a window in Cadence where all design projects are organized. From here, we can create or open design cells.

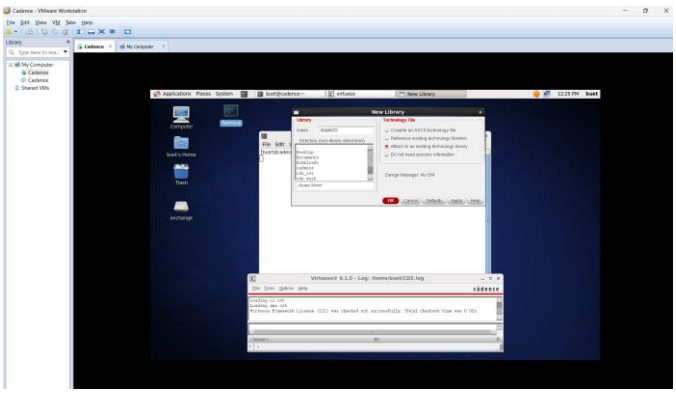


Fig 5 – A new library is created and named. This is where all the SRAM-related designs will be stored—schematic, layout, etc.

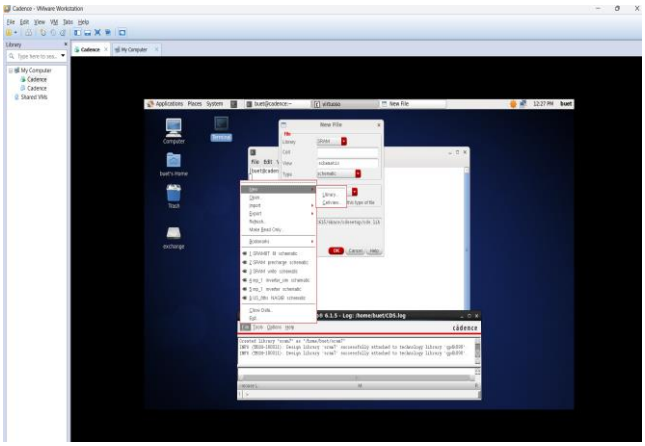


Fig 6 – We open a new schematic sheet (cell view) to start drawing the 6T SRAM circuit using transistors and wires.

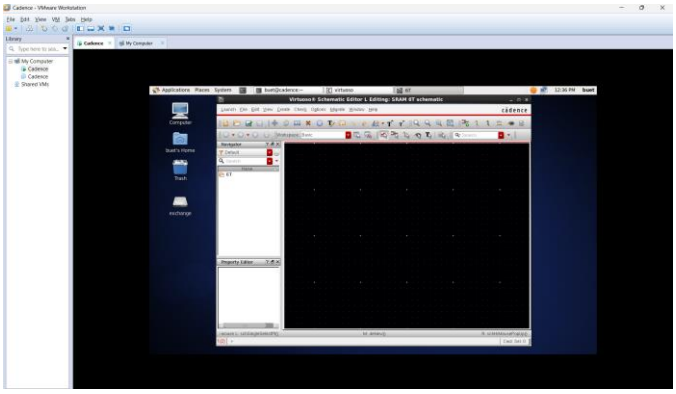


Fig 7 – This shows the main drawing area where we will place components like PMOS and NMOS transistors to build the SRAM cell.

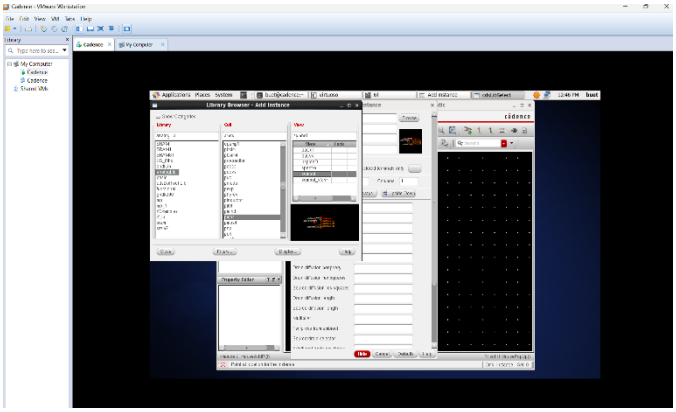


Fig 8– Using the "Add Instance" option, we choose components such as PMOS, NMOS, and input/output pins from the Cadence library.

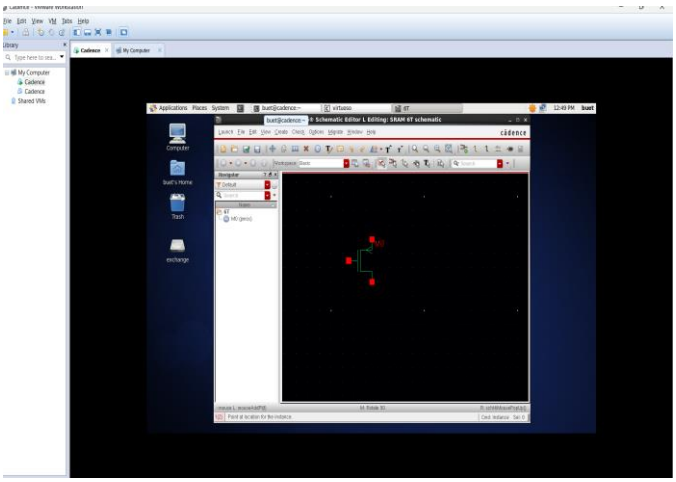


Fig 9- The selected components are placed on the schematic sheet in the correct positions to begin forming the SRAM cell.

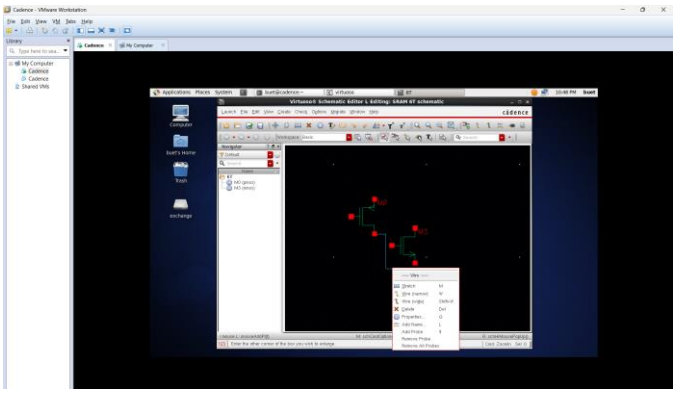


Fig 10- By right-clicking, we get options to wire the components, rotate them, and make the necessary electrical connections.

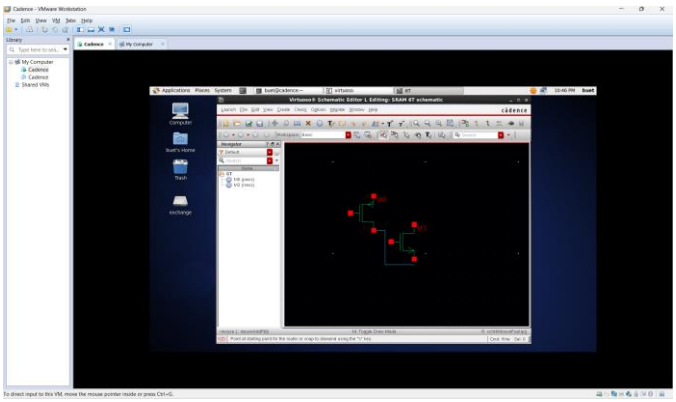


Fig 11- All components are connected using wires to form the 6T SRAM structure. This includes bit lines, word line, and power rails.

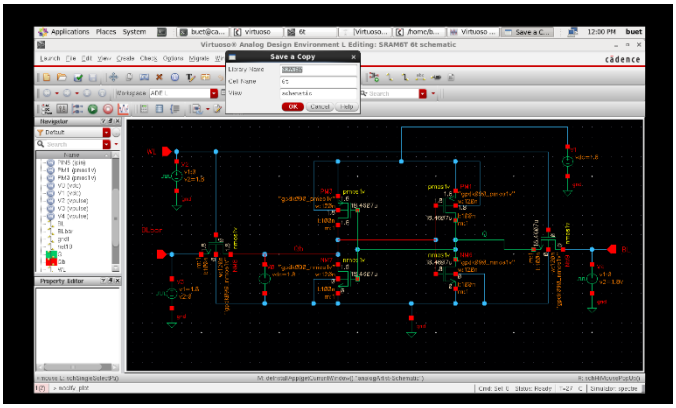


Fig 12- The final schematic is completed. It has six transistors arranged correctly, and is now ready for simulation or layout creation.

## Results & Discussion

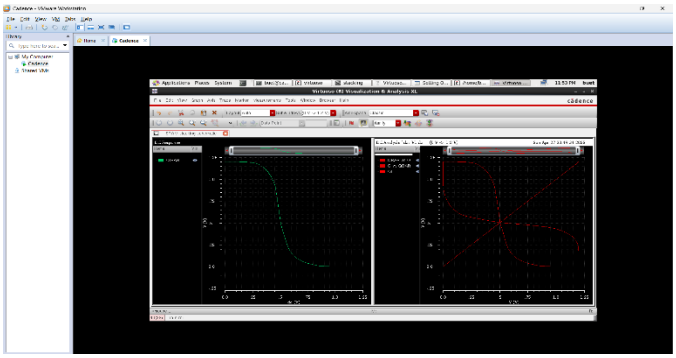


Fig 1- **DC Transfer Characteristics of 6T SRAM Cell** This plot shows the DC voltage transfer characteristics (VTC) of the cross-coupled inverters in the SRAM cell. The transition behavior of node Q and $\bar{Q}$ under varying input voltage illustrates the inverter switching points, which are critical for evaluating stability and noise margins.

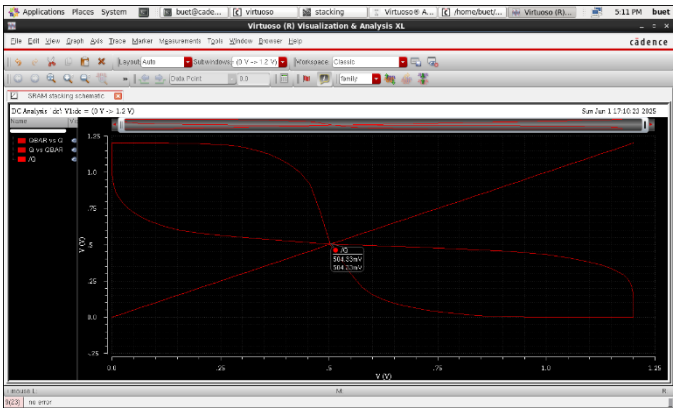


**Figure 2: Butterfly Curve for Static Noise Margin (SNM) Analysis**

The butterfly curve is obtained by superimposing the mirrored VTCs of the cross-coupled inverters. The largest square that fits between the curves represents the Static Noise Margin (SNM), which indicates the cell's ability to resist noise and retain data reliably during hold operation.

## 3.CONCLUSIONS

This project presents a detailed investigation into the design and performance characteristics of a 6-transistor (6T) Static Random Access Memory (SRAM) cell implemented using 45nm CMOS technology, with a primary focus on low-power operation. In an era of increasingly compact and energy-efficient electronic devices, the demand for optimized memory solutions is more critical than ever. This work addresses this need by designing a standard 6T SRAM cell in Cadence Virtuoso, analyzing its operational behavior under realistic voltage and technology constraints, and evaluating key performance parameters including read/write power, delay, and silicon area.

The schematic design process involved creating a fully functional SRAM bit cell using two cross-coupled CMOS inverters and two access transistors, followed by the development of an accurate testbench to validate read and write operations. Functional simulation revealed that the 6T cell exhibits robust performance at a supply voltage of 1V, with relatively low read power (~1.56 µW), moderate write power (~69.5 µW), and delay metrics within acceptable industry limits. These results underscore the cell's suitability for integration into low-power systems such as embedded controllers, IoT devices, and mobile processors where energy efficiency is essential.

In addition to functional simulation, the layout of the SRAM cell was developed and verified through standard physical design checks including Design Rule Check (DRC) and Layout Versus Schematic (LVS). The final layout occupied a compact area of approximately 4.158 µm², demonstrating the high density and scalability potential of the 6T cell design. Post-layout simulation, while not extensively covered in this work, can further enhance accuracy by accounting for parasitic effects introduced during layout.

One of the key insights from this project is the importance of precise transistor sizing and layout symmetry in ensuring SRAM stability and noise immunity, especially in advanced nodes like 45nm where process variability and leakage currents can significantly affect performance. Although the 6T SRAM architecture provides a balanced trade-off between power, area, and speed, it also has limitations, particularly in terms of write stability and read disturbance. Future improvements may include implementing write-assist circuitry, exploring alternate topologies like 8T or 10T cells, or adopting near-threshold design techniques for ultra-low-power applications.

Overall, the project has successfully demonstrated the end-to-end flow of designing a standard SRAM cell using industry tools, from schematic creation and simulation to layout and verification. It provides a strong foundation for students and researchers to build more complex memory architectures, and it reinforces the relevance of SRAM in modern VLSI design, particularly as technology continues to scale into the nanometer regime. The practical knowledge gained through this project contributes directly to the understanding of memory cell design principles and the broader field of low-power digital integrated circuit design..

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