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Design and Performance Evaluation of Conventional 6T vs. Single-Ended 6T SRAM Cell

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Abstract -As the demand for low-power, high-performance memory systems grows, the design of efficient SRAM (Static Random Access Memory) cells becomes increasingly crucial. This paper explores the power consumption, performance, and stability of two SRAM cell designs: the conventional 6T and the Single Ended 6T SRAM. While the conventional 6T SRAM is prone to read disturb noise and high leakage power, it remains widely used due to its simplicity and compactness. To address these issues, the Single Ended 6T SRAM cell is introduced as an alternative, which reduces both power consumption and area while maintaining competitive performance. The study provides a detailed analysis of static and dynamic power consumption, read/write stability, and overall energy efficiency for both cell architectures. Simulation results show that the Single Ended 6T SRAM offers significant improvements in power reduction without compromising speed, making it a promising solution for future low-power, high-performance memory applications.

Keywords— SRAM cell, Pre-Charge Circuits, Sense Amplifiers, and Single-Ended vs. Conventional 6T SRAM Cell.

1.INTRODUCTION

Power dissipation is a significant concern in VLSI circuit design, particularly with CMOS technology as the dominant choice for implementation. As technology scales down, leakage power has become a primary challenge in low-power design. This issue is further amplified by increasing chip densities, where memory designs like SRAM are heavily impacted by leakage power.

This study compares power dissipation across various SRAM systems, focusing on the 8T SRAM cell. The 8T design integrates two NMOS sleep transistors, placed in the pull-down paths of the two inverters in a standard 6T SRAM cell. This innovative approach reduces both leakage and dynamic power, positioning the 8T SRAM cell as an ultra-low-power solution. Furthermore, the cell features a self-correcting feedback mechanism, ensuring stability during active operation.

A 1-bit SRAM array is developed using key functional blocks, including the SRAM cell, data write circuitry, bit-line conditioning, and a sense amplifier. The study involves designing, simulating, and verifying a 1-bit memory cell using various SRAM configurations. It highlights the potential for significant power reduction in SRAM design, addressing challenges in modern chip technologies and contributing to energy-efficient memory solutions.

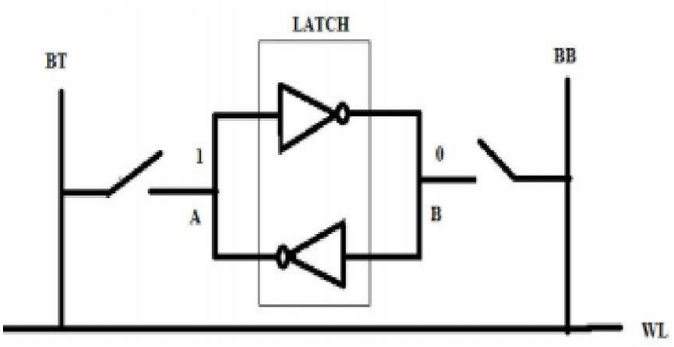

Fig.1. Basic SRAM Memory Cell

2. IMPLEMENTATION

This section presents the design of a 1-bit memory cell utilizing both the conventional 6T SRAM and the single-ended 6T SRAM configurations.

2.1 Conventional 6T SRAM Cell

The 6T SRAM cell comprises six transistors: two NMOS and two PMOS transistors form cross-coupled inverters that store a single bit of data, representing logic "0" and "1" in stable states. Two additional NMOS transistors act as access transistors, controlled by the word line (WL), which connects or disconnects the storage cell from the bit lines (BL and BL bar). These complementary bit lines facilitate data transfer during read and write operations, ensuring both the signal and its inverse are available to improve noise margins and reliability. During write operations, the bit lines are set to the desired data values while the word line activates, enabling data to be written into the cell. For read operations, the stored data is accessed through the bit lines. Although the 6T SRAM configuration outperforms resistive load 4T structures in terms of electrical performance, shrinking transistor sizes result in increased leakage power, leading to higher power dissipation—a significant challenge for modern low-power designs.

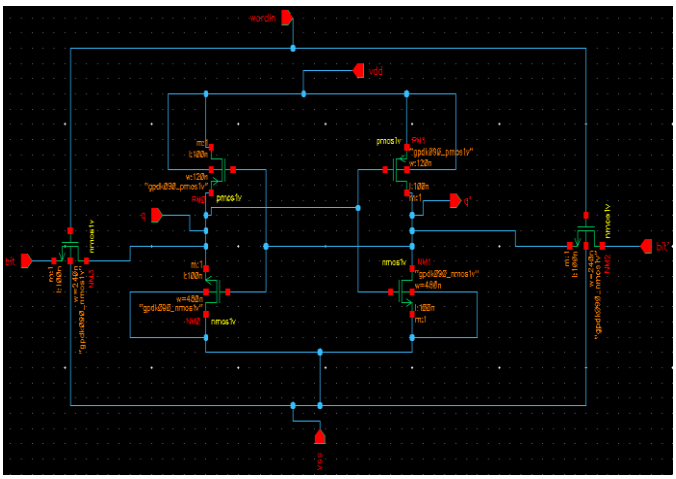

Fig.2. Conventional 6T SRAM CELL

2.2 SINGLE ENDED 6T SRAM CELL

A Single-Ended 6T SRAM Cell is a simplified variant of the traditional 6T SRAM architecture that uses only one bit line for read and write operations instead of the standard complementary bit lines. This design retains the six-transistor structure, with two NMOS and two PMOS transistors forming cross-coupled inverters to store a single bit of data in two stable states, and two NMOS access transistors controlled by the word line (WL) to enable data access. The single bit line facilitates data transfer during operations, simplifying the circuit design by eliminating the need for a complementary bitline and its associated driver and sense amplifier. This reduction in complexity and bitline switching activity significantly lowers power consumption, making the single-ended 6T SRAM cell well-suited for low-power applications such as IoT devices and energy-constrained systems. However, this simplicity comes at the cost of reduced noise margins, as the absence of a complementary bit line diminishes noise immunity. Additionally, the single-ended structure can cause read disturbance, where the bitline swing during a read operation affects the stability of the stored data. Despite these challenges, the single-ended 6T SRAM cell is a viable solution for applications prioritizing power efficiency and compact design.

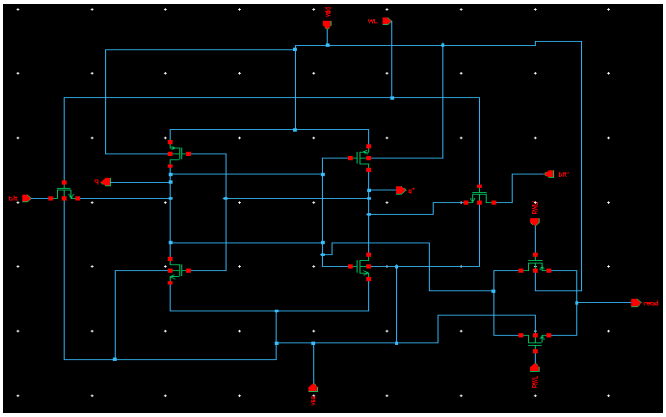

Fig.3. Single ended 6T SRAM Cell

2.3 PERIPERAL CIRCUITS

The complete memory system is illustrated in the figures. Accessing the SRAM cell requires additional circuitry, including:

- **Pre-Charge Circuit**
- **Data Write Circuit**
- **Sense Amplifier**

The **Pre-Charge Circuit** pre-charges the bit lines (BIT and BITN) to a logic "1" during the memory cell's inactive state. This pre-charging is disabled during read or write operations.

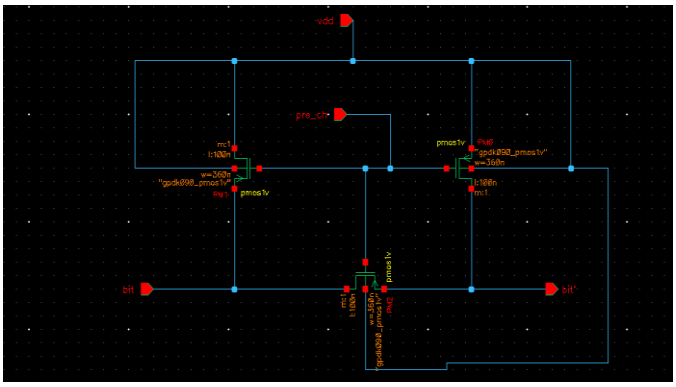

Fig.4. Pre-charge circuit

The **Data Write** Circuit writes data and its complement onto the bit lines. To write a "1" into the SRAM cell, the word line (WL) is activated, the BIT line is driven high, and BITN is driven low. Conversely, to write a "0," BIT is set low, and BITN is set high. Before a read operation, both BIT and BITN lines are pre-charged high, and the SRAM cell is selected. When the WL activates the SRAM cell for reading, one of the bit lines is pulled down based on the stored data. If BIT is pulled low, the data is "0," and if BITN is pulled low, the data is "1."

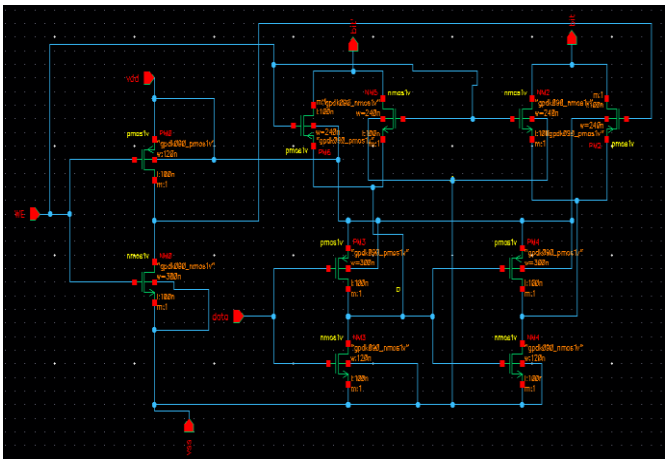

Fig.5.Write circuit

The **Sense Amplifier** circuit is responsible for detecting which bit line is being pulled down, enabling the read operation of the stored data. During the read operation, the signals READ and READ_BAR represent the stored data and its complement, respectively. The SRAM cell, along with the word line (WL), determines the address from which data is read or written. The signal data represents the single-bit value, either 1 or 0, that is stored in or retrieved from the SRAM cell. READ corresponds to the stored data, while READ_BAR is its inverse.

A significant drawback of the traditional memory system, which includes the write circuit, pre-charge circuit, and sense amplifier, is its high area and power consumption. To address this, a single-ended 6T SRAM design is introduced. This design reduces both area and power usage significantly by utilizing fewer transistors compared to conventional memory cells.

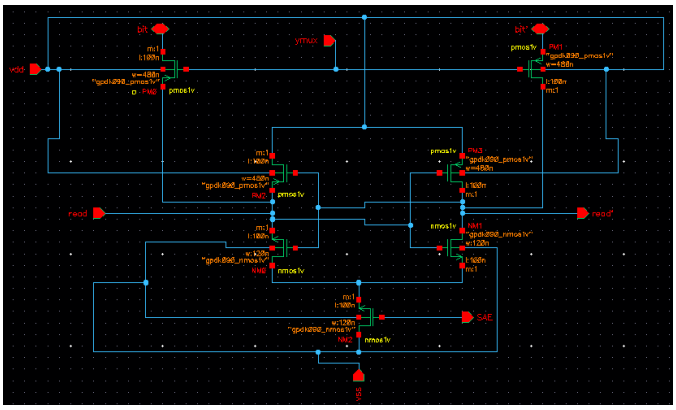

Fig.6. Sense Amplifier

3. POWER ANALYSIS

The 6T SRAM cell features a simpler design compared to the 8T SRAM cell, utilizing six transistors—four for data storage and two for access. This design facilitates data storage and read/write operations. In conventional 6T SRAM, power consumption can be higher during active mode due to the direct connection of pull-down transistors to the bit lines. Dynamic power dissipation is influenced by switching activity and the capacitance of the bit lines during operations.

Power dissipation in single ended 6T SRAM can be minimized by eliminating certain peripheral circuits required in more complex designs. For instance, a typical 6T SRAM design often avoids using precharge circuits or sense amplifiers for data reading. Instead, it employs a transmission gate at node Q, which simplifies the design and reduces power usage.

In single-ended 6T SRAM, the absence of precharge and sense amplifier circuits further decreases transistor count in the read process, simplifying the memory cell and reducing power consumption. Compared to conventional 6T SRAM, which includes additional transistors for improved stability and reduced leakage, the 6T design achieves lower complexity and power usage.

Moreover, the reduced total capacitance at the bit lines in 6T SRAM, due to the lack of extra series-connected transistors, contributes to lower dynamic power dissipation, as power dissipation correlates with capacitance and switching frequency**.**

4. Simulations and Results:

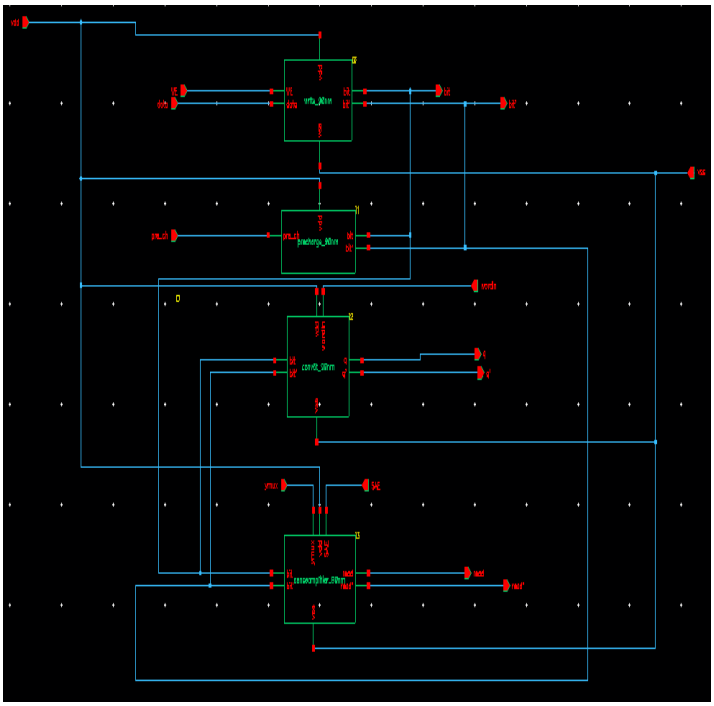

Fig.7. conventional 6T SRAM cell with peripheral circuits

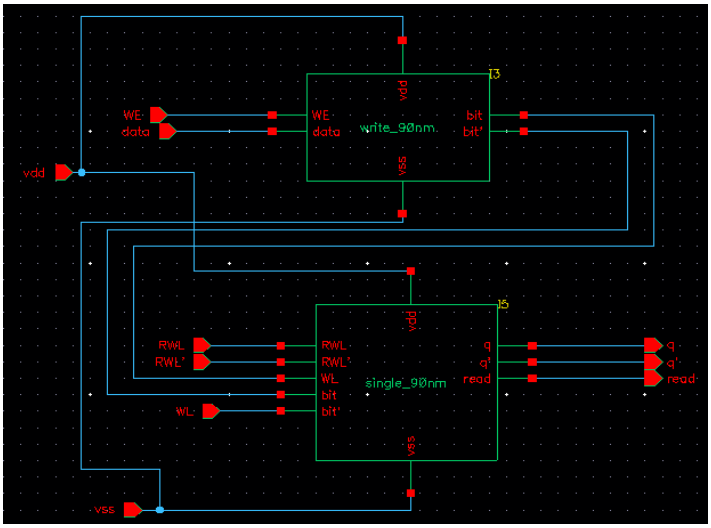

Fig.8. Single ended 6T SRAM cell without sense amplifier and pre charge circuit

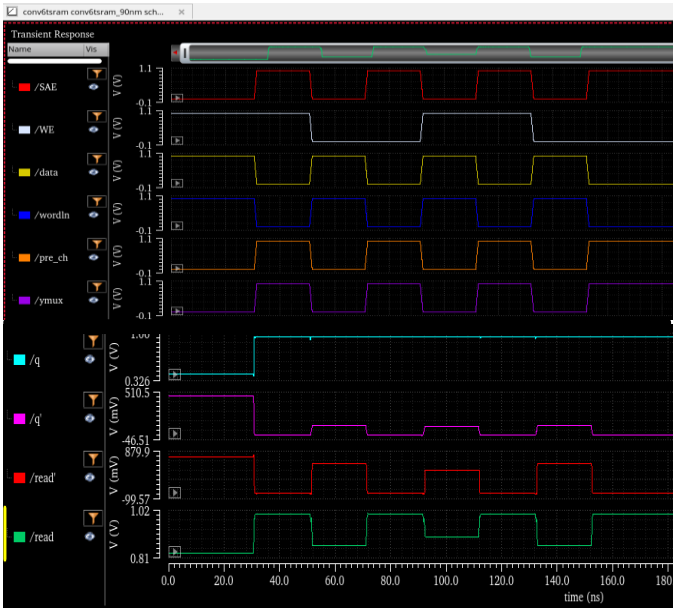

Fig.9. Waveform of conventional 6T SRAM cell

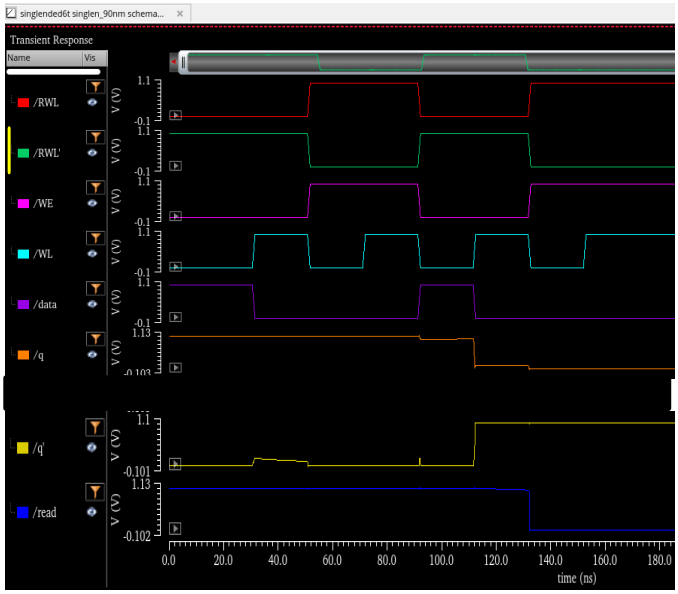

Fig.10. Waveform for single ended 6T SRAM cell

Table 1: Power analysis of single bit memory cell using different SRAM cells

SL.NO	1-bit SRAM Cell	Total power(nW)
1	Conventional 6T	423.8
2	Single Ended 6T	360.2

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