International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 10 Issue: 10 | Oct - 2026 SJIF Rating: 8.659 ISSN: 2582-3930

Design and Simulation of a BCD Up-Down Counter Using VLSI

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Abstract

BCD counters are used in systems like clocks, timers, frequency counters and decimal displays. In this work a synchronous BCD Up-Down counter is described in Verilog HDL. Checked through simulation. The design starts with a 4-bit counter, for one digit. Two such stages are then connected to form an 8-bit counter that represents two digits. Simulation and RTL synthesis are carried out using AMD Vivado Design Suite.

Key Words: BCD counter, Up-Down counter, synchronous counter, Verilog HDL, RTL, FPGA, VLSI, AMD Vivado.

1. INTRODUCTION

Digital circuits have uses, including counting, generating timing signals dividing frequencies and representing decimal numbers. Counters are circuits that provide these capabilities. To represent a circuit output, in decimal you can use BCD code, in which groups of four bits represent individual decimal digits.

A 4-bit binary number can show sixteen values. Only ten of those values from 0000 to 1001 are BCD digits. The binary values 1010 to 1111 are not BCD digits. Extra circuitry is required so that a BCD counter can reset to a value when it reaches the highest decimal digit. A BCD up-down counter can count in either direction. When up counting is chosen the BCD counter sequence goes from 0 to 9. Then starts again at 0. When down counting is chosen the BCD counter goes from 9 to 0 and then returns to 9. In a design the storage elements share the same clock so the state changes are coordinated at the clock edge. This also makes the BCD counter design convenient to model and test, in HDL.

This project is developed in two stages. First I. Tested a 4-bit synchronous BCD Up-Down counter. Then I connected two 4-bit stages to create an 8-bit counter that can display two digits. The lower stage holds the units digit while the upper stage holds the tens digit. I wrote the circuit in Verilog HDL. Verified it with simulation and RTL synthesis in AMD Vivado.

The aim is to build a counter using reusable blocks and verify the counter's main functions: decimal counting, direction control, correction, at the 0 and 9 limits and connection of multiple digits. The study is limited to RTL design and FPGA-oriented verification; the study does not claim transistor-level design or physical ASIC fabrication.

2. RELATED WORK

Digital counters can be built in ways. One way is the ripple counter. In a ripple counter when one stage changes it pushes a change to the stage and the delay can add up from one stage to the next. Another way is the counter. In a counter every storage element receives the same clock and a combinational logic block tells each element what to do next. Digital counters also include counters, where the counting sequence can be set by software and high-speed counter structures, which are built for very fast counting. Each type of counter has its own strengths and use cases. BCD counters are useful when a system needs values directly. For example BCD counters appear in clocks, timers, frequency counters, event counters and display circuits. The design of BCD counters must handle the boundary correctly. This ensures that the output of BCD counters never moves into a BCD state during normal counting.

A counter that has than one decimal digit can be made by putting together several BCD stages. When the counter counts up the units digit goes from 9 to 0. Tells the tens digit to go up. When the counter counts down the units digit goes from 0, to 9. Tells the tens digit to go down. Using the stage again makes the design easier to add more digits. HDL tools let you write a counter, run simulations

turn the design into logic and examine what the structure looks like before you put it on hardware. AMD Vivado has an RTL synthesis flow that takes the HDL description and turns it into a hardware representation, for analysis [1].

With these ideas in mind this project has a modular design that uses one 4-bit counter and two connected stages, for the 8-bit version. The main goal is to make sure the BCD transitions are correct to have a shared clock and to create a structure that can be expanded without making the design too complicated.

3. PROPOSED SYSTEM

The proposed circuit has two versions: a 4-bit BCD Up-Down counter and an 8-bit counter built by connecting two 4-bit stages. The 4-bit module is the building block, for both. In the 8-bit version both stages use the clock and reset signals. The carry and borrow conditions link the units digit stage to the tens digit stage.

A. 4-BIT BCD UP-DOWN COUNTER

When I look at the 4-bit module I see that it uses a clock, reset, direction control and a 4-bit BCD output. In up mode the 4-bit BCD output moves through 0000, 0001 0010. So on until 1001 then returns to 0000. In down mode the 4-bit BCD output moves from 1001, towards 0000 then returns to 1001. The transition logic is written so that the counter stays within

the BCD range.

The circuit can be understood as a register and next-state logic. The register stores the digit. The logic checks that digit with the direction input and selects the next valid value. At the clock edge the register takes that value. Reset brings the counter to a known starting state.

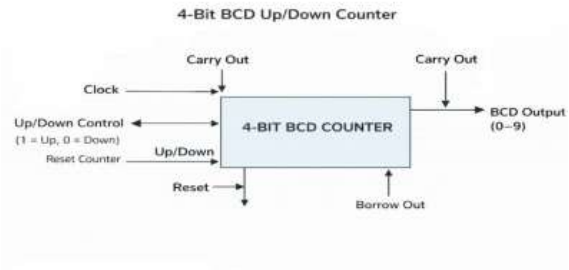


Fig. 1. 4-bit BCD Up-Down counter block diagram.

B. 8-BIT BCD UP-DOWN COUNTER

The 8-bit version shows two digits. The lower four bits, y[3:0] hold the units digit. The upper four bits, y[7:4] hold the tens digit. For example the bit pattern 0010 0101 means twenty-five in BCD. Both stages share the clock and reset signals.

When the counter is in up mode the units digit counts from zero to nine. When it rolls over from nine to zero a carry condition pushes the tens digit forward. When the counter is in down mode the units digit counts down. When it moves from zero to nine a borrow condition pulls the tens digit back. With these connections the two-digit counter can count up from 00, to 99. Count down from 99 to 00.

The two stages share the four-bit counting logic so the design does not need separate logic for the tens digit. This makes the circuit easier to read and to test. If decimal digits are needed simply add stages and connect their carry and borrow signals in the same manner.

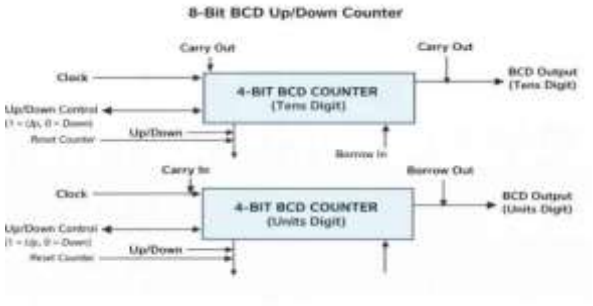


Fig. 2. 8-bit BCD Up-Down counter block diagram.

4. DESIGN METHODOLOGY

The design process contains defining the required counting sequence writing the RTL simulating the circuit synthesizing it and checking the outputs.

We first set the BCD states and up/down transitions.

The 4-bit counter is then described in Verilog HDL. Tested.

After that two stages are linked to form the 8-bit counter.

Step 1: Identify the inputs and output: clock, reset, direction control and BCD output.

Step 2: Set the BCD range from 0000 to 1001.

Step 3: Write the next-state logic for both up counting and down counting.

Step 4: Add correction so that 9 changes to 0 in up mode and 0 changes to 9 in down mode.

Step 5: Test the 4-bit module with a Verilog testbench.

Step 6: Connect two 4-bit stages to make the two-digit 8-bit counter.

Step 7: Connect the carry. Borrow conditions, between the units and tens stages.

Step 8: Run the circuit and look at the waveform it produces.

Step 9: Perform synthesis using AMD Vivado. Check the RTL schematic.

Step 10: Look at the simulated output. Compare it to the expected decimal sequence.

The testbench generates a clock that repeats. Adds reset and direction-control inputs. The clock changes at fixed times and the stored count is updated when the clock is active.

At the beginning of the simulation reset is used to set the counter to a starting value. Then the direction input is changed so that both up-counting and down-counting can be tested.

The tests, in this work are meant to check the logic function. They do not show the performance of a chip.

5. IMPLEMENTATION USING AMD VIVADO

The counter is written in Verilog HDL. Developed using the AMD Vivado Design Suite. This tool allows for RTL entry, simulation, synthesis and inspection of the logic that is generated. During synthesis the RTL description is transformed into a hardware netlist for FPGA implementation and analysis [1].

The process begins with the Verilog module and its testbench. After adding the source files the design is elaborated to verify the module structure and connections. A behavioral simulation is then executed to observe the clock, reset, direction input and counter output.

Once the simulation check is complete RTL synthesis is performed. The RTL schematic shows the structure that is inferred from the Verilog code. In the 4-bit version it displays the state storage and next-state logic. In the 8-bit version it also illustrates how the units and tens stages are connected through their control and carry/borrow signals.

This paper does not claim a completed ASIC layout or a fabricated chip. Transistor-level layout, fabrication and laboratory power measurements were not part of this work. Timing and power figures are not provided because such data would need to come from a report for a chosen FPGA device. The focus of this work is, on simulation and RTL-level synthesis.

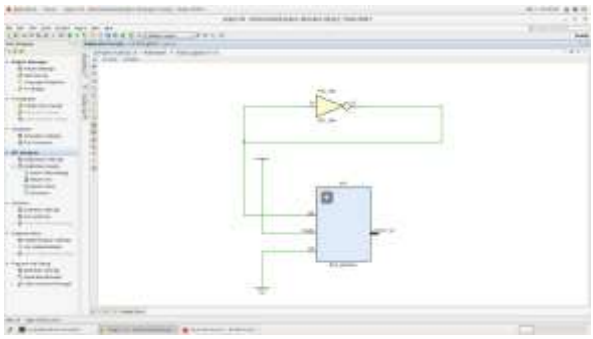


Fig. 3. RTL schematic view in AMD Vivado.

6. RESULTS AND DISCUSSION

Simulation was used to check how the 4-bit BCD Up-Down counter works. After a reset the output follows the sequence that the direction input chooses. In up mode the counter goes from 0 to 9. Then back to 0. In down mode the counter goes from 9 to 0. Then back to 9. The sequence that was planned only uses BCD states.

The waveform also shows that the counter works in a way. The clock keeps changing all the time. The stored output only changes when the clock edge is active. When the direction input changes the counter starts following the direction at the next clock edge. It does not change by itself between clock edges.

The 8-bit version takes this behavior. Uses it for two digits. The units digit changes with every count while the tens digit changes when the units part creates a carry or a borrow. Because of this the counter shows numbers from 00 to 99 when counting up and from 99 to 00 when counting down.

sThis way of arranging the circuit makes it easier to understand check and add to in the future.

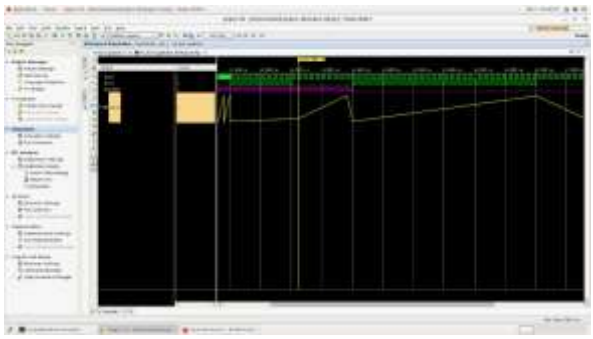


Fig. 4. Functional simulation waveform.

7. CONCLUSION

A 4-bit BCD Up-Down counter and its 8-bit two-digit version were designed in Verilog HDL and checked using AMD Vivado Design Suite. I built the 4-bit counter. The 4-bit counter counts in both directions while the 8-bit version uses two connected stages to represent two decimal digits. Simulation was used to check reset, direction control, decimal rollover and clocked state updates. In the two-digit design. Borrow conditions transfer the count between the units and tens stages. The RTL synthesis view provides a view of the logic described in HDL. Overall the project demonstrates how a small BCD counter can be built, tested and reused as a module for a decimal counter. A key advantage of this approach is that the same 4-bit block can be reused of writing a separate counter for every digit. Once the basic stage is tested additional digits can be added using the counting method. Design makes the design a useful exercise, in logic Verilog HDL, simulation and FPGA-oriented synthesis.

8. FUTURE SCOPE

The counter could be extended to three or more digits by adding more BCD stages. Such versions could be used in event counters, digital timers or clock-related circuits. Further work could include testing the design on an FPGA board connecting a BCD-to-seven-segment display driver and adding features like reset functionality or external clock inputs. This would make the counter more useful for situations. Features like enable, load, programmable limits or a clock divider. Timing how much resources are. Power consumption could also be shown after putting it on a certain FPGA device.

For a study in VLSI the RTL could go through steps that are specific to the device, like synthesis and physical design then power analysis or ASIC work. The simple synchronous design could also be looked at compared to counter types and ways to use less power.

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