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Design and Simulation of Clock Divider using VHDL

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Abstract

This paper presents the diesign and simulation of clock divider circuit using VHDL(VHSIC Hardware Description Language) on an FPGA(Field Programmable Gate Array). The clock divider circuit is a fundamental component in digital system for generating lower frequency clocks from a higher frequency reference clock. The paper starts up with simple divider where the clock is divided by even numbers, odd numbers and then later expands it into non- integer dividers.

Keywords:- clock divider, D flipflop, FPGA

1. Introduction

Clock divider is also known as frequency divider, which sivides the input clock frequency and produce output clock with a lower frequency. It's commonly used in digital systems to generate slower clock signals for various purpose like reducing power consumption, sychronizing different parts of a system, or interfacing with slower components.

For power-2 integer division, a simple binary counter can be used, clocked by the input signal. The least-significant output bit alterntes at ½ the rate of the input clock, the next bit at ¼ the rate, the third bit at 1/8 the rate etc. An arrangement of flipflops are a classic method for integer-n division. The easiest configuration is a series where each flipflop is a divided-by-2.

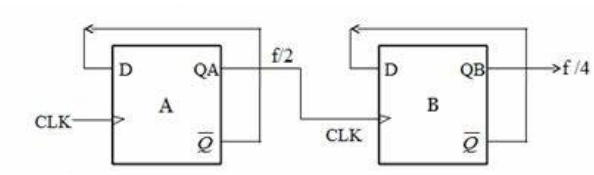

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Figure 1. Clock divider divides even number

Odd clock dividers with 50% duty cycle are designed ith the help of MOD counters that work both on the posedge and negedge of the clock and then combinational logic of the posedge and negedge counter gives the desired output.

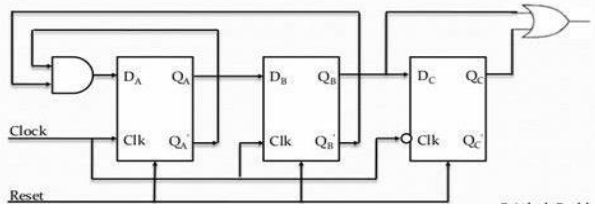

Figure 2. Clock divider divides odd number

Fractional dividers(clock divide by 1.5, 2.5 ete.) make use of the same concept as that of the odd clock dividers and the only difference between odd and fractional clock dividers is of the combinational logic.

A clock divider is to create a circuit or program that takes an input clock signal and produces an output

clock signal with a lower frequency or a divided frequency. This can be useful in various electronic applications, such as microcontrollers, digital systems, and communication devices, where you need to operate different components at different clock speeds or synchronize various parts of a system.

2. Literature survey

(1) In this article presents a CMOS 2:1 differential parametric frequency divider(PFD) design with an output frequency of 2.4 GHz and an input voltage range of 450-890 mV at 4.8 GHz. The topology is suitable for integration into RF System-on-a-Chip (SoCs), and has been constructed for sub-6 GHz applications. A design and optimization methodology for this on-chip PFD is also described in this paper. The simulation results show a performance improvement of the proposed differential PFD compared to a single-ended PFD designed for the same output frequency in the same 65nm CMOS technology.

(2) This paper describes the design and post-layout simulations of a 2/3/4-modulus frequency divider circuit, accompanied with an accumulator that controls the division count. The circuit is capable of operating as an integer or as a fractional divider. Key tpoic of this paper is the merging of div-2/3 and ¾ circuits into a single compact circuit that solves an issue of a forbidden state in fractional- division operation. The circuit is designed with 28-nm CMOS technology and the post-layout simulations indicate an operating input frequency range of 0.3-5.4 GHz with 13-bit fractional frequency resolution between division ratios of 2-4.

(3) An approach of representing a transient train of impulses under sinusoidal pumping is also described to model the resistive multipliers. The minimum conversion loss (CL) and the maximum conversion efficiency of parametric multipliers are derived. It is shown that, at high relative frequencies, the proposed time-varying response is theoretically capable of achieving higher maximum efficiency that what is calculated with conventional idler- based multiplier.

(4) A 0.045- to 2.5- GHz wideband frequency synthesizer (FS) employing time-to-digital converter (TDC) based automatic frequency calibration (AFC) method and phase switching (PS) multi-modulus divider (MMD) is presented in this paper. The traditional counter-based AFC method takes several reference cycles to calculate the instantaneous voltage-controlled oscillator (VCO) frequency, while the proposed TDC-based technique consumes only 2 cycles. In order to suppress the quantization noise caused by the sigma-delta modulator(SDM) in the MMD, the loop division step is reduced from 2 to 0.5 by adopting the PS technique. The FS is designed and implemented using TSMC 180nm RF CMOS process and provides the phase noise performance of -99.5/-123.5 dBc/Hz at 10kHz/1MHz offsets under 2.4 GHz carrier frequency. The AFC time measurement results for a 6-bit cap-array are 1.25-, 2.5- and 5- $\mathrm {\mus}$ when employing 48-, 24- and 12-MHz reference frequencies respectively. The chip area including pads and I/Os is 2.31 mm $^{\mathbf{2}}$ and the total power consumption is 108 mW.

(5) A new method is discussed for the systematic synthesis, design, and performance optimization of single-ended varactor-based 2:1 parametric frequency dividers (PFDs) exhibiting an ultralow-power threshold. For the first time, it is analytically shown that the <inline-formula> <tex-math notation= “ LaTex”>${P_{\mathrm{th}}}$ </tex-math></inline-formula>-value exhibited by any PFD can be expressed as an explicit closed-form function of the different impedances forming its network. Such a unique and unexplored property permits reliance on linear models, during PFD design and performance optimization. The validity of our analytical model has been verified, in acommercial circuit simulator, through the time- and frequency-domain algorithms. To demonstrate
the effectiveness of our new synthesis approach, we also report on a lumped prototype of a 200:100 MHz PFD, realized on a printed circuit board (PCB).

3. Design Methodology

Step 1. Determine the specific requirements for clock divider, such as the input clock frequency, the desired output frequencies (divided by even and odd numbers), and any additional features or constraints.

Step 2. Choose an appropriate division technique based on the requirements. For example, you could use flip-flops, counters, or other digital logic components to achieve the desired division ratios.

Step 3. Design the logic to divide the input clock by even numbers. This typically involves using flip-flops and logic gates to create a divided-by-2, divided-by-4,divided-by-8, etc.

Step 4. Design the logic to divide the input clock by odd numbers. This can be achieved by combining the even division logic with additional flip-flops and logic gates to create a divided-by-3,divided-by-5, divided-by-7, etc.

Step 5. Integrate the even and odd division circuits together to create a single clock divider that can divide by both even and odd numbers. This might involve multiplexers or other control logic to select between the even and odd division paths based on the desired output frequency.

Step 6. Simulate the design using digital logic simulation tools to verify its functionality and performance. Ensure that the divider meets the specified requirements and operates correctly under various conditions.

Step 7. Once the design is verified, synthesize it into hardware description language (HDL) code and implement it on the target FPGA or ASIC device.

Step 8. Test the implemented clock divider on the hardware platform, and debug any issues tha arise. Verify that it meets all functional and timing requirements.

Step 9. Depending on the specific requirements and constraints, you may need to optimize the design for factors such as power consumption, area utilization, or maximum operating frequency.

Step 10. Document the design methodology, implementation details, and test results for future reference and maintenance.

4. Result

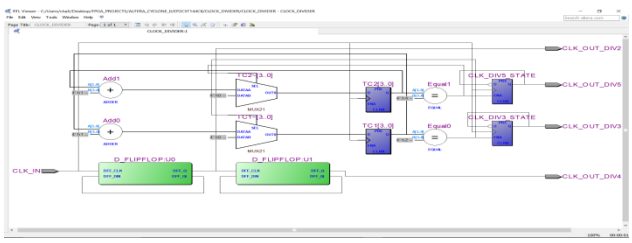

Figure 3. Clock divider RTL Diagram

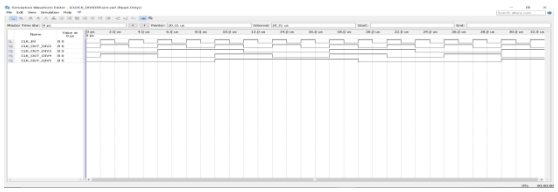

Figure 4. Clock divider simulation waveform

Clock to Output Times

	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
1	CLK_OUT_DIV3	CLK_IN	7.066	7.066	Rise	CLK_IN
2	CLK_OUT_DIV5	CLK_IN	6.807	6.807	Rise	CLK_IN
3	CLK_OUT_DIV2	D_FLIPFLOP:U0|DFF_Q	4.175		Rise	D_FLIPFLOP:U0|DFF_Q
4	CLK_OUT_DIV4	D_FLIPFLOP:U0|DFF_Q	6.339	6.339	Rise	D_FLIPFLOP:U0|DFF_Q
5	CLK_OUT_DIV2	D_FLIPFLOP:U0|DFF_Q		4.175	Fall	D_FLIPFLOP:U0|DFF_Q

Table 1.

Minimum Clock to Output Times

	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
1	CLK_OUT_DIV3	CLK_IN	3.294	3.294	Rise	CLK_IN
2	CLK_OUT_DIV5	CLK_IN	3.248	3.248	Rise	CLK_IN
3	CLK_OUT_DIV2	D_FLIPFLOP:U0|DFF_Q	1.807		Rise	D_FLIPFLOP:U0|DFF_Q
4	CLK_OUT_DIV4	D_FLIPFLOP:U0|DFF_Q	2.947	2.947	Rise	D_FLIPFLOP:U0|DFF_Q
5	CLK_OUT_DIV2	D_FLIPFLOP:U0|DFF_Q		1.807	Fall	D_FLIPFLOP:U0|DFF_Q

Table 2.

Unconstrained Paths			
	Property	Setup	Hold
1	Illegal Clocks	0	0
2	Unconstrained Clocks	0	0
3	Unconstrained Input Ports	0	0
4	Unconstrained Input Port Paths	0	0
5	Unconstrained Output Ports	4	4
6	Unconstrained Output Port Paths	4	4

Table 3.

5. Conclusion

In this paper, clock dividers (clock divided by even, odd and fractional numbers) are presented. This paper not only describeds how a clock's frequency can be divided by 2^n which usually have a 50 % duty cycle but also how frequency can be divided by (2n+1) with 50 % duty cycle. This paper also gives the idea of unusual clock division i.e. fractional clock dividers. Fractional clock dividers have a duty cycle of about 40-60 %. Thus our objective of studying clock dividers is complete and verified.

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