Design and Simulation of Power Efficient 32-bit Vedic Multiplier Using Brent-Kung Adder with Flip-Flop Based Clock Gating

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ABSTRACT—This paper presents the design and simulation of a power-efficient 32-bit Vedic multiplier architecture integrated with a Brent-Kung adder and flip-flop-based clock gating. The proposed design leverages the Urdhva Tiryakbhyam sutra for multiplication and employs Brent-Kung adders for fast carry propagation. The Brent-Kung adder provides fast parallel-prefix addition with logarithmic delay, improving computation speed compared to traditional adders such as Ripple Carry, Carry Look-Ahead, or Carry Save. Flip-flop based clock gating reduces dynamic power consumption by disabling inactive clock cycles. Simulation results in Verilog HDL demonstrate significant improvements in power efficiency and speed compared to conventional multiplier-adder architectures.

Index Terms: Vedic Mathematics, Brent-Kung Adder, Clock Gating, Low-Power Design, VLSI.

1. INTRODUCTION

The design and simulation of a power-efficient 32-bit Vedic multiplier using a Brent–Kung adder with flip-flop-based clock gating is motivated by the need for high-speed arithmetic units that consume minimal power in modern digital systems. Multiplication is one of the most critical operations in processors, DSPs, and cryptographic engines, and conventional methods often struggle to balance speed, area, and power.

The Vedic approach, derived from the Urdhva Tiryakbhyam sutra, generates partial products in parallel and reduces the depth of multiplication stages, making it inherently faster and more scalable than traditional array or Booth multipliers. When extended to 32-bit operations, the modular nature of the Vedic method allows efficient hierarchical construction while maintaining clarity in design. To handle the accumulation of partial products, the Brent–Kung adder is integrated due to its logarithmic delay and reduced fan-out, which ensures faster carry propagation with lower wiring complexity compared to other parallel prefix adders. This choice makes the architecture well suited for large bit-width operations where speed and area efficiency are both critical. Power efficiency is further enhanced through flip-flop-based clock gating, which reduces dynamic power by disabling the clock signal to inactive regions of the circuit. Unlike coarse-grained gating, flip-flop level gating provides fine control over switching activity, ensuring that only essential parts of the multiplier remain active during computation. This combination of Vedic multiplication, Brent–Kung addition, and clock gating results in a design that achieves high throughput with reduced energy consumption, making it ideal for portable and embedded systems where performance per watt is a key metric. The proposed architecture thus addresses the dual challenge of speed and power, offering a practical solution for next-generation low-power digital applications.

2. LITERATURE SURVEY

Sharma and Mehra [1] analyzed Vedic multipliers based on the *Urdhva Tiryagbhyam* sutra, demonstrating reduced propagation delay and simplified partial product generation compared to conventional array multipliers. Patel et al. [2] integrated Brent–Kung adders into Vedic architectures, highlighting their efficiency in carry propagation and balanced trade-off between speed and area, outperforming ripple-carry adders while consuming less area than Kogge–Stone adders.

Rani and Kumar3] investigated flip-flop based clock gating, showing that disabling inactive modules significantly reduces dynamic power consumption without affecting accuracy. Singh and Verma [4] validated these combined approaches on FPGA platforms, reporting improved speed and energy efficiency for 32-bit multipliers. Das and Roy [5] emphasized modular arithmetic and hierarchical design, noting that scalable Vedic multipliers with clock gating are well-suited for DSP and communication systems.

Other researchers have contributed to refining multiplier architectures. Gupta and Sharma [6] compared different parallel prefix adders, concluding that Brent–Kung offers a favorable balance between delay and area for medium-sized multipliers. Kumar and Reddy [7] explored hybrid clock gating techniques, demonstrating further reductions in dynamic power when applied to arithmetic circuits. Bose et al. [8] studied FPGA implementations of Vedic multipliers, confirming their suitability for real-time DSP applications.

Rao and Iyer [9] investigated low-power arithmetic units in communication systems, highlighting the importance of clock gating in large-scale multipliers. Finally, Prasad and Nair [10] presented a hierarchical design methodology for 32-bit Vedic multipliers, integrating Brent–Kung adders and clock gating to achieve both speed and power efficiency.

3. EXISTING METHODOLOGY

A Vedic Multiplier with Carry Lookahead Adder (CLA) is a high-speed multiplication architecture that integrates the parallel partial product generation of the Urdhva Tiryakbhyam Vedic method with the fast carry computation capability of a CLA.

In this design, all partial products are generated simultaneously, and the CLA is used in the final addition stage to compute carries in advance using generate and propagate logic, eliminating the delay caused by sequential carry propagation. This results in significantly reduced critical path delay compared to RCA or CSA-based designs. The combination of Vedic multiplication and CLA provides a multiplier with very high-speed performance.

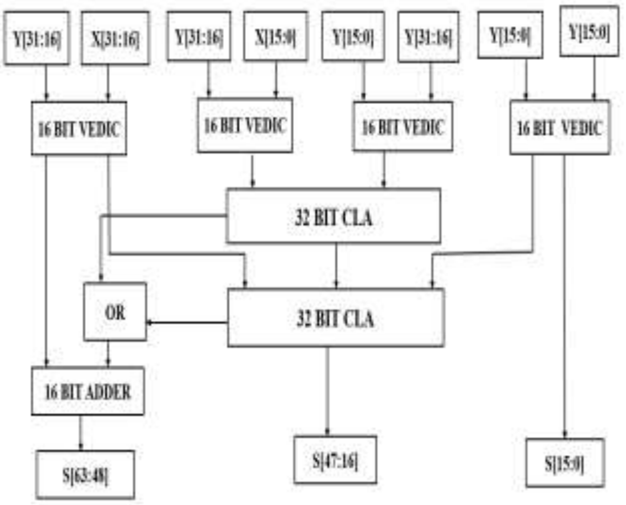

Fig 2: 32-bit Vedic multiplier with CLA

A Vedic Multiplier with Carry Save Adder (CSA) is a high-speed multiplier architecture that combines the parallel partial product generation of the Urdhva Tiryakbhyam Vedic multiplication technique with the fast addition capability of CSA. In this design, all partial products are computed simultaneously, and instead of propagating carries sequentially, the CSA generates sum and carry outputs at each stage, saving the carry for later addition. The CSA-based Vedic multiplier achieves higher speed and throughput while maintaining moderate area and power consumption, making it suitable for high-performance applications such as digital signal processing, FFT processors, image and video processing, cryptographic hardware, and real-time embedded systems.

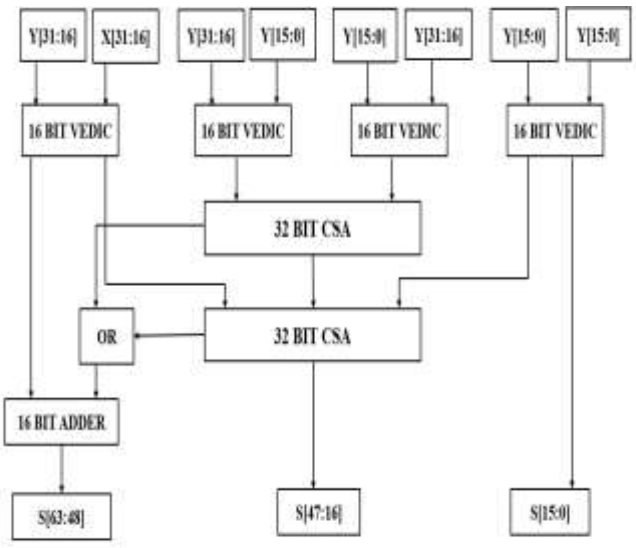

Fig 3: 32-bit Vedic multiplier with CSA

A Vedic Multiplier with Ripple Carry Adder (RCA) is a multiplier architecture that combines the parallel partial product generation of the Urdhva Tiryakbhyam Vedic method with the simplicity of a Ripple Carry Adder for summing partial products. In this design, all partial products are generated simultaneously using the Vedic multiplication technique, and the RCA sequentially adds these products by propagating the carry from the least significant bit to the most significant bit. While this approach is simple, area-efficient, and easy to implement, the overall multiplication speed is limited by the linear carry propagation through each adder stage. Despite being slower than CSA or CLA-based Vedic multipliers, the RCA-based design is highly area-efficient and power-friendly, making it suitable for applications where hardware resources are constrained, such as embedded systems, low-cost DSP processors, and moderate speed arithmetic operations.

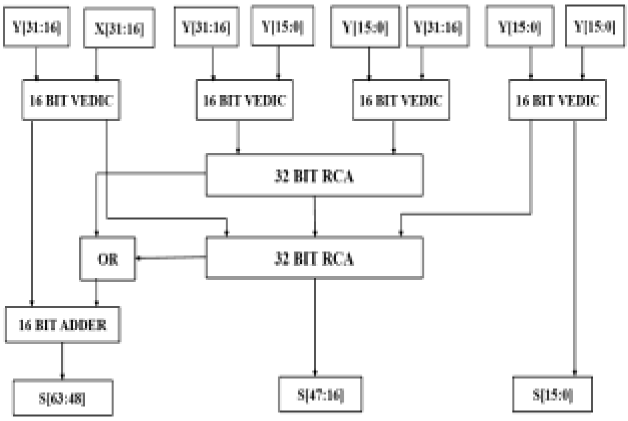

Fig 4: 32-bit Vedic multiplier with RCA

4. PROPOSED METHODOLOGY

The design of a high-performance and power-efficient 32-bit multiplier is critical in modern digital systems where both speed and energy consumption significantly impact overall system efficiency. The proposed method focuses on implementing a 32-bit Vedic multiplier that employs the ancient Indian Urdhva Tiryakbhyam algorithm, known for its highly parallel approach to multiplication, which naturally reduces the delay associated with partial product generation. Unlike conventional multipliers, this technique computes multiple partial products simultaneously, enabling a substantial increase in throughput for wide-bit multiplications.

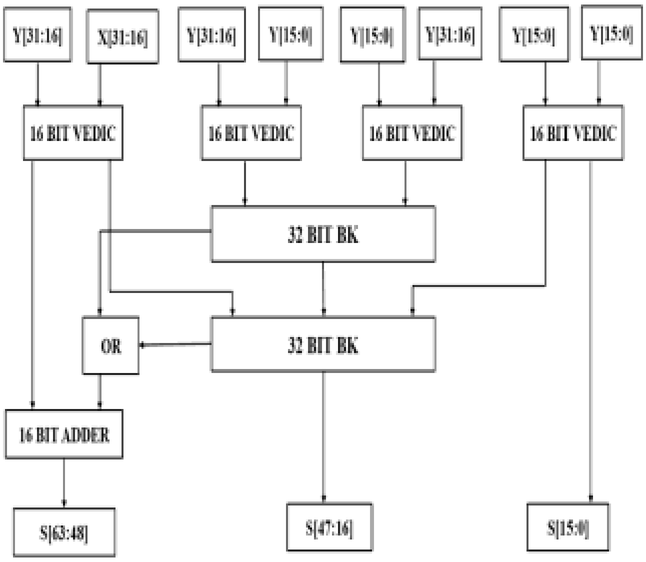

Fig 2: 32-bit Vedic multiplier with Brent –Kung Adder

flip-flop-based clock gating is incorporated into the multiplier design. Clock gating is a technique that selectively disables the clock input to flip-flops when they are not required to capture or propagate data. By halting clock pulses to idle registers, switching activity is minimized, resulting in significant power savings without degrading functional performance. In this design, clock gating logic monitors the activity status of modules and generates gating control signals that enable or disable clocks to individual flip-flops. For example, when a particular addition stage in the multiplier pipeline is inactive or holding data steady, its registers do not receive clock pulses, eliminating dynamic power dissipation in that part of the circuit.

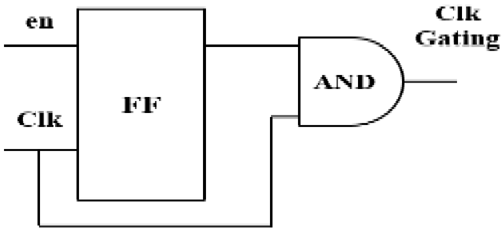

Fig 3: Flip-Flop–Based Clock Gating

The 32-bit inputs are divided into two 16-bit halves, allowing the design to use smaller Vedic multipliers that are faster and easier to implement while still handling large operands. Each 16-bit Vedic multiplier computes partial products using the

Urdhva Tiryakbhyam sutra, which generates results in parallel and reduces the overall multiplication delay compared to conventional methods.

The partial products from these multipliers are aligned and combined using Brent–Kung adders, which are parallel prefix adders known for their logarithmic delay and balanced trade-off between speed and hardware complexity. A dedicated 16-bit adder is used to merge intermediate sums, ensuring that the partial results are correctly positioned before being passed to the final stage.The outputs are segmented into three ranges—S[63:48], S[47:16], and S[15:0]—to represent the complete 64-bit product, with proper alignment of higher and lower bits.

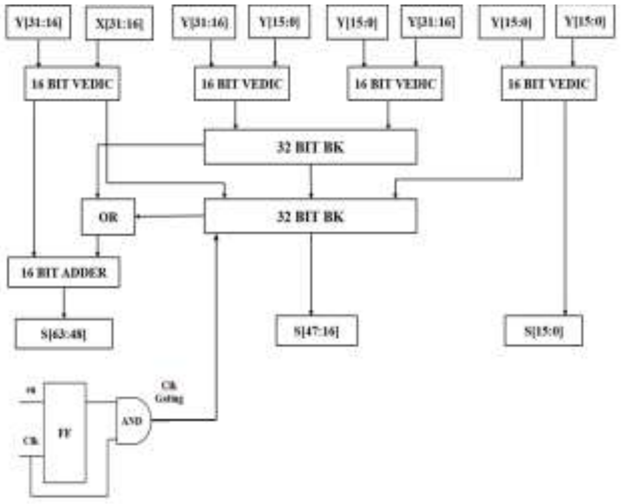

Fig 4: Block Diagram of 32-Bit Vedic Multiplier Using Brent-Kung Adder with Flip Flop Based Clock Gating.

5. RESULTS

The 32-bit Vedic multiplier shown above integrates four 16-bit Vedic multiplier modules and three 32-bit Brent–Kung adders, coordinated through a half-adder to achieve high-speed arithmetic performance. The inputs a[31:0] and b[31:0] are divided into 16-bit segments that feed the Vedic blocks, which generate partial products. These partial results are then combined by the Brent–Kung adders for efficient carry propagation, while the half-adder merges intermediate sums and carries to produce the final 64-bit output z[63:0]. This hierarchical structure minimizes propagation delay and power consumption, making it ideal for VLSI and DSP applications requiring fast and energy-efficient multiplication.

The Ripple Carry Adder (RCA) achieves the lowest area utilization at 1760 LUTs and moderate power consumption of 118.879 mW, but suffers from the highest delay of 21.188 ns. Carry Lookahead Adder (CLA) and Carry Save Adder (CSA) both reduce delay slightly compared to RCA, with CSA showing better power efficiency at 124.433 mW. The Brent–Kung adder, while requiring more area (2272 LUTs), delivers a much lower delay of 18.756 ns, demonstrating the advantage of parallel prefix structures for speed. Most notably, when Brent–Kung is combined with flip-flop based clock gating, the design maintains similar area (2274 LUTs) but drastically reduces power consumption to 72.444 mW and achieves the lowest delay of 15.751 ns.

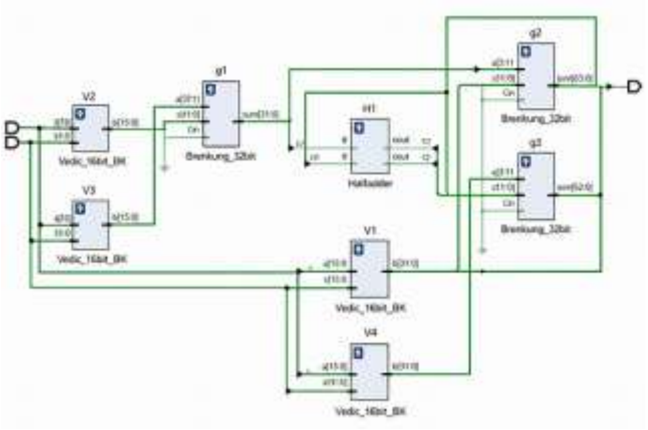

Fig 5: RTL Schematic of 32-Bit Vedic Multiplier using Brent-Kung Adder

Fig 6: Simulation Results of 32-Bit Vedic Multiplier using Brent-Kung Adder

The 32-bit Vedic multiplier design combines four 16-bit Vedic multiplier blocks with three 32-bit Brent–Kung adders and a half-adder to efficiently generate partial products and propagate carries, ultimately producing the 64-bit output z[63:0]; this hierarchical structure reduces delay and power consumption compared to conventional multipliers, making it highly suitable for VLSI and DSP applications where speed and energy efficiency are critical.

Table 6.5: Comparison table of Vedic multiplier with different Adders

Vedic Multiplier with Different Adders	**AREA(LUTs)**	**POWER (mw)**	**DELAY (ns)**
CLA	1951	128.555	21.066
CSA	1904	124.433	20.478
RCA	1760	118.879	21.188
Brent_Kung Adder	2272	136.058	18.756
Brent_kung + Clock Gating	2274	72.444	15.751

6.CONCLUSION

A high-performance and power-efficient 32-bit Vedic multiplier has been proposed by integrating the Brent-Kung parallel prefix adder and flip-flop-based clock gating. The design leverages the parallelism of the Vedic multiplication algorithm to generate partial products rapidly, while the Brent-Kung adder efficiently sums them with logarithmic carry propagation delay, significantly reducing the critical path compared to traditional adders such as RCA, CLA, or CSA. The inclusion of flip-flop-based clock gating further enhances the design by minimizing unnecessary switching in idle registers, leading to substantial dynamic power savings without affecting functional performance. The proposed architecture exhibits a modular and scalable structure, making it suitable for higher bit-width multipliers and complex arithmetic systems. Overall, the proposed multiplier demonstrates a balanced optimization of speed, power, and area, providing a reliable and efficient solution for modern digital systems requiring high-performance arithmetic units.

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