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# Design and Verification of an Efficient Packet Based Switching Network-on-Chip

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**Abstract -** With large number of cores and increased delay in SoCs, traditional point to point or bus based communication architecture becomes a new bottleneck. Traditional communication architectures cannot meet system requirements of bandwidth, latency, and power consumption.Integrated switching network has been proposed as an alternative approach to interconnect cores in SoC. Such network rely on a scalable and reused communication platform, called network on chip ( NoC ) system,to meet two major requirements: reusability and scalable bandwidth. The NOC architecture is a m × n mesh of switches and resources are placed on the slots formed by the switches. We assume a direct layout of the 2-D mesh of switches and resources providing physical-architectural level design integration. Each switch is connected to one resource and four neighboring switches, and each resource is connected to one switch. A resource can be a processor core, memory, an FPGA, a custom hardware block or any other intellectual property (IP) block, which fits into the available slot and complies with the interface of the NOC. The NOC architecture essentially is the on-chip communication infrastructure comprising the physical layer, the data link layer and the network layer of the OSI protocol stack. We define the concept of a region, which occupies an area of any number of resources and switches. This concept allows the NOC to accommodate large resources such as large memory banks, FPGA areas, or special purpose computation resources such as high performance multi-processor.

***Key Words***: Network-on-Chip, virtual channel router, SoC, verilog

## 1.INTRODUCTION

Traditional system on chips (SoCs) are based on buses. They introduce wiring delay, noise, power dissipation, signal reliability and synchronization problems. The interconnect architecture for on-chip communication is called Network on Chip (NoC).It provides a high performance communication infrastructure [1].

Networks-on-Chip (or NoCs) [2] have all requirements to be the future Systems-on-Chip (SoCs). It is composed by a set of routers and point-to-point channels interconnecting routers in a structured way. Each router has a set of ports which are used for connection with its neighbors and with the scalar processors, DSPs, controllers, memories, of the system [2][3].NoC can be used in many industrial application , such as 4G phone processor , Play station processors, video interconnecting device for TV...etc

Traditional computer networks consider collision between packets as an unavoidable problem, and the ultimate aim of computer networks is to reduce the probability of collision, but in on-chip networks the probability of dropped packets is very low. This is related to the fact that the Communication links of the router within a NoC are shorter than those in computer networks, allowing tight synchronization between routers [4].Furthermore,Some of the characteristics of an on-chip network are: low power consumption , area limited (in routing nodes), cheap wires and low interconnect delay. While the characteristics of traditional computer network are: long wires, high link latency and much complex routing nodes[4][5].

The real start of the NoC technology was in 2003 (S. Kumar and A. Jantsch and etc.)[6] discuss the design of NoC based on packet switching technology,(R.Pau)[7]in his M.sc thesis designed a router using dual crossbar to connect the input and output ports , the disadvantage of this design was the large number of slices required on FPGA . (A. Shaabany and F. Jamshidi) [8] design a NoC router using handshaking flow control , they implemented the design on FPGA and ASIC, the result of this work is compared with the results of the proposed router of this paper, while the result of the designed NoC is compared with the result of Ref.[9]

In this paper , a proposed NoC router is designed such that all input ports are connected to the output ports yielding a lattice connections between the input and output ports .The results show that NoC based on this router will minimize the number of slices and maximize the speed of flits flow.

## 2. Related work

It is being realized, by all research groups involved in system level design, that it is absolutely necessary to allow reuse of already designed components or blocks. Wentzlaff [5] have proposed an IP-centric embedded system design methodology. The major challenges in the IP centric methodologies are the interface synthesis among various IP blocks and system verification. Recently, Platform Based Design methodology [6] has been proposed which not only allows reuse of components but also reuse of system architectures and topologies. The basic idea is that an architecture, which is suitable and efficient for one application will also be suitable and efficient for many similar applications. The idea of using the same architecture (platform) for development of application not only speeds up application design but also reduces its verification time. Guerrier et. al. [7] have extended the idea of platform based design by including a layer of software on top of the hardware

platform to help application development. This layer is called Software Platform. The combination of hardware and software platforms is referred to as System Platform. It has also been realized that the key to reuse and integration of IP components is the communication from the physical to the system and conceptual level, and consequently communication centric architectures, platforms and methodologies have been developed [8, 9, 10].

The future system on a chip, incorporating many different types of processing and memory elements, has to operate using Globally Asynchronous Locally Synchronous (GALS) paradigm [15], at least at the hardware level. GALS paradigm not only avoids the problem of clock skew but also leads to lower power consumption.

## 3. Network on Chip Architecture

The NOC architecture provides the communication infrastructure for the resources. We have two main objectives. Firstly, it is possible to develop the hardware of resources independently as stand-alone blocks and create the NOC by connecting the blocks as elements in the network. Secondly, the scalable and configurable network is a flexible platform that can be adapted to the needs of different workloads, while maintaining the generality of application development methods and practices.

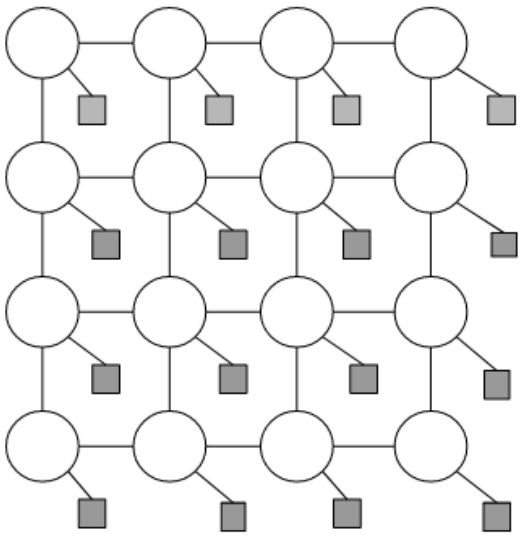

**Fig -1**: A 4 × 4 2D mesh with a single core connected to each router.

### 3.1. Noc Topology

In our network-on-chip a simple 4x4 mesh topology where x-addr and y-addr are attributed to each router and defines its X,Y coordinates. The mesh topology is chosen because of its properties such as concurrent, regularity, data transmission , and controlled electrical properties [6]. Each router can have a maximum of five input ports (north, south, west, east and local). The number of ports depends on the position of the switch in the design, since we have to eliminate any unused links that have no connections with other switches in order to reduce power consumption.

### 3.2. Switching Technique

Switching technique determines how and when internal switches of the network are set to connect router inputs to outputs for transferring messages. We adopt virtual cut through packet switching. Each packet is 36 bits where the first 6 bits represents the source address and next 6 bits indicates the destination address and next one bit represents the virtual channel id and remaining bits have the data.

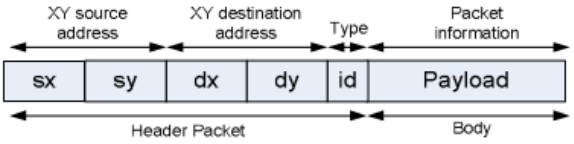


**Fig -2**: Packet format.

### 3.3. Routing

4x4 NoC routing is based upon X-Y static routing algorithm, where the X, and Y coordinates are satisfied in order. X-Y routing is presented as the vertically balanced routing algorithm which has the best performance.

The routing process at each switch can be defined by three main pipeline stages:

1) Routing calculation: At each input-port for each router, an 36 bits flit input signal is fetched and decoded in order to extract the information about the destination address and the Next-Port direction. The router then compares the actual addresses of the router and the destination addresses to define the New-Next-Port:

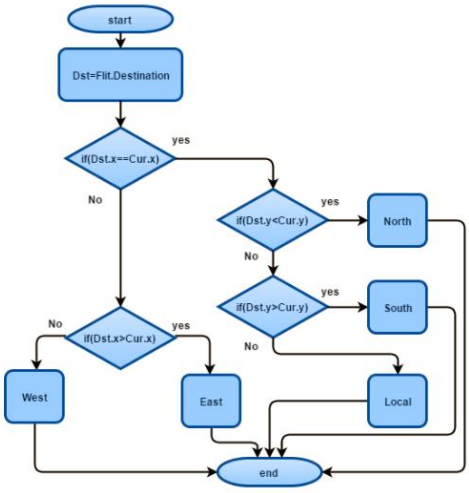


**Fig -3**: Routing Flowchart.

2) Switch allocation: After the routing calculation stage, the information about the New-Next-Port is transmitted to the switch allocator. The main function of the switch allocator is to decide which output port should be granted to which input port, and when this grant should be allocated. When several flits compete for the same output port, 4x4 NoC arbiter in the switch allocator schedules a round-robin scheme. This scheme

allows for each request to be served in a fair way, without taking into consideration priority.

3) Crossbar traversal: The switch allocator sends the sw-cntrl to the crossbar circuit where information about the selected input port and the Next-Port are embedded. Depending on the information, the crossbar sends flits to the appropriate ports. When all the flits are transmitted, the tail bit informs the switch allocator via a tail-sent signal that the flit transmission is completed and can free the used channel so it can be exploited by another flit.

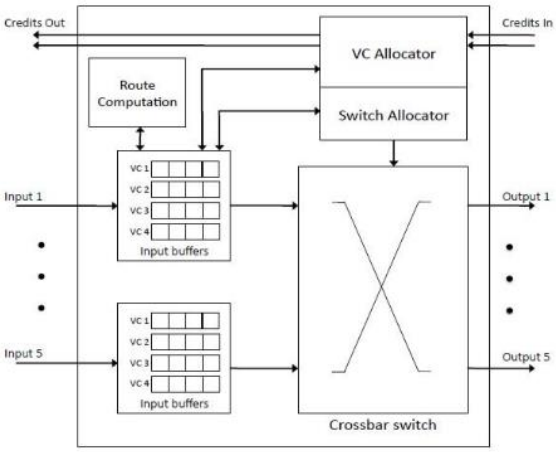


**Fig -4**: Router Architecture.

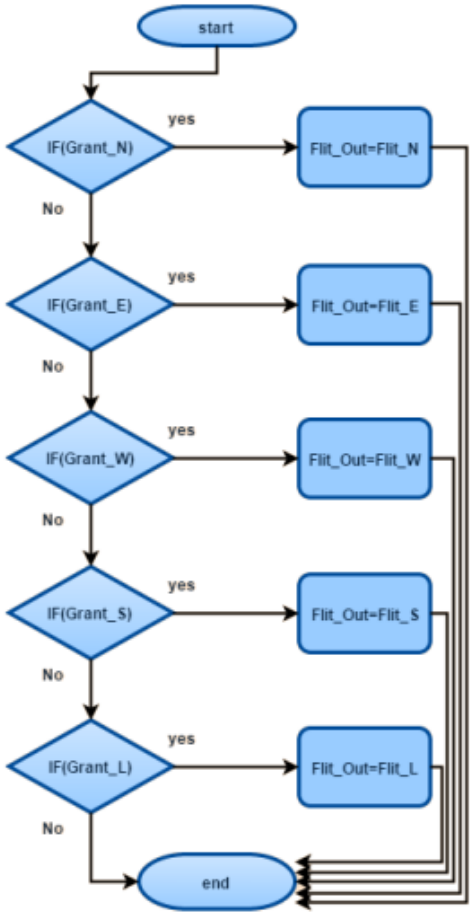


**Fig -4**: Flowchart of arbiter.

## 4. Results

Simulation results are based on test performed on iverilog The verification is done using Verilog HDL.

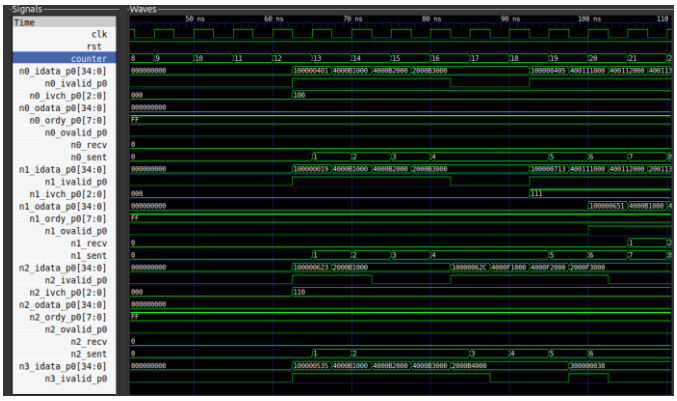

**Fig -6**: Output waveform of 4x4 NoC.

## 5. Synthesis report

Overall implementation of network on chip are shown below:

| Site Type | Used | Fixed | Prohibited | Available | Util% |
|---|---|---|---|---|---|
| Slice LUTs* | 16587 | 0 | 0 | 134600 | 12.76 |
| LUT as Logic | 16587 | 0 | 0 | 134600 | 12.76 |
| LUT as Memory | 0 | 0 | 0 | 46200 | 0.00 |
| Slice Registers | 37736 | 0 | 0 | 269200 | 14.32 |
| Register as Flip Flop | 37736 | 0 | 0 | 269200 | 14.32 |
| Register as Latch | 0 | 0 | 0 | 269200 | 0.00 |
| F7 Muxes | 38348 | 0 | 0 | 67300 | 5.98 |
| F8 Muxes | 936 | 0 | 0 | 33650 | 2.74 |

**Fig -4**: Resource utilization report**.**

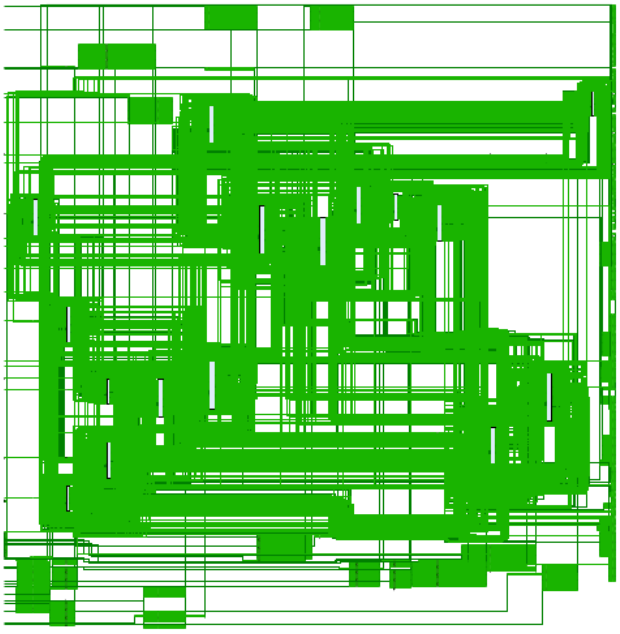

**Fig -7**: Synthesis RTL Schematic.

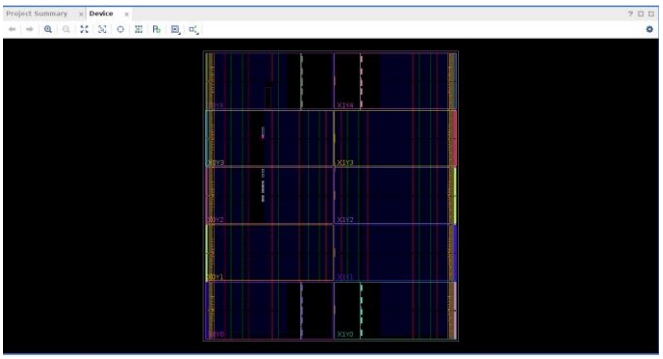

**Fig -8**: Implemented Design of 4x4 NoC.

## 3. CONCLUSIONS

The rapid scaling of devices led to the design of SoCs being communication-centric and issued numerous challenges to researchers which gave rise to Network-on-Chip technology. The field of NoC is beginning to have a tremendous influence in the design of multicore and multilayer SoC architectures.
In this paper, a 4×4 Mesh topology for NoC has been designed in Verilog with the help of iverilog and Xilinx tools. Its implementation has been done in Artix 7 FPGA and the functionality of the design has been verified. The design perfectly allows data packets to traverse through the network with a minimum latency of 4 clock cycles per router length.

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