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Design and Verification of SRAM Using GPDK using 45nm Technology

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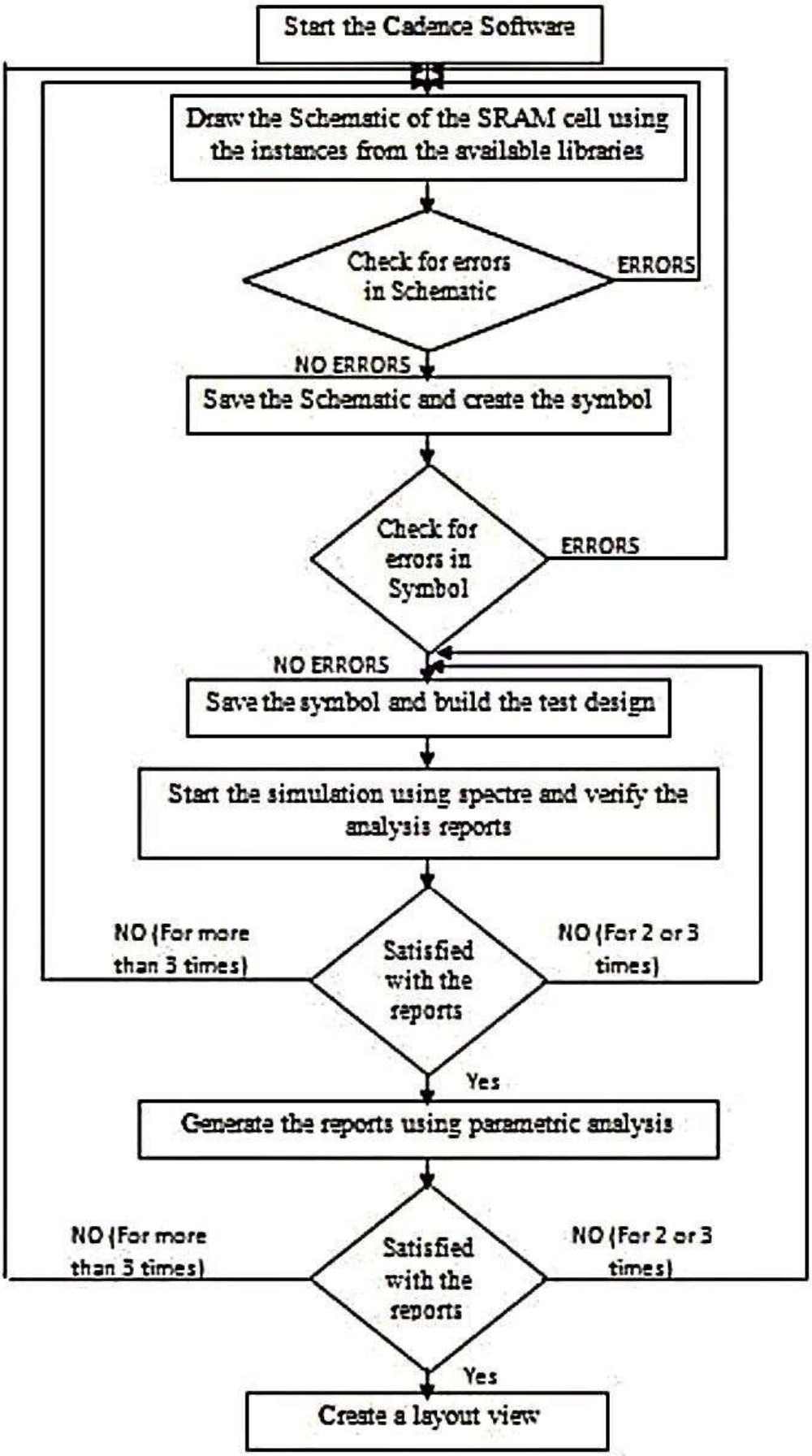
Highlights:

- Presents a complete design and verification methodology for SRAM cells using GPDK 45 nm technology in Cadence Virtuoso.
- Explains the transistor-level operation of the SRAM cell, verifying MOSFET functionality during read, write, and hold modes.
- Performs schematic design, layout implementation, and post-layout verification including DRC and LVS checks.
- Analyzes key performance parameters such as static noise margin (SNM), power consumption, access delay, and leakage current.
- Validates the correctness and reliability of the SRAM design through pre-layout and post-layout simulations under 45 nm process constraints.

Graphical Abstract:



***Abstract*— Static Random Access Memory plays vital role in cache memory, processor and in high speed computing applications. This work illustrates the design, simulation and physical verification of SRAM cell using GPDK 45nm technology in cadence. Cadence design tools are widely used in the VLSI industry for accurate circuit design and physical verification at deep sub-micron technology nodes. This paper presents the design and verification of an SRAM cell using GPDK 45 nm technology implemented in Cadence Virtuoso. The complete SRAM design flow is carried out using Cadence schematic and layout environments, ensuring accurate transistor-level modeling and physical realization. Supporting Peripherals such as pre-charge circuit, sense amplifier, read write circuit, decoder and 4*4 memory array are also designed. Functional simulation verifies the read, write and hold operations whereas physical design checks including DRC, LVS and ERC confirm that the layout is correct. It's helpful in understanding read, write and hold operation separately which was helpful in calculating the power and area as well. Simulations are helpful in determining the functionality of each circuit through the waveforms. Layout designs are useful in chip designing and comparing the schematic with layout. Based on the improving technology the designing the reliable circuits and scaling is very challenging. This paper represents the verification of six transistor SRAM using latest cadence virtuoso. It's abundantly used in chip designing, in low power portable devices and in digital processing systems. The working of MOSFETS and transistors is verified. Through this read and write noise margins are degraded. The SRAM cell must meet the requirements in nanometer range. Post-layout verification is performed through Design Rule Check (DRC) and Layout Versus Schematic (LVS) to ensure physical correctness and consistency between the schematic and layout. Key performance parameters such as static noise margin (SNM), power dissipation, access delay, and leakage current are evaluated to assess the reliability and efficiency of the SRAM design. The simulation results demonstrate stable operation and acceptable performance at the 45 nm technology node. This work provides a systematic methodology for SRAM design and verification at advanced technology nodes and serves as a practical reference for low- power memory design in contemporary VLSI applications.The final section of the paper presents simulation waveforms and performance metrics, such as static noise margin (SNM), power consumption, access delay, and leakage current, confirming reliable operation of the SRAM cell at the 45 nm technology node. Overall, the graphical abstract conveys a clear end-to-end workflow from schematic design to post-layout verification, emphasizing accuracy, reliability, and performance optimization of SRAM in advanced CMOS technology. This work demonstrates a structured and industry-relevant SRAM design flow, making it suitable for low- power cache memory and embedded system applications.**

Keyword: Memory design; SRAM cell; Cadence virtuso; DRC check; LVS; Power consumption.

INTRODUCTION

Static Random Access Memory (SRAM) is broadly used in embedded systems, processors, cache memory, buffer memory and in register files. The 6T SRAM cell is most liked choice for its low latency, low delay, high speed, low power consumption and better performance for small memory sizes. The rapid growth of portable electronics, high-performance processors, and embedded systems has significantly increased the demand for high-speed and low-power memory circuits. Among various memory types, Static Random-Access Memory (SRAM) is extensively used in cache memories and register files due to its fast access time, simple read/write operations, and compatibility with standard CMOS technology. As CMOS technology continues to scale toward deep sub-micron nodes, the design and verification of reliable SRAM cells have become increasingly challenging. At advanced technology nodes such as 45 nm, SRAM design faces critical issues including reduced noise margins, increased leakage current, process variability, and sensitivity to parasitic effects. These challenges make transistor-level accuracy and thorough physical verification essential. Hence, the use of industry-standard Electronic Design Automation (EDA) tools is crucial for achieving reliable and manufacturable memory designs. Cadence Virtuoso is widely adopted in both academia and industry for custom VLSI design, offering integrated environments for

schematic capture, simulation, layout implementation, and physical verification. This project deals with schematic design, simulation, layout design and its verification of 6T SRAM using 45nm technology. SRAM does not require cyclic refreshing as required in DRAM. The 6T SRAM cell is selected due to its low power consumption, high operating speed, low latency and better performance for small memory sizes. SRAM is a class of semiconductor memory that stored data using the cross coupled inverter which forms a latch circuit. It preserve data as long as power is supplied without use of cyclic refreshing. The 6T SRAM cells selected over 7T and 8T designs because it provides best overall balance between speed, power, area and stability. Where SRAM is a fundamental building block used in various integrated circuit due to its low access latency, high speed operations and compatibility with the other CMOS technologies. SRAM is widely used in applications because of its scaling and improved technology. As semiconductor technology scaled to achieve reliability and to reduce power consumption is challenging due to increment in leakage current and reduced supply voltage. Functional Verification of SRAM cell is carried out by simulating memory operations including read, write, and hold operations. The primary goal of this project is to develop efficient and reliable designs of SRAM cell suitable for advanced VLSI applications. The developed work demonstrates successful verification and stable operation of SRAM using generic process design kit of 45nm technology. It include design of SRAM layout through which the comparison between schematic design of SRAM and layout is verified by using layout versus schematic check and the parameters like sizing of transistors are been verified using design rule check method. The layout connection can be done by using the wires such metal 1, metal 2 and by using poly. The sizing of transistor plays important role in designing. The VLSI projects helps in understanding various technologies along with the usage of various kits. A transmitter gate scheme and bitline balancing scheme are proposed for high performance of SRAM cell. SRAM chips are often used in various devices such as cell phones, wearable and other consumer devices. It also used as printer LCD display, disk drive as buffer and in networking devices such as switch or routers. SRAM is more expensive and requires larger space than the DRAM but it does not require periodic refreshing for every time. SRAM cells are common choice in RAM design, which offers faster speed and lower power consumption compared to DRAM making it as a preferred choice. The Semiconducting memory are designed on organizing and structuring the SRAM cells in array fashion for minimal power dissipation and leakage enhancing operation under various temperature. There are many possibilities through which we can enhance the performance of cell on varying width, length, power supply or configuration for optimal result. This paper aims to achieve new configuration, which can store bits efficiently with low leakage current. Various SRAM cells have been designed such as 6t, 7t, 8t, 9t, 10t but in that 6t is effective and had efficient usage. SRAM uses bistable latching circuitry to store each bit efficiently. The performance is analyzed considering factors such as leakage current, delay SNM, static power dissipation. SRAM occupies a significant portion of the total silicon area in modern System-on-Chip (SoC) designs, especially in cache memory architectures of microprocessors and digital signal processors. Due to its non-destructive read operation and high-speed performance, SRAM is preferred over dynamic memory for on-chip storage. However, as technology scales, the increased density of SRAM arrays intensifies challenges related to power consumption, stability, and yield, making optimized SRAM design essential. At the 45 nm technology node, short-channel effects, threshold voltage variations, and increased leakage currents significantly impact SRAM cell stability. Reduced supply voltage further degrades static noise margin (SNM), increasing the probability of read and write failures. Additionally, interconnect parasitics introduced during physical layout can affect access time and power dissipation. These challenges necessitate detailed pre-layout and post-layout analysis using reliable EDA tools. The General Purpose Design Kit (GPDK) 45 nm technology provides scalable CMOS models and standard design rules, enabling realistic simulation of nanometer-scale circuits. Although GPDK is not tied to a specific foundry, it is widely used for academic research and training due to its consistency and ease of use. It allows designers to study the impact of technology scaling on circuit performance without violating foundry confidentiality. The motivation of this work is to provide a clear and systematic SRAM design and verification methodology using Cadence tools at the 45 nm technology node. The major contributions include transistor-level analysis of SRAM operation, complete schematic-to-layout flow, and performance evaluation under realistic conditions. This work serves as a practical reference for students and researchers working on low-power and reliable SRAM design.

LITERATURE SURVEY

The paper "Design and Analysis of 6T SRAM in 45NM technology" by V. Panduranga Vemula, S. Priyanka, M. Raheez, and A. Sairam (IJERT, Vol. 11, Issue 05, May 2022) presents the design and performance evaluation of a six-transistor (6T) static random-access memory cell using 45nm CMOS technology. The authors explain that the 6T SRAM cell is composed of two cross-coupled CMOS inverters that store a single bit of data and two NMOS access transistors that enable read and write operations. The paper discusses the three modes of operation—standby, read, and write—and highlights how the cell maintains data without refresh in standby mode, provides access to stored data during read, and allows overwriting during write. Using Cadence Virtuoso with GPDK 45nm libraries and Spectre simulations, the study analyzes key parameters such as power dissipation, delay, and static noise margin (SNM). Results show that scaling down to 45nm reduces power consumption and improves speed compared to larger nodes, though challenges such as leakage currents and reduced SNM affect stability [1].

The paper "Performance Analysis of 6T,8T,and 10T SRAM Cell in 45nm Technology" by M. G. Shrinivas and Bhavana M. S (IJEAT, Vol. 13, Issue 5, June 2024) provides a detailed comparative study of different SRAM cell architectures implemented in 45nm CMOS technology. The authors explain the design of conventional 6T SRAM, which is widely used due to its compact area and fast operation, but highlight its limitations in terms of reduced stability and static noise margin (SNM) at deep submicron nodes. To address these issues, they analyze 8T and 10T SRAM cells, which incorporate additional transistors to improve read stability, write margin, and overall robustness against process variations. Using Cadence Virtuoso and Spectre simulations with GPDK 45nm libraries, the paper evaluates parameters such as power consumption, delay, and SNM across the three designs. The results show that while the 6T cell is efficient in terms of area and speed, the 8T and 10T cells achieve better stability and reliability, making them more suitable for low-power and high-performance applications [2].

The paper "Performance Evaluation of 6T SRAM Cell Using 90nm Technology" by Varanasi Koundinya, Jithendra Pulivarthi, Madanu Karun Chand, and D. Jayanth Sai Kumar (IJERT, Vol. 10, Issue 09, September 2021) presents the design and analysis of a conventional six-transistor (6T) SRAM cell implemented in 90nm CMOS technology. The authors describe the structure of the cell, which consists of two cross-coupled CMOS inverters for storing data and two NMOS access transistors for enabling read and write operations. They explain the three modes of operation—standby, read, and write—and evaluate the cell's performance using Cadence Virtuoso and Spectre simulations. Key parameters such as power consumption, propagation delay, and static noise margin (SNM) are analyzed to understand the impact of the 90nm node on efficiency and stability. The results show that the 6T SRAM cell at 90nm achieves reliable performance with reduced leakage compared to larger nodes, but faces challenges in maintaining adequate SNM and robustness under process variations [4].

METHODOLOGY

Fig.1 is the schematic circuit of 6T SRAM using GPDK 45nm technology. A typical circuit of SRAM cell is made of six MOSFETs.In this two inverters connected in cross coupled form providing two stable states given as 0 or 1. In addition it consist of two nmos transistor known as access transistors which are enabled during read and write operation and also responsible for controlling the word line (WL). The state word line defines whether the connection is to be established with associated bitline such as BL and BLB. During the read operation the data is driven from the inverterts and based on the given condition sutaible data is stored in bitlines which act as a output node. In write operation BL and BLB acts as input nodes through which data is written inside the cell. During a read operation, the access transistors connect the cell to the bit lines, allowing the stored value to be sensed, while in a write operation, they enable new data to overwrite the existing state.

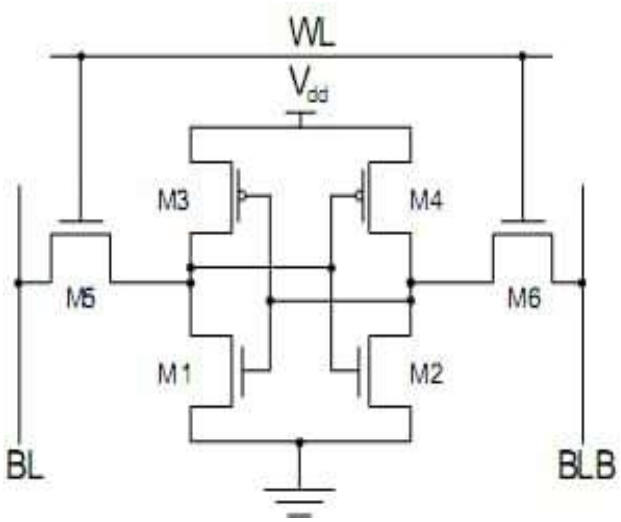


Fig. 1 SRAM cell

This SRAM cell performes three different operation such as:

1. Hold operation.
2. Read operation.
3. Write operation.

The three operation work as follows:

1. ***Hold Operation:***

Fig. 2 is the schematic diagram of hold operation. In this memory the hold operation refers to the condition in which the cell provides the data previously stored inside the sram cell .In this the is isolated from bitlines and simply store its state (‘0’ or ‘1’).During this period the Word line is kept active low, which turn off the access transistors. Because of this this the bitlines are disconnected from the cell. This ensures that the logic levels at the internal nodes (Q and Q’) remail unchanged. The SRAM cell is completely isolated from the bit lines, and the data is preserved by the positive feedback of the cross-coupled inverters. As long as the power supply is maintained, the stored data remains stable without any refresh operation. The hold operation represents the idle state of the SRAM cell when no read or write access is performed. Data retention during the hold mode is achieved through the cross- coupled inverter configuration, which provides positive feedback. The strength ratio between the pull-up and pull- down transistors plays a crucial role in ensuring reliable data retention, especially at reduced supply voltages. Larger HSNM ensures data is preserved even under voltage fluctuations or minor disturbances. Leakage current during hold contributes to static power consumption, making low-leakage design important in deep-submicron nodes. Cross- coupled inverters maintain data. One inverter reinforces the other, ensuring logic retention.

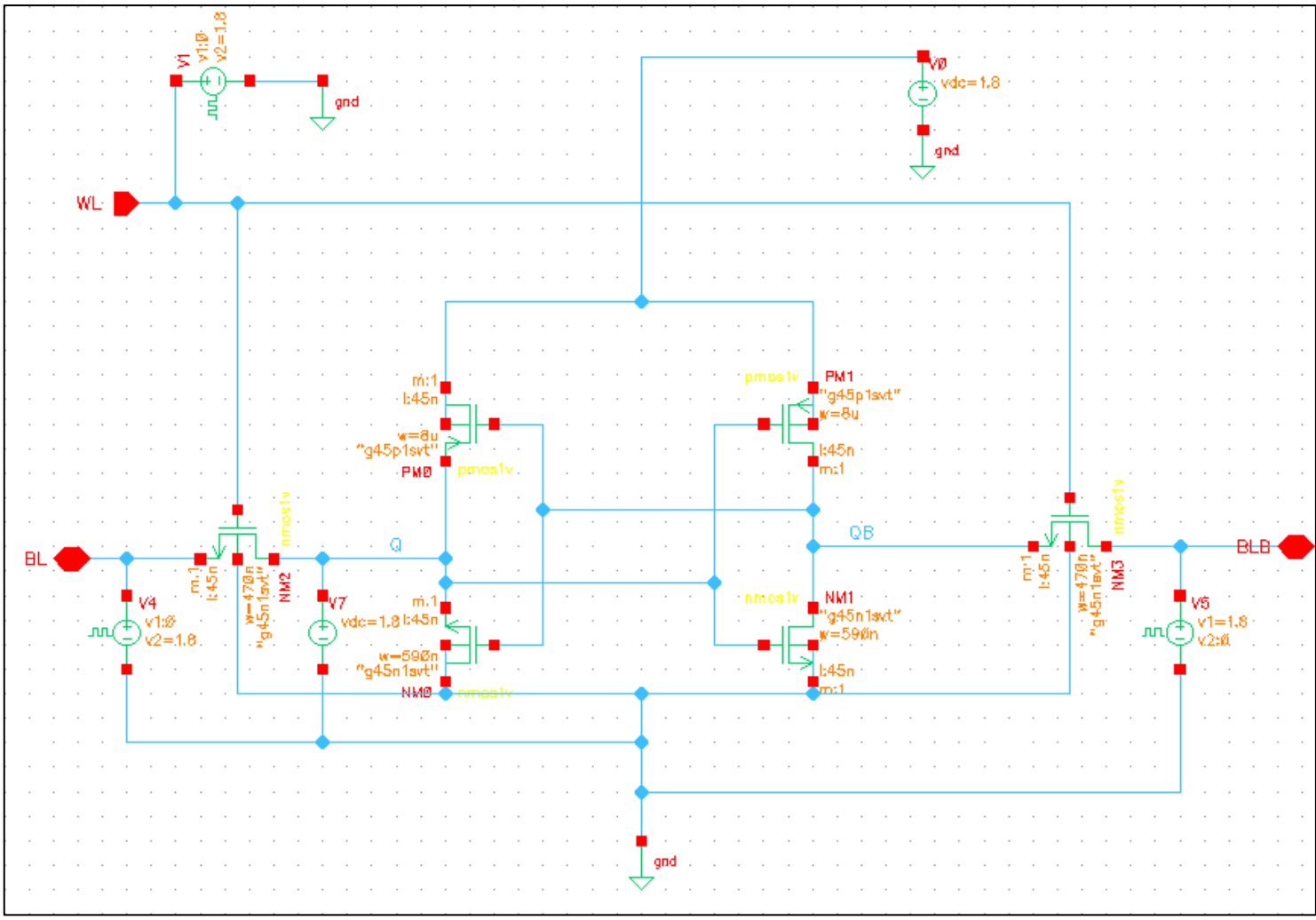


Fig.2. 6T SRAM cell hold operation schematic in cadence virtuoso

2. ***Read operation:***

Fig. 3 represents the design of read operation. In this operation, both bit lines are pre-charged to logical high (1). These Bit lines are act as output node during read operation. The word line is asserted to logic 1 which enables both the access transistors which are connected to internal nodes (Q & Q') to the corresponding bitlines. The node which store logic 0 slightly pull down its bitline through access transistor and another node which store logic 1 keeps its bitline nearer to 1. At the last any one of the bitline discharge slightly creating a small voltage difference between BLB and BL.This voltage difference is then sensed by the differential sense amplifier and provide the neccessaried output without altering it. This is accomplished by using proper transistor sizing. Overall this operation provides the sensing bitline voltage drop ensuring the original values stored inside the internal nodes. At 45 nm, parasitic capacitances reduce voltage swing, so fast and sensitive sense amplifiers are required. During read, the stored data must not flip. The node storing a '0' is weakly held by PMOS and accessed via NMOS pass-gate, so read disturbance can occur if transistor sizing is not optimized. Increasing pull-down NMOS strength improves RSNM but may impact write margin.Careful balance between read stability and write ability is required.

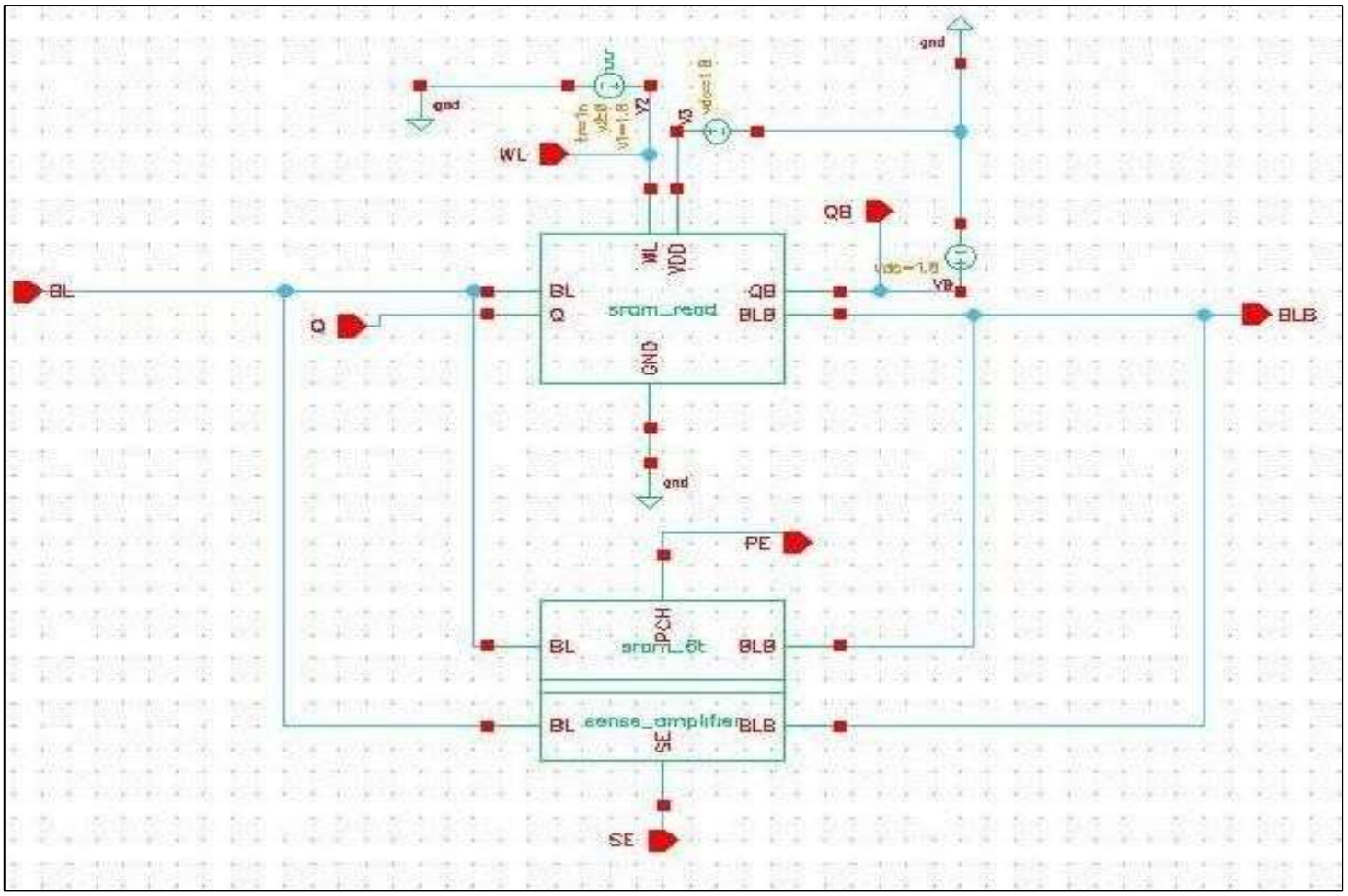


Fig.3. 6T SRAM cell read operation schematic in cadence virtuoso

3. ***Write Operation:***

Fig. 4 illustrate the design of write operation. This write operation is carried out on forcing logical values which need to be stored directly to the bitlines. The logics driven in bitlines by using write drivers the assigned value will be stored in BL and its compliment in BLB.Then the wordline is asserted to logic high, turning on the access transistors which helps in connecting bitlines to its corresponding internal nodes. Then the updated values are written inside the sram cell. Then the word line is lowered which helps in isolating the cell allow the cross coupled inverters to store the updated data. The ability to successfully write depends on the ratio of access transistor strength to pull-up transistor strength. This ensures the input data can overwrite the previous value. The write operation is characterized by voltage forcing through strong bit-line drivers, while the read operation relies on detecting a small voltage difference on the bit lines without disturbing the stored data. The write static noise margin (WSNM) quantifies how easily the stored value can be overwritten. Higher WSNM ensures robust writes even under process variations.

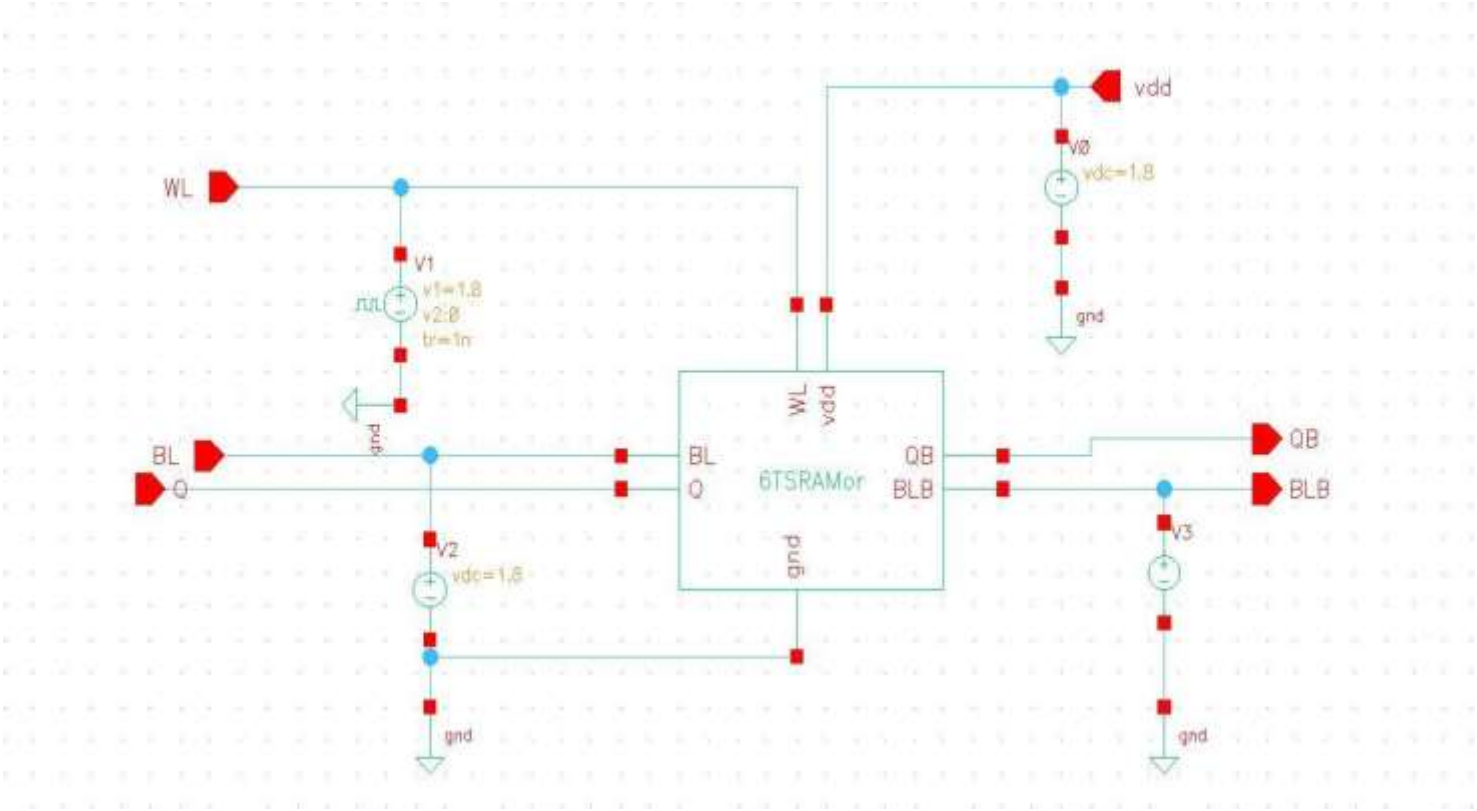


Fig.4. 6T SRAM cell write operation schematic in cadence virtuoso

4*4 MEMORY DESIGN

A 4*4 memory array is a small block giving total storage capacity of 16 bits.

Fig. 5 shows the memory organization interfaced with precharge circuitry, row decoder, write driver circuit,sense amplifier and 6t cell to achieve write,hold and read operation. One the left side of memory array, a 2:4 decoder using AND gate is implemented to activate single horizontal wordlines during each memory access,where other wordlines are deactivated to prevent undesired cell operations. The first horizontal line in the memory corresponds to precharge circuitry. Before read functionality the bitlines BL and BLB corresponding to each column are precharged to vdd. Next four rows consists of 6t sram cells to perform hold,write and read operation .In which each row is connected to unique word line driven by row decoder.In last row first row consist of write driver circuit to load new data to be written. And last row consists of sense amplifier block, which detects the small voltage difference developed between BLB and BL in read operation.

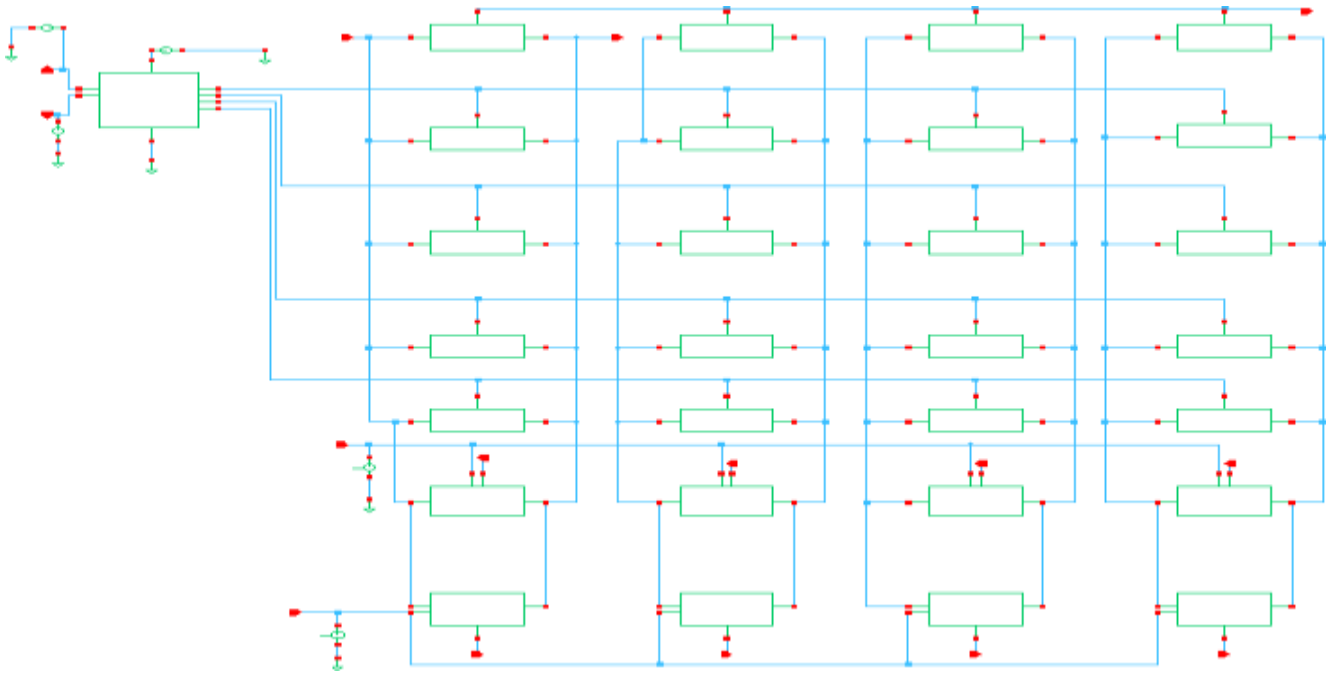


Fig5. Design of 4*4 memory array

Layout

The layout of the 6t SRAM cell is implemented using symmetrical structure to ensure minimum area and resilient read write operation. To make sure both write stability and read stability, transistors size must satisfy certain dimensional limitation. Additionally, to achieve great layout density, transistors size must be designed to be as small as possible. The layout of SRAM is designed to determine the achievable cell density and the area occupied by single bit.The connection of the cella are implemented with metal 1 for wires and poly silicon gates.

Layout of the proposed 6T SRAM is in Fig 6. The layout design and area efficiency are continuous reduce in scale, size or extent for CMOS technology that strengthens the efforts for more compact structure and contraction of circuit element. LVS check is used to ensure that the physical layout of circuit matches its schematic.The check verifies pin names, transistor sizing and interconnection are identical in both representation.The LVS has been verified it shown in Fig 7.

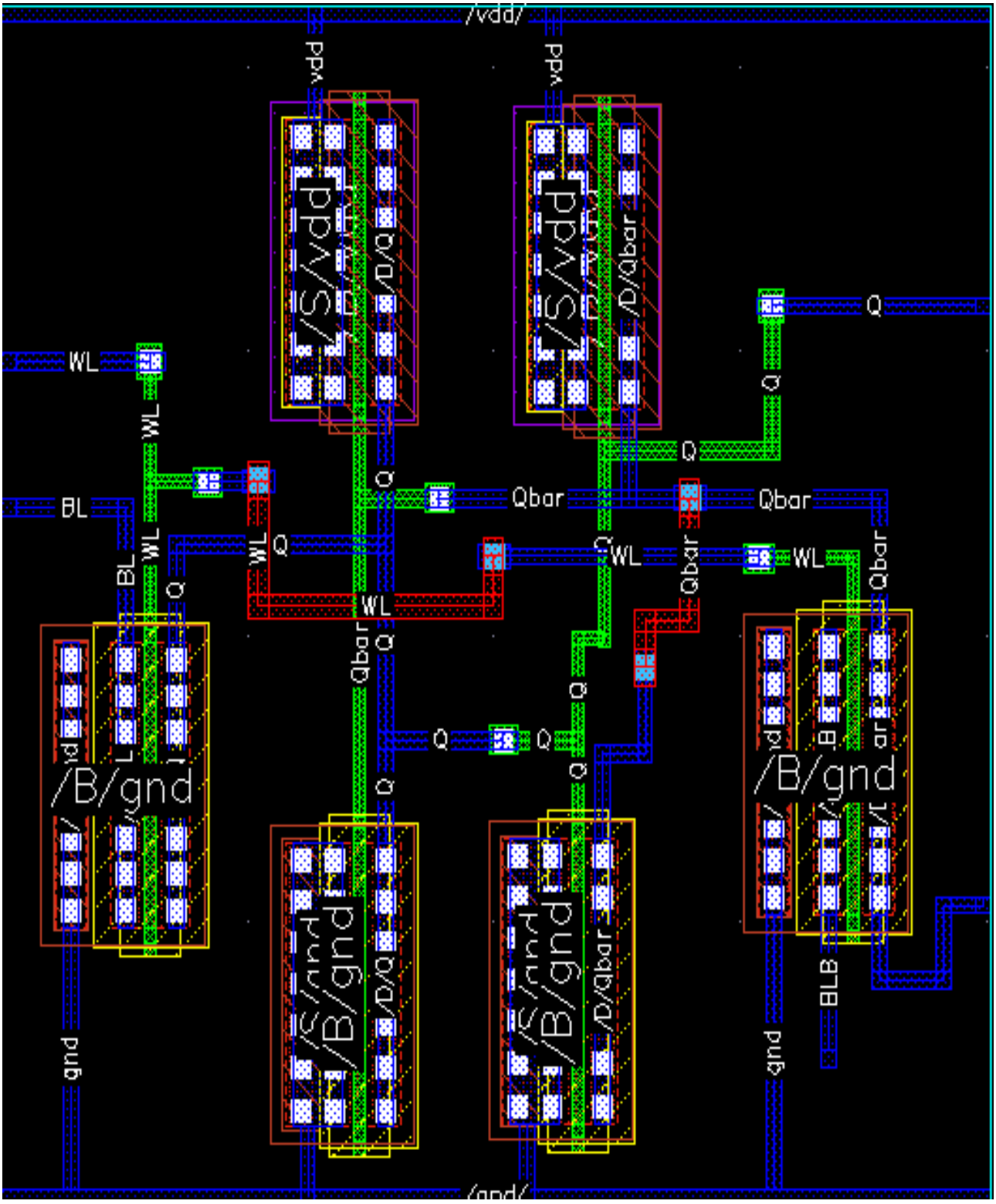


Fig.6. Layout of 6T SRAM Cell

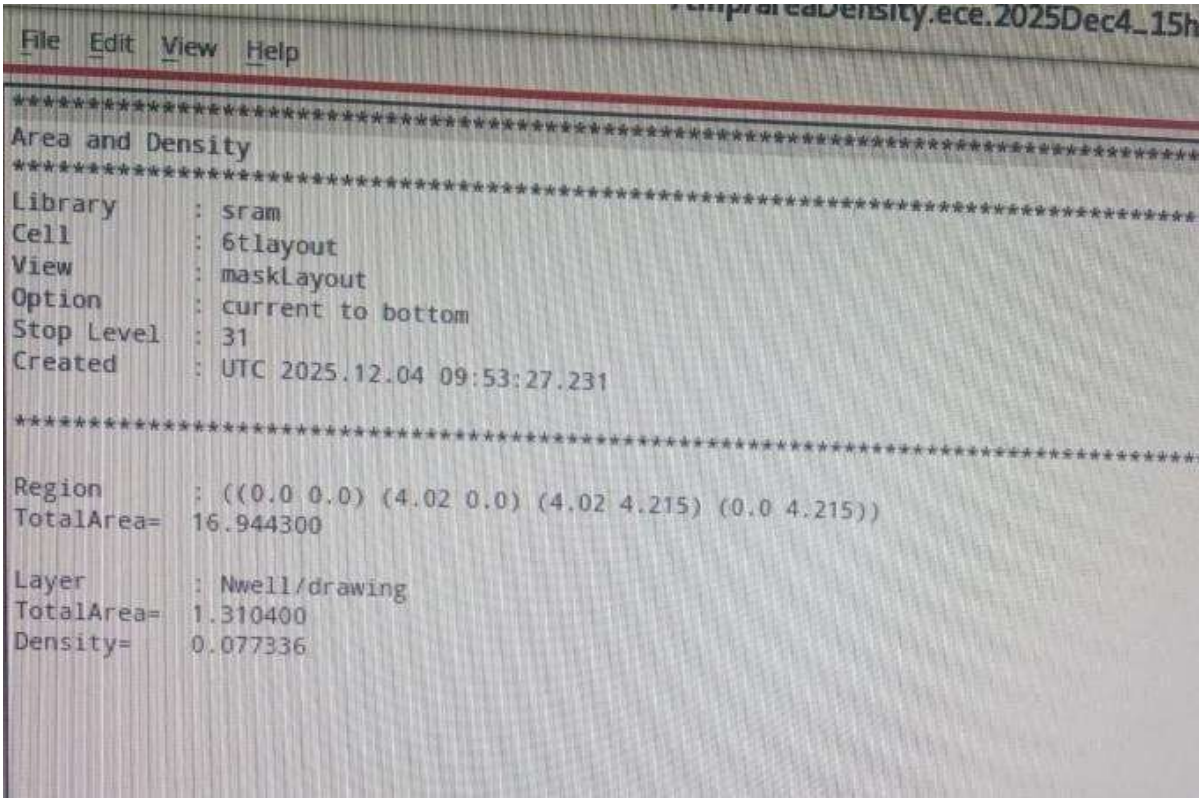


Fig.7: Area & Density measurement.

RESULT

Cadence simulation is for analyzing of DC waveform which has given a good result in 45nm technology. Here, the analyzsis was done by the support of DC simulation results by giving inputs as a DC signal to understand the capability of the SRAM cell. Power consumed has been calculated with the help of Cadence tool during simulation.

The Waveform of 4*4 memory array is given in below figure 8 to check how the read and write operations are performed together by using suitable peripherals.Instead of using dummy input how practicslly the same operation is been verified by using memory cell is analyzed by verifying dc simulation.Also usedsed to dermine the power and delay consumed by the design.

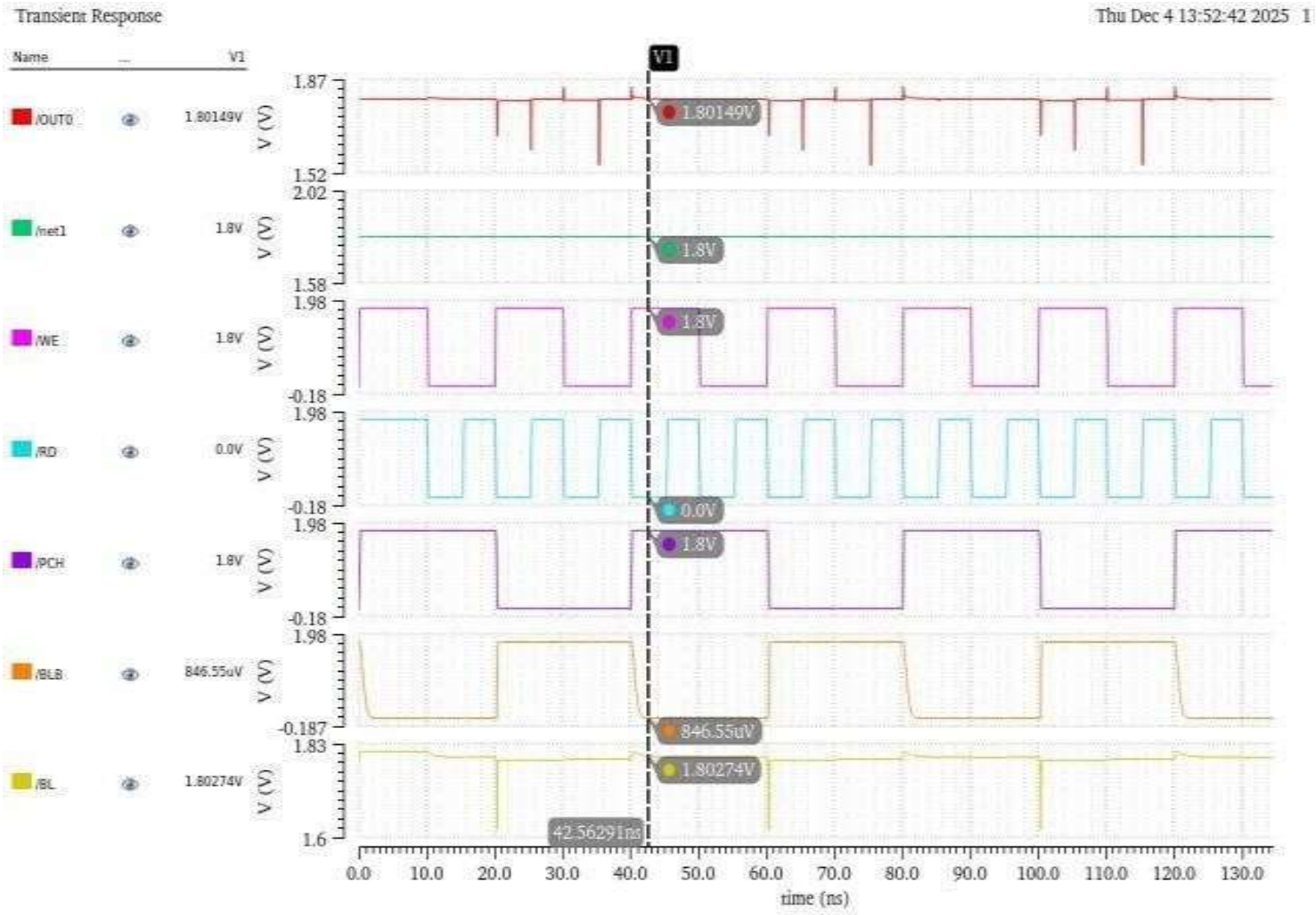


Fig 8: Output waveform of 4*4 memory.

. CONCLUSION

This research paper show cases the pattern of SRAM cell in 45nm technology that have reduced and also area very low power consumption. The low power SRAM cell of 6t design is examined. The DC analysis is carried during simulation process and the power consumption is evaluated. Also, the simulation is done by Cadence Virtuoso tool. The simulation is done using 45nm technology for 6T SRAM cell. The design shows the advancement of speed and also shrinking of technology also area is decreased. Power dissipation decreases on scaling of technology. Simulation and result verification has been done in terms of area and power dissipation. Both DRC and LVS checks has been satisfied with zero errors and low area consumption. Overall usage of GPDK 45nm technology enables optimized sizing of transistor and reduced leakage power, making SRAM cell appropriate in modern VLSI technology. The design methodology and verification approach presented in this work provide foundation for future enhancements, including array level implementation and further power optimization techniques for advanced semiconductor memory designs. Layout simulations were performed to evaluate the impact of parasitic effects, confirming that the designed SRAM cell maintains reliable performance under technology scaling. Performance parameters such as power consumption, delay and noise margins were evaluated, demonstrating improved efficiency and stability compared to conventional design. The results indicate that the proposed SRAM design is suitable for low power and high density memory applications. The SRAM architecture was designed at the transistor level and implemented using cadence virtuoso, ensuring accurate representation of device behavior in deep submicron technology.

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DECLARATIONS

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the institution for providing access to Cadence Virtuoso tools and the GPDK 45 nm technology design kit for research purposes.

Data Availability: The data is collected on studying various reseach paper and designed the schematics based on considering factors by ourselves.

Authors' Contribution: Author 1(Akshata kitturkar): Developed the initial concept for the SRAM project.

Designed the transistor-level schematic of the 6T SRAM cell using Cadence Virtuoso. Drafted the first version of the manuscript, including introduction, abstract, and technical descriptions.

Author 2 (Arifa Donsal): Performed pre-layout simulations for read, write, and hold operations.

Verified MOSFET behavior, ensuring that the SRAM cell operates correctly.Collected and analyzed simulation data, such as voltage waveforms, delay, and stability metrics.

Author 3 (Aishwarya Daddi): Created the physical layout of the SRAM cell in Cadence Virtuoso Layout Suite.

Performed Design Rule Check (DRC) to ensure the layout follows the GPDK 45 nm process rules.

Conducted Layout Versus Schematic (LVS) verification to confirm the layout matches the schematic design.

Author 4 (Akshata Arawal): Evaluated key performance metrics, including static noise margin (SNM), access delay, power consumption, and leakage current.Generated figures, tables, and waveform illustrations for the manuscript.Edited and refined the manuscript for clarity, grammar, and journal formatting.

Author 5 (Prof.Rajeshwari.P): Provided conceptual guidance and technical mentorship throughout the project.

Reviewed and advised on the SRAM design methodology, simulations, layout, and post-layout verification.

Suggested improvements for manuscript structure, clarity, and technical content.

***Use of AI and AI-Assisted Technologies:** AI tool named as ChatGPT used to study and understand every concept and flow of the design along with its functionality.

***Conflict of Interest:** No conflict of interest.

***Copyright Permissions:** All figures and tables included in this article are original and designed using tool named Cadence Virtuoso.

REFERENCES

[1]V.Panduranga vemula, S.Priyanka,M.Raheez,A.Sairam "Design and Analysis of 6T SRAM in 45NM Technology." International Journal of Engineering Reasearch & Technology(IJERT), Vol.11, Issue-05, May-2022. https://www.ijert.org/design-and-analysis-of-6t-sram-in-45nm-technology [1].

[2]M G Shrinivas,Bhavana M S "Performance Analysis of 6T,8T,and 10T SRAM Cell in 45nm Technology". International journal of Engineering and Advanced Technology (IJERT),volume-13,Issue-5,June 2024.https://doi.org/10.35940/ijeat.E4447.13050624 [2] .

[3]Calhoun, B. H., & Chandrakasan, A. P. (2021). "Static Noise Margin Variation for Sub threshold SRAM in 65-nm CMOS." IEEE Journal of Solid-State Circuits, 41(7),. https://doi.org/10.1109/JSSC.2006.87428 [3].
[4]Varanasi Koundinya, Jithendra Pulivarthi, madanu Karun Chand, D.Jayanth Sai Kumar "performance Evaluation of 6T SRAM cell using 90nm Technology"vol-10,Issue-09,September-2021.DOI: 10.17577/IJERTV10IS090027 [4].
[5]Usha mehta,Shubham Thaker "Design and Development of In-Memory-Compute SRAM Cell Using 45nm Technology" IEEE International Conference on Intelligent Signal Processing and Effective Communication Technologies (INSPECT), December 2024. DOI:10.1109/INSPECT63485.2024.10896129 [5].
[6]Namgiri Snehith,E Santosh Kumar,Srinivasa Rao Karumuri "Design and Analysis of 8× 8 SRAM Memory Array using 45 nm Technology at 100 MHz" IEEE Devices for Integrated Circuit (DevIC) , April 2023 DOI:10.1109/DevIC57758.2023.10135059 [6].
[7]Praveen K N, Dr.B.G Shivaleelavathi "SRAM Memory Layout Design in 180nm Technology",vol.04,issue 08. DOI:http://dx.doi.org/10.17577/IJERTV4IS080677 [7].
[8]Mrs. T. Kalpana, Challa Lakshmi Reddy, Poluboyina Naveen " A Low Voltage 6T SRAM Cell Design and Analysis Using Cadence 90nm And 45nm CMOS Technology" Published in IEEE International Conference, 23 April 2024. DOI:10.1109/ICDCS59278.2024.10560497 [8].
[9]D. Mittal and V. K. Tomar, "Performance Evaluation of 6T, 7T, 8T, and 9T SRAM cell Topologies at 90 nm Technology Node," in 2020 11th International Conference on Computing, Communication and Networking Technologies (ICCCNT), Kharagpur, India, 2020, pp. 1-4. https://doi.org/10.1109/ICCCNT49239.2020.9225554 [9].
[10] F. Moradi and J. K. Madsen, "Improved read and write margins using a novel 8T-SRAM cell," 2014 22nd International Conference on Very Large-Scale Integration (VLSI-SoC), Playa del Carmen, Mexico, 2014, pp. 1-5. https://doi.org/10.1109/VLSI-SoC.2014.7004186 [10] .
[11] R. Kumar et al., "Design and Benchmark of Iso-Stable High Density 4T SRAM cells for 64MB arrays in 65nm LSTP," in 2020 IEEE 17th India Council International Conference (INDICON), New Delhi, India, 2020, pp. 1-7. https://doi.org/10.1109/INDICON49873.2020.9342091 [11].
[12] P. S. Grace and N. M. Sivamangai, "Design of 10T SRAM cell for high SNM and low power," in 2016 3rd International Conference on Devices, Circuits and Systems (ICDCS), Coimbatore, India, 2016, pp. 281-285. https://doi.org/10.1109/ICDCSyst.2016.7570609 [12].
[13] P. S. Grace and N. M. Sivamangai, "Design of 10T SRAM cell for high SNM and low power," in 2016 3rd International Conference on Devices, Circuits and Systems (ICDCS), Coimbatore, India, 2016, pp. 281-
285. https://doi.org/10.1109/ICDCSyst.2016.7570609 [13].
[14] Mehdi Bathaee,Zed Mostoufi,Hamid Ghezelayagh,Anahita Afkham," A 2.0 GHz 4 Mb pseudo-SRAM with on-chip BIST for refresh in 0.18u CMOS technology with LVDS output data bus drivers",IEEE explore,February 2002. DOI: 10.1109/ICECS.2002.1046306 [14].
[15] Rohin Gupta,Sandeep Singh Gill " AN EFFICIENT NOVEL 6T SRAM CELL WITH OPTIMIZED LAYOUT AND DESIGN METRICS IN 45NM TECHNOLOGY", ICTACT JOURNAL ON MICROELECTRONICS, JULY 2022, VOLUME: 08, ISSUE: 02, DOI: 10.21917/ijme.2022.0233 [15].
[16] Aruru Sai Kumar, K. N. Rao, +3 authors Sai Vinay," Design and Implementation of 1KB SRAM array in 45 nm Technology for Low-Power Applications",IEEE, DOI:10.1109/ACCESS57397.2023.10200801 [16].
[17] Hamsa S,Dr.Anant A.G," Design of SRAM and DRAM Volatile Memories using 45nm Technology for FPGA Architecture" International Journal of Engineering Research & Technology (IJERT), Vol. 4 Issue 05, May-2015, https://doi.org/10.17577/IJERTV4IS051279 [17].
[18] Paramandla Akhila "Design and Performance Analysis of Low Power 6T SRAM Cell in 45nm CMOS Technology" INTERANTIONAL JOURNAL OF SCIENTIFIC RESEARCH IN

ENGINEERING AND MANAGEMENT,June 2025, DOI:10.55041/IJSREM49554 [18].

[19] Sheetal Begali,Balasetty Sravani,B Kavya, M B Varalakshmi, ”Design and Parametric Analysis of 6T SRAM Using 180nm and 45nm Technology”, International Conference on Network, Multimedia and Information Technology (NMITCON) September 2023, DOI:10.1109/NMITCON58196.2023.10275903 [19].

[20] Vaibhav Sharma,Akkala Subbarao,” Performance Enhancement of 6T SRAM : A Comparative Study of Conventional and Stacking Techniques in 45nm Technology using cadence virtuoso” IEEE International Students' Conference on Electrical, Electronics and Computer Science (SCEECS), January 2025, DOI:10.1109/SCEECS64059.2025.10941159 [20].

[21] Anil kumar Rajput,Manisha Pattanaik,Gaurav Kaushal,” An energy-efficient 10T SRAM in-memory computing macro for artificial intelligence edge processor” Memories - Materials Devices Circuits and Systems, August 2023, DOI:10.1016/j.memori.2023.100076 [21].