"Design and VLSI implementation of Delta-Sigma ADC"

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***Abstract*—In this work, a Delta-Sigma Analog to Digital Converter is designed using CMOS VLSI technology. The main aim of this design is to convert low-frequency analog signals into digital form with good accuracy and low power usage. Instead of using complex analog circuits, this converter uses oversampling and a feedback loop to improve resolution. The design mainly consists of an integrator, comparator, and a one-bit feedback circuit. Each block is designed and tested separately and then connected together to form the complete system. Simulation results show that the output bitstream correctly follows the input signal, which proves proper noise shaping and stable operation. Due to its simple structure and reliable performance, this design is suitable for low-power and low-frequency VLSI applications.**

Keywords—Delta-Sigma ADC, CMOS VLSI, Oversampling, Noise Shaping, Low Power Design, Mixed Signal Circuit.

I. INTRODUCTION

Nowadays, most electronic systems work in digital form, but real-world signals are analog in nature. Because of this, Analog to Digital Converters play a very important role in modern VLSI systems. Applications like sensor systems, medical devices, and portable electronics need converters that give good accuracy while consuming less power. Traditional ADCs need complex analog circuits and careful component matching, which makes the design difficult in CMOS technology. Delta-Sigma ADC is a better option for such applications because it uses oversampling and feedback to achieve high resolution with simple analog blocks. This work focuses on designing a Delta-Sigma ADC that is easy to implement, stable in operation, and suitable for low-frequency signal conversion.

1.1 Problem statement:

Many conventional ADC designs require complicated analog circuits, which increase power consumption and chip area in VLSI implementation. This creates difficulty when the ADC is used for low-frequency and low-power applications. Although Delta-Sigma ADCs reduce analog complexity, their performance depends on stable loop operation and proper block design. Hence, there is a need to design a simple and reliable Delta-Sigma ADC using CMOS technology that provides accurate conversion with low power usage.

II. METHODOLOGY

The design process starts by selecting a first-order Delta-Sigma architecture because it offers better stability and easy implementation. The basic working of oversampling and noise shaping is first studied at system level. After that, each block such as integrator, comparator, and one-bit DAC is designed separately using CMOS circuits. These blocks are tested individually to verify their operation. Once all blocks work properly, they are connected together to form the complete Delta-Sigma ADC. Finally, simulations are carried out using different input signals to observe output behavior and stability.

III. DESIGN AND IMPLEMENTATION

The proposed Delta-Sigma ADC uses a closed-loop structure that includes an integrator, comparator, and a one-bit DAC in the feedback path. The integrator is implemented using a two-stage operational transconductance amplifier to achieve sufficient gain and accurate signal accumulation. Stability is ensured by proper compensation techniques. The comparator converts the analog integrator output into a single-bit digital signal based on reference voltage comparison. The one-bit DAC converts this digital output back into an analog signal for feedback. The complete circuit is implemented and simulated in a VLSI design environment, and the output is obtained as a high-frequency bitstream.

3.1 Implementation of Two-Stage OTA

The two-stage OTA is designed to give enough amplification for the analog part of the system. In the first stage, the difference between the input signals is sensed and converted

into a small current. This current is then passed to the second stage, where it is changed into a stronger voltage signal. A small compensation capacitor is connected between the two stages so that the output does not become unstable. Careful selection of transistor sizes helps in reducing power usage while maintaining proper gain. This OTA works smoothly and supports accurate signal processing inside the sigma-delta loop.

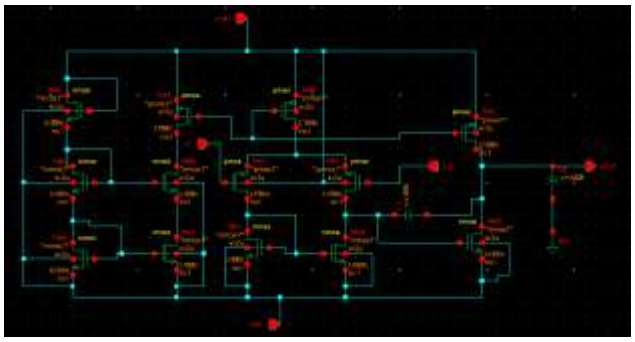

Figure 1 : Two-Stage OTA schematic

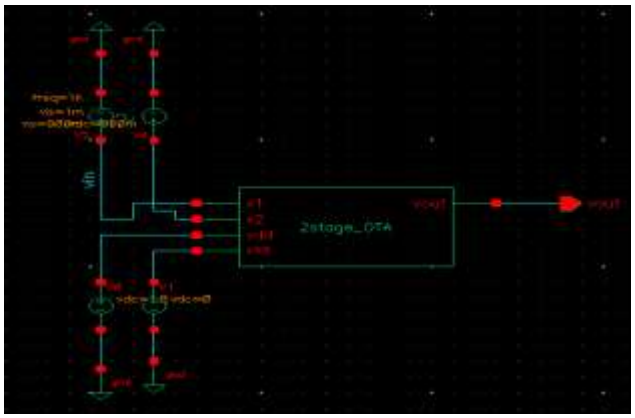

Figure 2 : Two-Stage OTA test

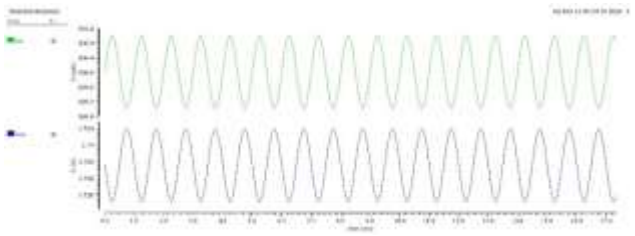

Figure 3 : Two-Stage OTA waveform

4.2 Implementation of Operational Amplifier

The operational amplifier is built using CMOS transistors so that power consumption stays low. Its main role is to amplify the difference between the input terminals and provide a clean output signal. The amplifier is designed to maintain steady performance even when the input signal changes slowly. Biasing is adjusted to keep all transistors in correct operating region. This ensures the amplifier gives a reliable output without distortion, which is important for correct integration and feedback operation.

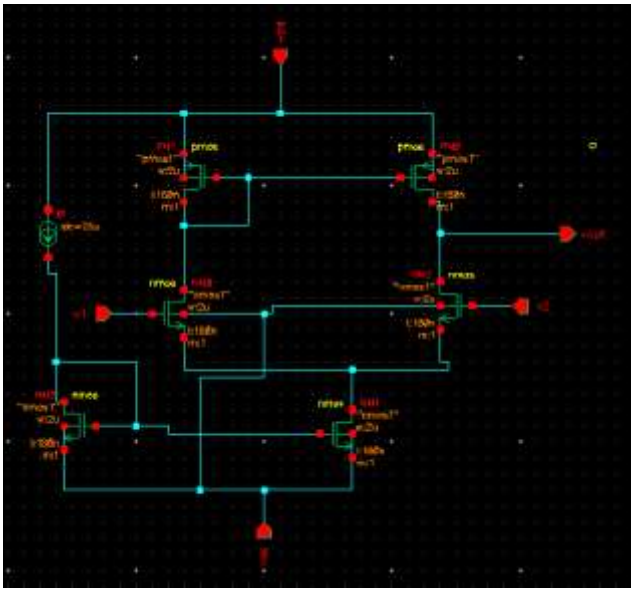

Figure 4 : Operational amplifier schematic

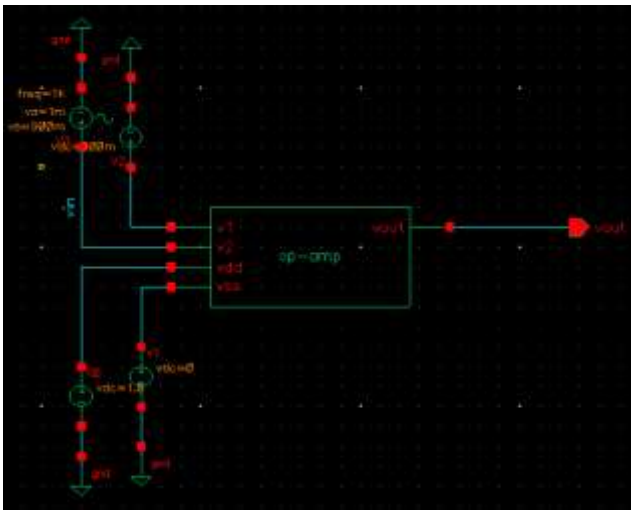

Figure 5 : Operational amplifier circuit

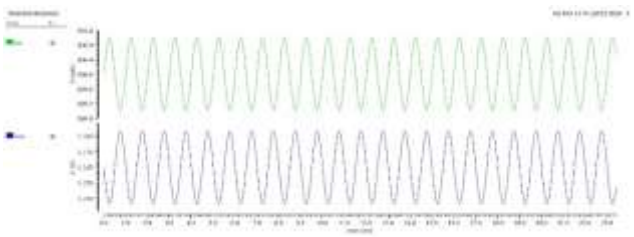

Figure 6 : Operational amplifier waveform

4.3 Comparator

The comparator acts like a decision-making block in the circuit. It checks whether the input signal is higher or lower than a fixed reference level. Based on this comparison, the output instantly switches to either high or low logic level. A simple CMOS structure is selected to avoid unnecessary circuit complexity. The comparator responds quickly and produces clear transitions without glitches. This fast and clean operation helps the sigma-delta loop work without errors.

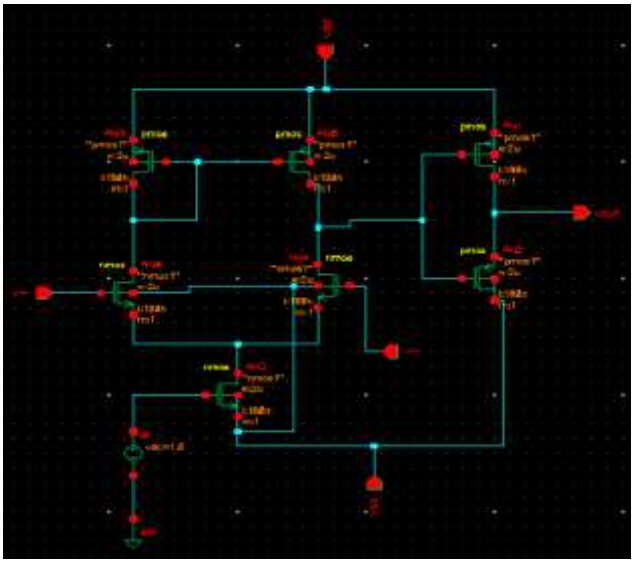

Figure 7: comparator schematic

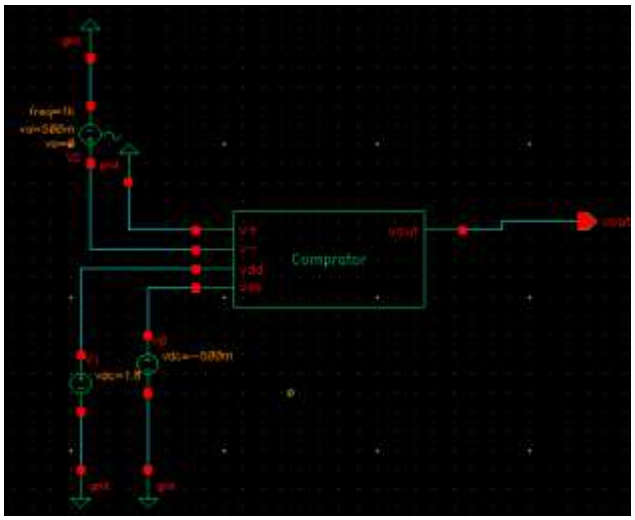

Figure 8 : comparator test circuit

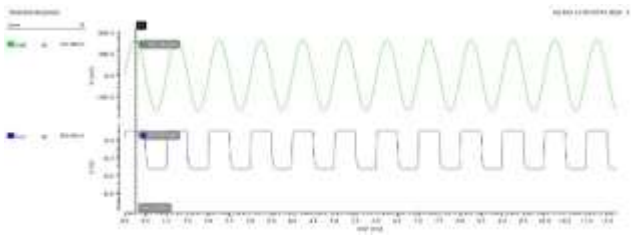

Figure 9 : comparator waveform

4.4 Digital-to-Analog Converter

The analog to digital conversion in this design is done using the sigma-delta method. Instead of producing a direct digital number, the converter generates a stream of single-bit outputs at high speed. The average value of this bitstream represents the input signal level. Oversampling helps push noise away from the useful signal band. Because of this approach, the design achieves good resolution while keeping the analog circuitry simple and easy to implement.

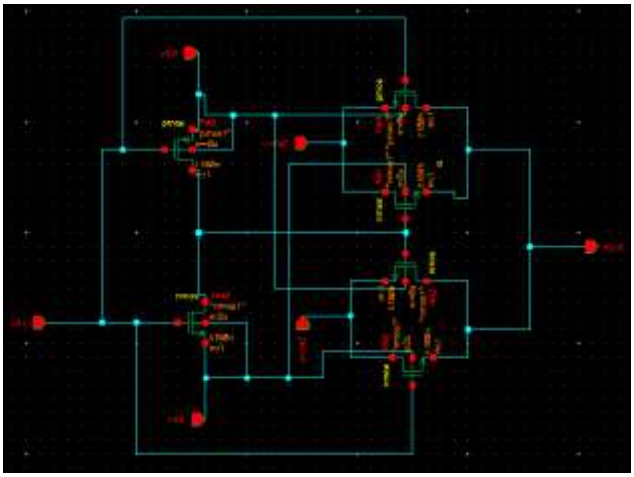

Figure 10 : 1bit -DAC schematic

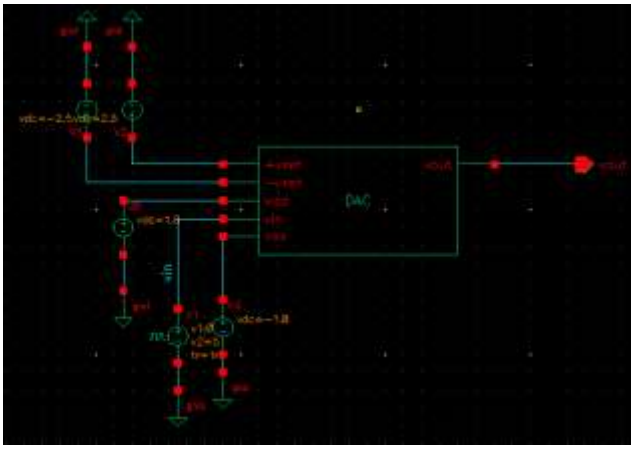

Figure 11 : 1bit- DAC test circuit

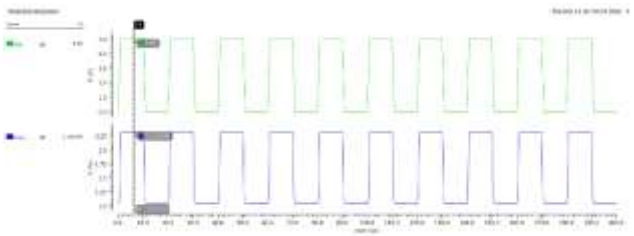

Figure 12 : DAC waveform

4.5 Integrated Delta-sigma ADC

In the final sigma-delta setup, all individual blocks are connected in a closed feedback loop. The input signal and feedback signal are continuously compared, and the difference is accumulated by the integrator. The comparator observes this accumulated value and produces a one-bit output. This output is converted back into an analog signal and fed again into the loop. The system automatically balances itself and tracks the input signal correctly. Simulation results show stable behavior and proper digital output generation, proving the effectiveness of the design.

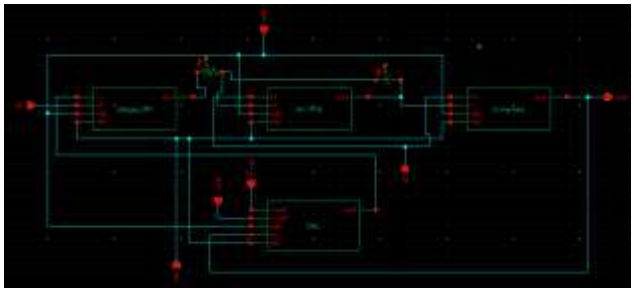

Figure 13 : Delta – sigma schematic

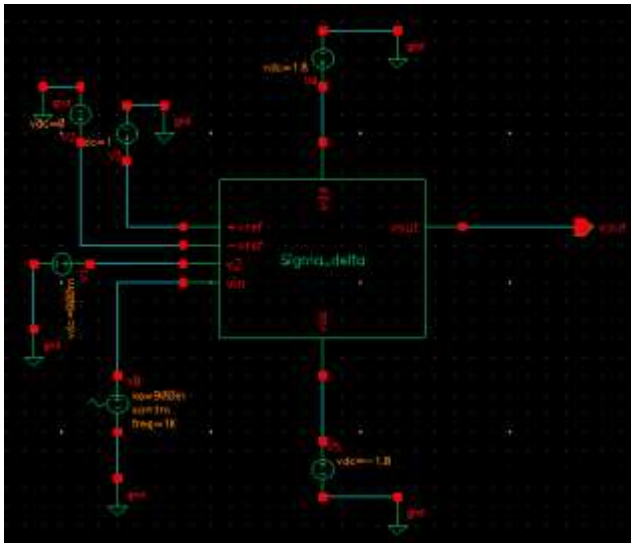

Figure 14 : Delta – sigma test circuit

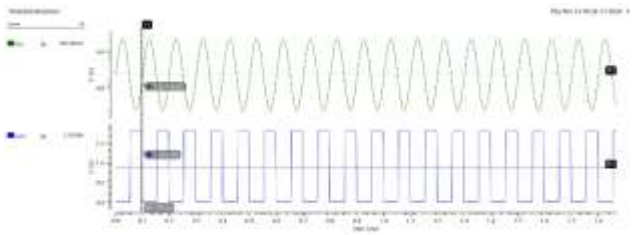

Figure 15 : Delta sigma waveform

V. Result and Observation

- The designed Delta-Sigma ADC was successfully implemented and verified through circuit-level simulations using CMOS technology. Individual functional blocks, including the integrator, comparator, and one-bit DAC, were first simulated independently to confirm correct operation.
- The integrator output showed smooth and continuous voltage variation, indicating proper accumulation of the error signal.
- The comparator produced a clean single-bit output with correct switching behavior in response to changes in the integrator output.
- After integrating all blocks, the complete Delta-Sigma modulator was simulated using a low-frequency input signal.
- The output of the modulator was observed as a high-frequency bitstream whose density varied according to the input signal amplitude. This confirms correct oversampling and feedback operation. Stable loop behavior was maintained throughout the simulation without oscillations or distortion.
- The results demonstrate that the implemented Delta-Sigma ADC performs as expected and is suitable for low-frequency, low-power VLSI applications.

III. CONCLUSION

In this project, a Delta-Sigma Analog to Digital Converter is successfully designed and implemented using CMOS VLSI technology. The design achieves accurate signal conversion by using oversampling and feedback while keeping the analog circuitry simple. All functional blocks are verified through simulation and show stable operation. The output results confirm proper noise shaping and correct bitstream generation. Because of its low complexity and reliable performance, this design is suitable for low-power and low-frequency applications. In future work, higher-order modulators and digital filters can be added to improve overall performance

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