

Design of a Ternary Segmented MUX-Based Approximate Adder for Low-power Applications

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Abstract - Digital systems today need fast arithmetic units which consume minimal power for their image processing and multimedia and artificial intelligence tasks. The full carry propagation method which traditional adders use leads to increased waiting time and power consumption problems. Approximate computing has emerged as an effective technique to improve energy efficiency in error-tolerant applications where small computational errors are acceptable.

The project presents a ternary segmented MUX based approximate adder which implements dynamic accuracy control. The adder design requires two regions which include an approximate LSB section and an accurate MSB section. The design achieves lower power consumption and critical path delay reduction through its method of approximating lower significant bits while maintaining higher bit accuracy.

The system achieves multiple operating modes which allow users to adjust between power consumption and processing speed and output quality. The results from simulation and implementation show all existing designs operate at lower power levels and higher speeds while producing better Power-Delay Product (PDP) results.

Key Words: Approximate Adder, Ternary Logic, MUX-Based Design, Low Power, Dynamic Accuracy Control.

1.INTRODUCTION

Arithmetic circuits function as the foundational elements of contemporary digital systems which find their applications in processors and digital signal processing units and multimedia processing systems. The commonest circuit component in these systems functions as an adder which engineers use to create advanced arithmetic systems that include multipliers and accumulators and arithmetic logic units. The rising power

requirements which drive modern technology development together with customer needs for improved performance have turned into vital design issues that engineers must address when creating arithmetic circuits.

Recent years have demonstrated that image processing and video processing and machine learning and multimedia systems maintain a high level of capacity to handle calculation errors. The systems require numerical precision only to a certain extent because tiny computational errors do not impact their final results. The field of approximate computing has emerged as a design approach which allows engineers to decrease computational precision for better performance in power consumption and speed and hardware system complexity.

The design of approximate computing systems depends on their use of approximate adders. The power usage and delay times of approximate adders decrease when designers implement simplified logic or restrict their carry propagation abilities in comparison to standard adders. The design of approximate adders presents designers with a major challenge to achieve a suitable balance between accuracy and performance which needs to work for applications that use different precision levels during their operational time.

Exact adders achieve complete accuracy through their design but this causes them to use more power and sustain longer critical path delays which become worse when their bit-width increases. Existing approximate adders provide significant benefits in power usage and delay times yet most of these systems operate with fixed accuracy which restricts their performance to specific application or operating conditions. Modern systems increasingly require adaptive precision, which enables

users to adjust system accuracy according to their application needs and system power limits and their current workload conditions. The image preprocessing stages enable higher approximation errors, while the final output stages require complete precision. The need for multiple accuracy levels drives the creation of reconfigurable approximate adders, which deliver different accuracy modes through one architectural design.

The effective solution of Partitioned-Bit Approximate Adders (PBA) partitions the adder into multiple bit-level sections, which enables users to control approximation, while maintaining accuracy, in their most important digital components. The industry standard design evaluation tools need to verify the practical performance of these designs. Xilinx Vivado serves as an FPGA design and synthesis platform, which enables users to accurately assess power consumption and delay times and area requirements for digital designs.

The design of the N-bit adder system uses multiple partitions which depend on the significance of their individual bits. The least significant bit (LSB) partitions use approximate logic methods for their implementation because this approach decreases both system complexity and operating time. The most significant bit (MSB) partitions use precise methods which help maintain system performance within defined error limits. The design includes a reconfiguration mechanism which permits users to activate or deactivate approximation features for specific adder segments whenever they need to switch between different accuracy settings. The design system allows users to enhance system accuracy at their convenience because it maintains power efficiency throughout the process. The complete design process uses Hardware Description Language (HDL) to create a model which Xilinx Vivado uses for synthesis operation. This process enables researchers to assess hardware performance through measurement of usage and system delays and energy expenditures.

2. LITERATURE SURVEY

The increasing need for energy-efficient yet powerful computing systems has led to research efforts which focus on developing new device technologies and multi-valued logic systems and approximate arithmetic circuits. Ternary logic systems and approximate adders have emerged as major research areas because they enable power reduction and simpler circuit designs and faster processing in systems which need to handle errors during

image processing and multimedia operations. This reviews of research studies which investigate short-channel device performance together with CNTFET-based ternary logic circuits and approximate ternary adders and accuracy-configurable arithmetic architectures which serve as the basis for this study.

Chaudhry and Kumar [1] presented a comprehensive review of short-channel effects in deep-submicron SOI MOSFETs and their impact on device reliability. Their research showed that circuit performance and power usage in electronic devices are impacted by three specific factors which include leakage current, threshold voltage variation, and diminished gate control. The research demonstrated that arithmetic circuits require new device technologies to achieve performance enhancements.

Zhang et al. [2] conducted a study to evaluate how ballistic carbon nanotube FinFETs operate at the circuit level. The analysis showed that CNT-based devices outperformed traditional CMOS technologies through better switching speed and lower power consumption. The research established CNTFETs as viable options for building power-saving arithmetic and logic circuits which would benefit from upcoming computing technologies.

Deng and Wong [9], [10] invented SPICE models which create compact representations of CNTFETs that exact match their core channel operations and all nonideal characteristics. The models showed accurate simulation results and performance results for circuits which used CNTFET technology. Their work established a foundation which researchers used to verify the operation of ternary and approximate arithmetic circuits which use CNTFET technology.

Lin et al. [15] investigated how to create ternary logic gates and arithmetic circuits through the use of CNTFET technology. The researchers proved that CNTFETs let users create efficient multi-valued logic systems through their ability to control threshold voltage. The authors showed that their ternary adders and arithmetic blocks consumed less power and used fewer transistors to prove that ternary logic works for arithmetic calculations.

Murotiya and Gupta [4] created a new ternary full adder design which uses CNTFETs as its building blocks. Their architecture aimed to achieve two objectives which required them to use fewer transistors while they worked to save energy and perform ternary functions correctly.

Simulation results confirmed the system used less power than CMOS-based ternary adders.

Malik et al. [7] introduced both exact and approximate CNTFET-based ternary full adders which they used to conduct their comparison study. The research showed that exact designs lose energy efficiency compared to approximate designs which proves that approximation plays a vital role in ternary arithmetic circuits.

The examined previous studies about advanced device technologies and ternary logic foundations and CNTFET-based ternary adders and approximate arithmetic designs and accuracy-configurable adders. The existing adder designs have achieved better energy efficiency and performance but developers still need to create flexible reconfigurable partitioned approximate adder designs.

3. PROPOSED METHODOLOGY

3.1 Proposed N-trit approximate adder using a segmentation technique.

The complete adder chain system contains two primary operational areas which divide its functions into two distinct components.

1. The Most Significant Segment (MSB Segment) contains two Full Adders (FA) and one Half Adder (HA) which together perform computations with complete accuracy while maintaining the correct output results. The segment enables carry propagation because it prevents major numerical inaccuracies from affecting its results.

2. The Least Significant Segment (Approximate Segment) contains multiple Half Adder Simplified (HAS) blocks which operate without stage carry propagation while using controlled approximation to decrease both delay and power consumption.

The red dashed line in Figure 1 clearly separates the accurate MSB segment from the approximate LSB segment.

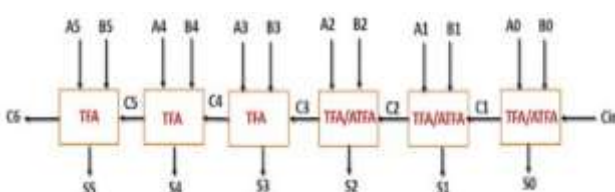


Fig -1: Proposed N-trit approximate adder using a segmentation technique

3.2 Concept of Partitioned-bit approximate adder

The proposed method divides an N-bit adder into multiple bit segments which activate according to their importance for processing. λ The Most Significant Bit (MSB) Partitioning method uses precise calculations to maintain numerical accuracy and prevent significant errors in the output. λ The Intermediate Partition provides two operational modes which users can select through their chosen setup. λ The Least Significant Bit (LSB) Partition uses basic approximate logic because errors from these bits do not significantly affect the total output quality. The PBA system enables partition-based approximation controls which allow dynamic adjustment of accuracy between different levels, which marks a major advance beyond current segmentation methods.

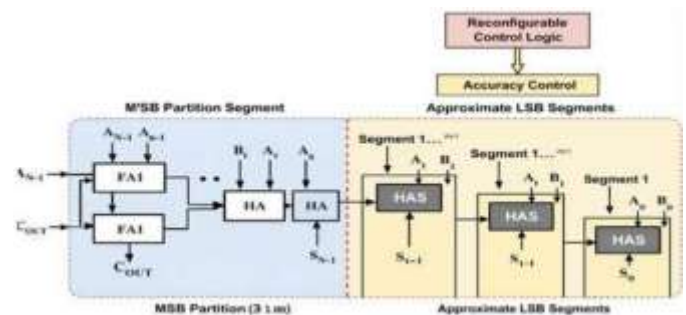


Fig -2: Proposed PBA Architecture

3.3 Ternary Segmented Mux-Based Approximate Adder

The suggested approach presents a ternary segmented MUX-based approximate adder, incorporating dynamic accuracy reconfiguration to enhance power efficiency and minimize critical path delay. This architecture partitions the adder into two distinct areas: an approximate least significant bit (LSB) region and an accurate most significant bit (MSB) region. Within the LSB section, MUX-based ternary logic, specifically 3:1 multiplexers, is utilized to produce approximate sum outputs with a controlled error margin, thus mitigating both switching activity and hardware complexity. A dynamic boundary half-adder, which separates the two areas, manages carry propagation based on the chosen operating mode.

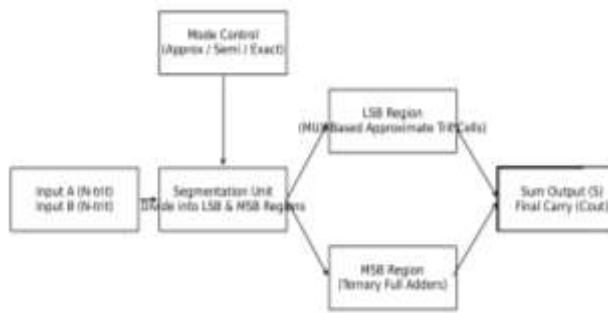


Fig -3: Proposed Method of Block Diagram

The MSB region utilizes accurate ternary full adders to preserve precision in higher significant bits and limit overall error magnitude. The design supports runtime switching between Approx, Semi, and Exact modes which enables users to create different combinations of power usage and processing speed together with precise outcomes. The proposed method achieves reduced power consumption, shorter critical path delay, and improved Power-Delay Product (PDP) through the use of MUX-based ternary structures for carry path optimization and lower bit approximation, which makes it suitable for energy efficient approximate computing applications. The architecture and implementation of the ternary mux approximate adder is shown in fig.3 and fig.4.

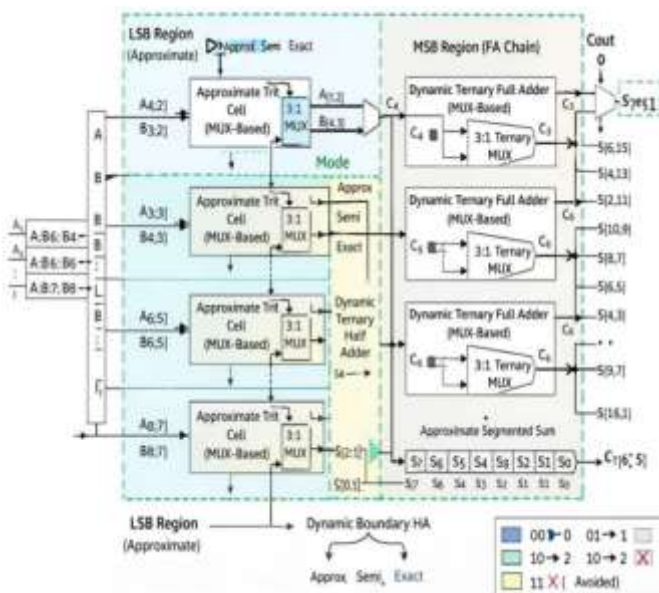


Fig -4: Architecture of the proposed method

The Ternary segmented MUX-based approximate adder develops to reduce power consumption while it enhances processing speed and maintains constant computational performance. The method executes through four steps

which include segmentation and ternary encoding and MUX-based computation and dynamic accuracy control.

3.4 Ternary Representation

The equations 1 and 2 and 3 show that ternary logic defines three different values for each trit digit.

$$T \in \{0, 1, 2\} \dots \dots \dots (1)$$

The ternary addition of two trits A and B with input carry Cin

is defined as:

$$\text{Sum} = (A + B + C_{in}) \dots \dots \dots (2)$$

$$C_{out} = \lfloor A + B + C_{in} \rfloor_3 \dots \dots \dots (3)$$

The calculation produces trit Sum which becomes the final output because Cout generates interference that affects the next trit.

3. RESULTS AND DISCUSSION

The functional operation of the suggested segmented ternary MUX-based approximate multiplier was proved through behavioral simulation testing. The system tested operational accuracy by applying random 16-bit input vectors and comparing the approximate output results with the exact multiplication results.

At the observed simulation instant:

a) Input operands:

$$A = 9186$$

$$B = 9650$$

b) Exact multiplication result:

$$9186 \times 9650 = 88644900$$

c) Approximate multiplier output:

$$\text{Approximate Output} = 0x0001005$$

The simulation framework executed statistical error metric computations throughout its testing process which included multiple test vectors. The first testing session which included 100 test cases produced these results:

Table -1: Expected Results

Parameter	Observed Value
Total test vectors	100
Erroneous outputs	99
Correct outputs	1
Accuracy	1%
Maximum error	15375
Total accumulated error	639780
Relative error metric	59.82

The results obtained from this study demonstrate that the proposed system achieves successful implementation of approximate multiplication through its design which achieves substantial reductions in calculation accuracy. The system displays high error rates because its present method of dividing operations and creating approximations works to decrease hardware demands but results in loss of calculation accuracy.



Fig -3: Simulation Result

The proposed design is evaluated against the existing architecture in five technical areas which include power, delay, frequency, area, and temperature measurements. The results show that power consumption decreased from 10.125 W to 8.56 W which resulted in a 15.45% energy efficiency improvement. The propagation delay decreased from 8.607 ns to 8.146 ns which indicates that computations now occur at a quicker pace. The system throughput improves because maximum operating frequency rises from 116 MHz to 122.7 MHz when delay times decrease. The number of cells shows a minor decrease from 75 to 74 which demonstrates better area optimization results. The thermal performance shows improvement because temperature decreased from 44.1°C to 41.1°C. The optimized logic design together with the decreased switching activity results in these improvements. The proposed architecture delivers superior speed performance while using less power and achieving greater hardware efficiency than the existing design.

Table -1: Comparison table

Metric	Existing	Proposed	Overall Improvement
Power	10.125 W	8.56 W	15.45% Lower
Delay	8.607 ns	8.146 ns	Faster
Frequency	116 MHz	122.7 MHz	Higher
Cells	75	74	Optimized
Temperature	44.1°C	41.1°C	Cooler

3. CONCLUSIONS

The study developed an approximate adder which uses a ternary segmented MUX structure to enable dynamic accuracy changes between two different operational modes, which results in better power consumption and faster processing speeds for applications that tolerate errors. The proposed architecture divides the adder into an approximate LSB region and an accurate MSB region, separated by a dynamic ternary boundary half-adder. The design achieves reduced switching activity and critical path delay through lower significant bit approximation together with 3:1 MUX-based ternary logic, which maintains higher-order accuracy. The results from the Xilinx Vivado implementation show a 15.45% decrease in total on-chip power consumption, dropping from 10.125 W to 8.56 W. Additionally, the critical path delay is reduced by 5.35%, from 8.607 ns to 8.146 ns. The system operates at its maximum frequency of 122.7 MHz while maintaining a junction temperature of 41.1°C which demonstrates better thermal efficiency. The research can progress through multiple paths for future work. The proposed architecture can be realized through CNTFET technology which provides improved energy performance at nanoscale dimensions.

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BIOGRAPHIES



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They have made academic contributions through their research work and technical publications which appeared in esteemed journals and conferences. The students developed their technical and research abilities through his mentorship which focused on hardware and system-level design.