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DESIGN OF AN FIR FILTER USING RIPPLE CARRY ADDERS AND VEDIC MULTIPLIERS

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Abstract—FIR (Finite Impulse Response) filters play an essential role in the field of Digital Signal Processing (DSP) to eliminate noise suppression in Electro Cardio Graph (ECG), imaging devices and the signal stored in analog media. In this fashion the filter calculation is accomplished to reduce the noise level. The Filter passes only the desired frequency to pass thereby reducing distortion in the processed signal during measurement. In this project, an FIR filter is proposed, which is designed, considering two main parameters, total time (path) delay and area used by the filter. Ripple carry Adder has been introduced to reduce the area occupancy of the circuit. A Vedic multiplier and D-type register have also been introduced in the proposed FIR filter to perform multiplication within less steps by preserving linear – phase characteristics.

Keywords- FIR filter, Digital Signal Processor, Vedic Multiplier

I. SYNOPSIS

To implement this filter, Ripple carry Adder has been introduced to reduce the area occupancy of the circuit. A Vedic multiplier and D-type register have also been introduced in the proposed FIR filter to perform multiplication within less steps by preserving linear – phase characteristics.

8-bit 5 tap direct form of FIR filter has been designed for computational data comparison. The inconsiderable amount of lag elements of FIR further reduces energy usage and area. Therefore, by the proposed circuits, the overall performance and area occupancy of FIR filter can be improved significantly. To design the circuits, Xilinx ISE Design Suite software is preferred to be used.

II. INTRODUCTION

In signal processing, a filter is a device that removes some unwanted components or features from a signal. Filtering is a device or process that removes unwanted part partially or completely from the signal.

Filters are predominantly used in electronics and telecommunication, radio, television, audio recording, radar, control systems, music synthesis, image processing, and computer graphics. Digital filters can be implemented in two ways, by convolution (also called finite impulse response or FIR) and by recursion (also called infinite impulse response or IIR). Filters carried out by convolution can have far better performance than filters using recursion.

In digital signal processing (DSP) systems such as fast Fourier transforms, discrete cosine transforms (DCT's), and error correcting codes, Finite impulse response (FIR) filters have great importance because of their linear- phase characteristics and feed forward implementations.

FIR FILTER:

In signal processing, a finite impulse response (FIR) filter is a filter whose impulse response (or response to any finite length input) is of finite duration, because it settles to zero in finite time. This is in contrast to infinite impulse response (IIR) filters, which may have internal feedback and may continue to respond indefinitely (usually decaying).

The FIR filter contains the delay element which is implemented using d flip-flop, multiplier is implemented using Vedic multiplier and in the place of adders, ripple carry adders are implemented.

III. EXISTING METHODOLOGIES

FIR filter can be enforced by using three digital hardware elements, a delay element (D- register), a multiplier and an adder. Therefore, the area and delay parameters depend on the type of multiplier and adder used. Multiplication involves two introductory operations: the generation of the partial products and their accumulation. Thus, there are two possible ways to enhance the multiplication is

is to reduce the number of partial products or accelerate their accumulation. Existing systems make use of the following multipliers for designing FIR filters.

Array Multiplier: Array multiplier is much suitable modest architecture due to its less design, time complexity and performs fast multiplication in pipelined manner. It is a digital combinational circuit to perform multiplication of two n-bit numbers based on ADD and SHIFT algorithm.

For n x n array multiplier, it requires n*n AND gates, n*(n-2) Full Adders (FA) and n Half Adders (HA). The main disadvantage of the array multiplier is the worst-case delay of the multiplier proportional to the width of the multiplier. The speed will be slow for a very wide multiplier.

Booth Multiplier: Booth Multiplier implements Booth Algorithm, named after by its originator, A. D. Booth. This algorithm is implemented for signed multiplication of integers and can be extended to real numbers too. Algorithm is based on recording the multiplier to a recorded value leaving the multiplicand unchanged.

Booth Multiplier performs fewer additions than a serial multiplier. Two main drawbacks of Booth Algorithm are the inefficiency of the circuit when isolated 1's are encountered and difficulty in designing parallel multipliers as number of shift-and-add operations vary. The circuit of Booth multiplier is more complex to generate a partial product bit in Booth encoding.

IV. PROPOSED SYSTEM

The proposed system of an FIR filter makes use of

- Vedic Multiplier which uses Urdhva-Tiryagbhyam Sutra for fast multiplication.
- Ripple carry adder which is an area efficient adder.
- D-type register is used to provide necessary delays.

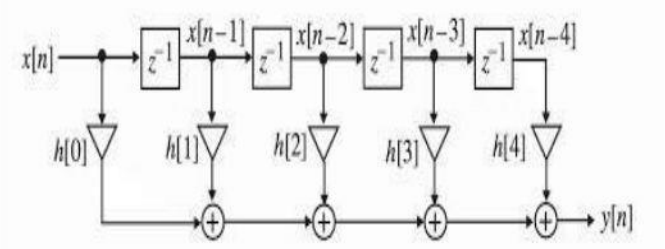

Fig 1: *Five tap direct form FIR filter.*

The above block diagram represents a five tap direct form FIR filter which is fed with an input signal x[n]. The filter coefficients are represented as h[0], h[1], h[2], h[3], h[4] which can be calculated according to the characteristics of the desired digital filter. The blocks "z^{-1}" indicate the delay element or D- type register to introduce specific delays so as to preserve the phase relationship of the input signal. The input signal is then multiplied with the appropriate filter coefficients (convolution) and the result at each stage is summed and provided as output.

The output y of a linear time invariant system is determined by convolving its input signal x with its impulse response b_k. For a discrete-time FIR filter, the output is a weighted sum of the current and a finite number of previous values of the input. The operation is described by the following equation, which defines the output sequence y[n] in terms of its input sequence x[n]:

$$Y(n) = \sum_{K=0}^{N} b_K x(n-k)$$

Where
Y(n) = Output
signal x(n) = Input
signal b_k = Filter coefficients also known as tap weights, that make up the impulse response.
N = Order of the filter terms on the right-hand side.
The x[n-k] - In these terms are commonly referred to as taps, based on the structure of a tapped delay line that in many implementations or block diagrams provides the delayed inputs to the multiplication operations.

V. LITERATURE SURVEY

1. Mittal Anubhuti , Ashutosh Nandi, and Disha Yadav. "Comparative study of 16-order FIR filter design using different multiplication techniques." IET Circuits, Devices & Systems 11.3 (2017): 196-200.]

This literature describes about FIR filters, represents designing and implementation of a low power and high speed 16 order FIR filter. To optimize filter area, delay and power, different multiplication techniques such as Vedic multiplier, add and shift method and Wallace tree (WT) multiplier are used for the multiplication of filter coefficient with filter input. Various adders such as ripple carry adder, Kogge Stone adder, Brent Kung adder, Ladner Fischer adder and Han Carlson adder are analysed for optimum performance study for further use in various multiplication techniques

along with barrel shifter. Secondly optimization of filter area and delay is done by using add and shift method for multiplication, although it increases power dissipation of the filter.

2. M. Hasan, M. J. Hossein, M. Hossain, H. U. Zaman and S. Islam, "Design of a Scalable Low-Power 1-Bit Hybrid Full Adder for Fast Computation," in *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol.67, no.8, pp.1464 - 1468, August 2020.

This literature describes about, a novel design of a hybrid Full Adder (FA) using Pass Transistors (PTs), Transmission Gates (TGs) and Conventional Complementary Metal Oxide Semiconductor (CCMOS) logic is presented. Performance analysis of the circuit has been conducted using Cadence toolset. Only the proposed FA and five of the existing designs have the ability to operate without utilizing buffer in intermediate stages while extended to 64 bits. Based on the simulation results, it can be stated that the proposed hybrid FA circuit is an attractive alternative in the data path design of modern high-speed Central Processing Units.

VI. BLOCK DIAGRAM

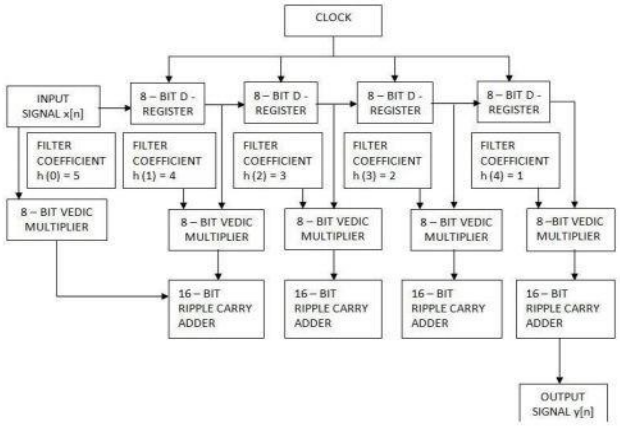

Fig 2: *Block Diagram of Proposed FIR filter*

VII. RESULTS

In signal processing, a finite impulse response (FIR) filter is a filter whose impulse response (or response to any finite length input) is of finite duration, because it settles to zero in finite time. Here, the 8 – bit input signal x[7:0] is convoluted with the digital filter designed i.e., the 8 – bit input is multiplied with appropriate 8 – bit filter coefficients in one or many stages and the output is obtained as the result of summation of all the outputs at respective stages.

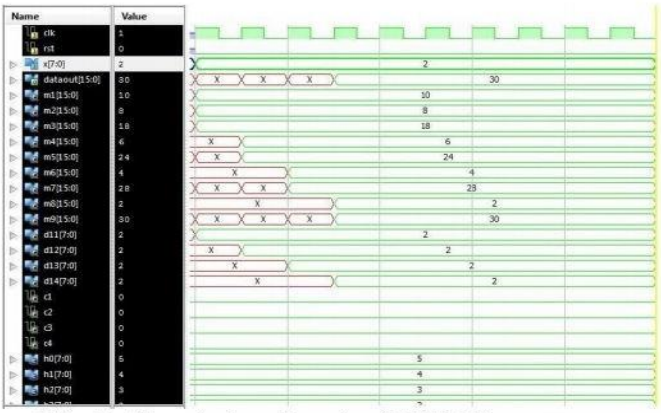

Fig 3: *Simulation Result of FIR Filter*

The timing summary and device utilization summary of FIR filter are shown below

Timing Summary:

Speed Grade: -2
Minimum period:
1.753ns
(Maximum Frequency: 570.451MHz)
Minimum input arrival time before clock: 3.306ns
Maximum output time after clock: 16.020ns
Maximum combinational path delay: 18.102ns

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	32	54576	0%
Number of Slice LUTs	108	27288	0%
Number of fully used LUTFF pairs	17	123	13%
Number of bonded IOBs	26	218	11%
Number of BUFG/BUFGCTRLs	1	16	6%

Fig 4: *Device Utilization Summary of FIR filter*

VIII. CONCLUSION

This project presents an FIR filter which uses Vedic multipliers and Ripple Carry adders. Vedic multipliers, effectively reduce the number of partial produ cts to compute the product of two numbers, in this case convolution of input signal, x[n] and output signal, y[n], thereby reducing the delay or time required to perform multiplication operation. Ripple carry adders are area efficient adders when compared with other adders such as carry select adders, carry save adders, etc.

The proposed FIR filter performs the complete process with a total delay of 18.102ns. By observing the device utilization summary, the utilization of bonded IOBs is 11% and utilization of BUFG/BUFGCTRLs (general clock buffer (BUFG), with 2:1 multiplexer for two clock inputs (BUFGCTRL)) is 6%. Hence, area required by the FIR filter is less.

IX. REFERENCES

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