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Design of an Innovative Eleven-Level Quadruple Boost Inverter for Electric Vehicles

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ABSTRACT

To meet the precise voltage and current demands of electric vehicles (EVs), lithium-ion cells are commonly arranged in series and parallel configurations. To ensure the safe operation of these cells, voltage and charge equalization techniques are employed. However, these equalization circuits can introduce energy losses into the system, and in the event of cell failure, the battery pack may disconnect as a protective measure. As an alternative approach to satisfying voltage requirements, **switched-capacitor (SC) inverters** have gained traction due to their ability to boost voltage without using bulky transformers or inductors.

This paper presents a novel **eleven-level quadruple boost (ELQB) multilevel inverter** specifically tailored for EV applications. The proposed inverter architecture enhances operational efficiency through an **inherent self-voltage balancing capability**, eliminating the need for external sensor circuits or complex balancing control mechanisms. The charge/discharge sequence of the capacitors naturally ensures proper voltage levels at the output, maintaining balanced capacitor voltages throughout operation.

The eleven-level output waveform enables a quadruple voltage gain compared to the input source, delivering high-quality power suitable for driving electric vehicle motors. Additionally, a comprehensive analysis is provided, comparing component requirements such as capacitors, gate drivers, and power switches. System-level performance metrics including **voltage gain, blocking voltage, and total standing voltage (TSV)** are evaluated to demonstrate the advantages of the proposed ELQB inverter over recently developed multilevel topologies.

I. OVERVIEW

Due to their higher output quality and expanded power handling capabilities, multilevel inverters (MLIs) are becoming more and more popular, which is in line with the global trend toward greater use of renewable energy sources. Improved output quality, less voltage stress, less electromagnetic interference, and the requirement for a tiny filter are only a few benefits of MLIs. Because of these qualities, MLIs are a sensible option for a range of applications. Among the various MLI types, researchers have focused on switched-capacitor MLIs (SC-MLIs) because of their ability to increase voltage. SC-MLIs are used in a variety of industries, including fuel cells, solar cells, and electric cars. A reduced semiconductor SC-MLI was proposed in a study by [1], in which several power switches were swapped out for discrete diodes, lowering the total number of semiconductors. However, because it uses symmetric DC sources, this SC-MLI has a limited voltage gain and requires extra capacitors to reach high voltage levels. A multi source SC MLI architecture that does not require an H-bridge inverter was proposed by the authors in [2]. However, as the number of levels increases, this design's efficiency decreases and prices rise due to the many DC sources, capacitors, and semiconductors used. In their study from [3], Lee and Lee presented a seven-level configuration with two capacitors that evenly divide the source and a single input DC supply. The voltage enhancement ratio is 0.5, suggesting that greater input DC sources are required to produce higher-level expansions even though the semiconductor peak voltage strain is twice the input voltage.

TABLE 1. Component comparison of the proposed NLQB with newly recommended MLIs.

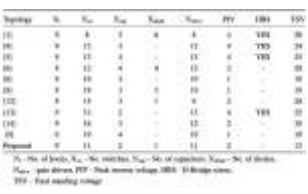

TABLE 2. Cost comparison of the proposed NLQB inverter with newly evolved SC based MLIs.

Component	Series	Rating	Unit price ($)	Topology							
				[13]	[1]	[5]	[14]	[8]	[9]	[6]	P
MOSFET	IRFZ30PBF	50 V	1.63	-	-	-	-	-	-	-	-
	IRFP140NPBF	100 V	1.89	8	4	8	14	19	19	4	7
	IRFP240PBF	200 V	2.31	1	-	-	2	-	-	8	4
	IRFP350PBF	400 V	6.13	4	4	4	-	-	-	-	-
Gate driver	IR2110SPBF	-	1.92	12	8	13	12	19	19	12	11
Diode	SDT10A100P5	100 V	0.61	-	6	-	-	-	3	4	1
Capacitor	B41231A9128M	3.3 mF	1.51	3	3	3	3	3	3	4	2
Total price ($)				69.5	55.6	71.0	58.6	76.9	78.7	87.5	47.22

A switched-capacitor inverter for high frequency applications is described using the topology suggested in [4], which is based on a cascaded MLI. An H-bridge cell makes up each of the fundamental switching capacitor units in this configuration. To extend the inverter to higher levels, input DC supplies must be included. In order to reduce the number of components needed, the authors in [1] developed a SC-based MLI with segregated DC supply. However, because of the H-bridge at the load end, the blocking voltage of the converter rises and the voltage boosting of each capacitor is restricted to one. With smaller components, an asymmetric inverter proposed in [5] provides more levels. However, the TSV stays high and the boosting factor is restricted to one per capacitor, just like in [1]. To achieve notable voltage boosting increases, the inventors of [6] and [7] developed asymmetric inverters using binary boosting factors. However, the creation of higher TSV rises as a result of higher voltage levels requiring additional capacitors. Single-stage inverters were created in an attempt to get around the drawbacks of the previously listed topologies. through [8, 9], [10], and [11]. These topologies remove the requirement for an H-bridge in order to create polarity. For these inverters, the DC voltage is equal to the peak inverse voltage (PIV). One voltage gain per capacitor is attained by references [8] and [9], whereas 0.5 voltage gains per capacitor are attained by references [10] and [11]. However, high-power switches and capacitors are needed to further develop these converters. Target high-voltage gain was suggested by topologies in [12], [13], [14], and [9], where each capacitor's voltage gain increases in binary. Nevertheless, these topologies suffer from problems with blocking voltage and a large part count. The modules suggested by [15] and [16] split the DC-link into equal halves using capacitors to provide nine levels. Thus, additional isolated capacitors are needed to achieve higher-level extensions. Furthermore, semiconductors have a reverse blocking voltage that is twice the supply voltage. A voltage gain of one per capacitor is attained by Sandeep et al. [8] and Taghvaie et al. [9], but Lee [10] and Bhat Nagar et al. [11] attain a voltage gain of 0.5 per capacitor. However, additional development of these converters is required. high-power capacitors and switches. Conversely, high voltage boosting topologies, in which each capacitor's voltage gain rises in a binary fashion, were put out by Wang et al. [12], Kovvali et al. [13], Siddique et al. [14], and Taghvaie et al. [9]. However, the huge number of semiconductors and blocking voltage in these topologies are drawbacks. Capacitors are used in nine-level modules, which were first shown by Kumari et al. [15] and Mohamed et al. [16], to split the DC link in half. More isolated capacitors are therefore required to achieve higher-level extensions. Furthermore, semiconductors have a blocking voltage that is double the supply voltage. In [17] and [18], the authors constructed self-voltage balancing SC-based seven-level converters and suggested seven-level topologies with a 1.5 output voltage gain. Twelve switches, two diodes, and two capacitors are required for the topology in [17]. However, the design in [18] calls for three capacitors, four diodes, and eight switches. However, reaching greater heights requires a significant number of elements. A architecture that makes use of a single voltage source is provided in the paper by [19]. Nine semiconductors, three capacitors, and two diodes are required for this setup in order to provide seven output voltage levels. However, the circuit requires more components as the number of levels rises. With a primary focus on photovoltaic (PV) applications, the studies in [20], [21], and [22] suggested topologies that prioritized common ground and voltage boost features. Three capacitors and an inductor are used by the inverters that [20] and [21] introduced to produce five levels. These converters' high semiconductor count, forward voltage drop across the diode, and magnetic size present difficulties despite their benefits. However, the circuit suggested by [22] uses an inductor, three capacitors, and thirteen semiconductors to produce nine levels. One capacitor is charged to provide voltage, and the other two have a boosting factor of 0.5. This topology has a large number of components even if it provides common grounding. Moreover, high power switches and capacitors are needed for further converter expansion. The circuit in [23] uses eight switches, two diodes, three caps and two inductors to provide five output levels. For the same voltage gain, inductors are larger and heavier

than capacitors. When the voltage gain is two, the inductor-based boost converter's efficiency drops to 90%, and when the voltage gain is four, it drops to 70%. Furthermore, as the boosting gain rises, the inductor begins to saturate. The circuit in [24] uses one capacitor, two diodes, and twelve switches to produce five levels. This layout necessitates additional components to generate levels and does not increase the output voltage. Topologies for combining several DC sources and capacitors are suggested in [25] and [26]. These inverters are best suited for particular applications, such renewable energy systems, and require extra voltage supplies to expand to higher levels. A nine-level inverter with twelve switches and four capacitors was suggested by the study in [27]. Despite using four capacitors, the boosting gain is only two.

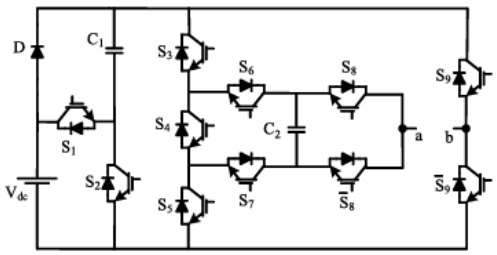

FIGURE 1. Proposed NLQB inverter topology.

Switched-capacitor inverters face difficulties like higher component counts and TSV as the voltage gain rises. These restrictions have a major effect on the converter's total cost. For the topology to be cost-effective, the blocking voltage and component count must be kept to a minimum. By addressing the aforementioned issues, the goal of this research is to develop a revolutionary voltage-boosting converter with fewer components. Tables 1 and 2 compare the components and costs of the suggested topologies with those previously discussed. in turn. Section IV offers a thorough comparison analysis of these tables. The operation principles, capacitor sizing, and modulation approaches are all thoroughly investigated. To validate the claims of the suggested Multilevel Inverter (MLI), substantial hardware verification is provided.

2. SUGGESTED TOPOLOGY

A. Illustration of Topography

This section introduces a single-phase, nine-level inverter with voltage gain capability. The suggested nine-level quadraple boost (NLQB) structure's design is shown in Figure 1. Eleven power switches, two capacitors, and a diode make up the switched-capacitor network. The voltages of ±1VDC and ±2VDC, respectively, are charged to the switching capacitors C1 and C2. Terminals a and b are linked to the load. Nine voltage levels—±4VDC, ±3VDC, ±2VDC, ±1VDC, and ±0VDC—can be supplied at the output terminals of the suggested NLQB. Figure 2 displays a graphic representation of each stage. The proposed circuit's ability to generate zero and negative levels without the need for a back-end H-bridge is another noteworthy benefit. As a result, lower voltage semiconductors can be used with the NLQB inverter.

B. STATES IN OPERATION

The switch occurrences and capacitor state at each voltage level are displayed in Table 3. The operating states of charge, discharge, idle, ON, and OFF are denoted in the table by the appropriate symbols C, D, −, 1, and 0. Figure 2 shows the modes of functioning at each voltage level.

TABLE3. Look-up table for NLQB circuit.

$V_o = V_{ab}$	Semiconductors									Charge state	
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	C_1	C_2
$4V_{dc}$	1	0	1	1	0	0	1	1	0	D	D
$3V_{dc}$	0	1	1	1	0	0	1	1	0	C	D
$2V_{dc}$	1	0	1	0	1	1	1	1	0	D	C
V_{dc}	0	1	1	0	0	1	0	1	0	C	-
0	0	0	1	0	0	1	0	1	1	-	-
0	0	0	0	0	1	0	0	0	0	-	-
$-V_{dc}$	0	1	0	0	1	0	1	0	1	C	-
$-2V_{dc}$	1	0	1	0	1	1	1	0	1	D	C
$-3V_{dc}$	0	1	0	1	1	1	0	0	1	C	D
$-4V_{dc}$	1	0	0	1	1	1	0	0	1	D	D

(1 - ON, 0 - OFF, - - No effect, C - Charging, D - Discharging)

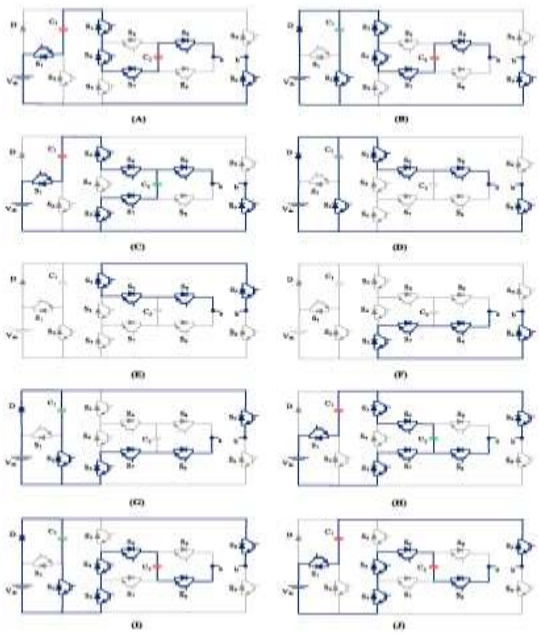

FIGURE2.ModesofoperationoftheproposedNLQBinverter:(a)4Vdc,(b)3Vdc,(c)2Vdc,(d)1Vdc,(e)0Vdc,(f)0Vdc,(g)−1Vdc,(h)−2Vdc,(i)−3Vdc,(j)−4Vdc.

Mode of 4Vdc [Fig. 2(a)]: The remaining switches are off, except switches S1, S4, S6, and ¯ S8 are on. The load receives the energy discharged by capacitors C1 and C2. The output voltage that results is therefore the sum of the capacitor and dc-link voltages (Vdc). The output voltage is shown as

$$\begin{cases} V_{C1} = V_{dc} \\ V_{C2} = 2V_{dc} \\ V_0 = V_{C1} + V_{C2} + V_{dc} = 4V_{dc} \end{cases}$$

Switches S1, S4, and ¯ S8 are ON in 3Vdc Mode [Fig. 2(b)], while the other switches are OFF. Capacitor C1 charges from the DC-link voltage via the S7 switch, while Capacitor C2 releases its energy to the load.

As a result, the output voltage is the head condition of the C2 capacitor voltage and the DC source voltage. The output voltage is shown as

$$\begin{cases} V_{C1} = V_{dc} \\ V_{C2} = 2V_{dc} \\ V_0 = V_{C2} + +V_{dc} = 3V_{dc} \end{cases}$$

S1, S3, S6, and ¯ S8 switches are ON to generate 2Vdc level in 2Vdc Mode [Fig. 2(c)]. Capacitor C1 discharges and Capacitor C2 charges via the S5 switch. The output voltage is shown as

$$\begin{cases} V_{C1} = V_{dc} \\ V_{C2} = 2V_{dc} \\ V_0 = V_{C1} + +V_{dc} = 2V_{dc} \end{cases}$$

S1, S3, S7, and ¯ S8 switches are ON in 1VdcMode [Fig.2(d)], while the other switches are OFF. In order to supply voltage, capacitor C1 is charged, and capacitor C2

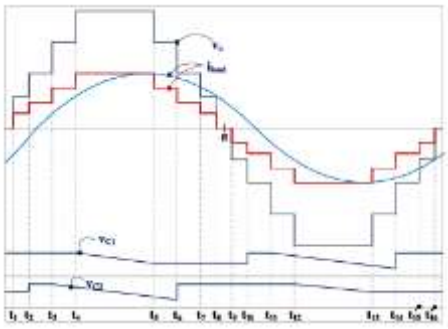

FIGURE3. Key output waveform so NLQB inverter.

stays in an idle state. The output voltage is shown as

$$\begin{cases} V_{C1} = V_{dc} \\ V_0 = V_{dc} \end{cases}$$

• [Fig. 2(e)] 0VdcMode: Switches S3, S6, S8, and S9 are all ON at this level, while the others are off. Both capacitors stay in a condition of inactivity. The output voltage is shown as

$$\begin{cases} V_{C1} = 0 \\ V_{C2} = 0 \\ V_0 = 0 \end{cases}$$

Similarly, as Fig. 2(f),(g),(h),(i),and(j) demonstrate, negative operating modes are also obtained.

C. DETECTION OF FACILITY

In SC-based MLIs, capacitance calculation is essential to ensuring that ripple stays within allowable bounds. Reduced power loss and increased converter efficiency are directly correlated with a smaller ripple in capacitor voltage [4]. Considerations include the voltage ripple, the longest discharging time, the capacitance calculation, and the current flowing through the capacitor. When there is only a resistive load, the load current and voltage are equal. Because the peak current is halfway through the integration, the maximum discharge in the capacitor occurs at the unity power factor. Consequently, there is less voltage ripple at other power factors when the capacitoratunity power factor is designed. The longest

discharge periods C1 and C2 occur between [t11, t14] and [t3-t6], respectively, as shown in Figure 3. Each C1, C2's charge equation can be calculated as follows:

$$\Delta Q_{C1} = \int_{t11}^{t14} I_{load} sin(\omega t) dt$$

(1)

$$\Delta Q_{C2} = \int_{t3}^{t6} I_{load} sin(\omega t) dt$$

(2)

where the fundamental frequency in rad/sec and the maximum current passing through the load are denoted by Iload and ω, respectively. Instants of time (t1−t8) are indicated by

$$t_1 = \frac{\sin^{-1}(\alpha_4/V_{ref})}{2\pi f_{ref}} = 3.5440 \times 10^{-4} sec$$

(3)

$$t_2 = \frac{\sin^{-1}(\alpha_3/V_{ref})}{2\pi f_{ref}} = 1.0817 \times 10^{-3} sec$$

(4)

$$t_3 = \frac{\sin^{-1}(\alpha_2/V_{ref})}{2\pi f_{ref}} = 1.8749 \times 10^{-3} sec$$

(5)

$$t_4 = \frac{\sin^{-1}(\alpha_1/V_{ref})}{2\pi f_{ref}} 2.8365 \times 10^{-3} sec$$

(6)

$$t_5 = \frac{\pi - \sin^{-1}(\alpha_1/V_{ref})}{2\pi f_{ref}} 7.1634 \times 10^{-3} sec$$

(7)

$$t_6 = \frac{\pi - \sin^{-1}(\alpha_2/V_{ref})}{2\pi f_{ref}} 8.1250 \times 10^{-3} sec$$

(8)

$$t_7 = \frac{\pi - \sin^{-1}(\alpha_3/V_{ref})}{2\pi f_{ref}} 8.9182 \times 10^{-3} sec$$

(9)

$$t_8 = \frac{\pi - \sin^{-1}(\alpha_4/V_{ref})}{2\pi f_{ref}} 9.6455 \times 10^{-3} sec$$

(10)

Therefore, the following formula can be used to calculate the minimum capacitance needed to maintain the permitted voltage ripple percentage (x%):

$$C_n = \frac{\Delta Q C_n}{x\% \times V_{Cn}}; n = 1,2,3. \quad (11)$$

$$C_1 = \frac{1}{x\% \times V_{C1}} \int_{t11}^{t14} I_0 sin(\omega t)\, dt \quad (12)$$

$$\frac{1}{0.1 \times 50} \int_{1.8749 \times 10^{-3}}^{8.125 \times 10^{-3}} 3 sin(2\pi f t) dt \quad (13)$$

$$C_1 = 3.1760 mF$$

(14)

$$C_2 = \frac{1}{x\% \times VC_2} \int_{t3}^{t6} I_0 sin(\omega t) dt$$

(15)

$$\frac{1}{0.1 \times 50} \int_{1.8749 \times 10^{-3}}^{8.125 \times 10^{-3}} 3 sin(2\pi f t) dt$$

(16)

$$C_2 = 3.1760 mF$$

(17)

D. VOLTAGE BALANCING CAPACITOR

At first, both capacitors C1 and C2 are charged to the supply voltage. These capacitors use a series-parallel approach to go through cycles of charging and discharging. The capacitors are connected in parallel to the supply during the charging phase and in series during the discharging phase. Throughout a cycle, this process is repeated several times. Because capacitors and semiconductors have low parasitic resistance, the charging path's time constant is barely impacted, enabling the capacitor voltage to rapidly reach its final value.

Nevertheless, the output resistance, which is greater than the devices' intrinsic series resistance, raises the discharge path's time constant when discharging. Even with fewer charging events, the voltage across the capacitors is kept at the optimum levels. This lowers control complexity by ensuring that the capacitors'

voltage stays constant without requiring a balance circuit.

III. THE PROPOSED NLQB CONTROLSCHEME

The constant carrier method, a well-known modulation technique, is used to assess the suggested topology. This method creates a switching pattern for the semiconductors in the NLQB by comparing a modulating sinusoidal control signal to four level-shifted carriers. The suggested switching approach for the NLQB is shown in Figure 4(a). These selectors, A0–A3, show the results of the comparison between the carrier signals and the difference, as well as the Pistecycle selector. The recommended switching technique generates the gating pattern for all power electronic switches using a logic-based methodology. The difference and carrier signals are used to express the amplitude modulation index, or ma:

$$m_a = \frac{V_m}{\left(\frac{2n-1}{2}\right)\times \bar{V}car} \quad (18)$$

When the carrier signal's peak magnitude is shown by VCar and the difference magnitude is represented by Vm. The transition angle (αn) is determined by the reference and voltage levels (Nl) as follows:

$$\alpha_n = \left(\frac{2n-1}{2}\right) \times V_{in}; n = 1,2,3\ldots,\frac{N_1-1}{2} \quad (19)$$

Vmis is the absolute value of the reference signal, and α1−α4 are the carriers' magnitudes. Equations for the switches are provided, and the resultant pulses are depicted in 4(b).

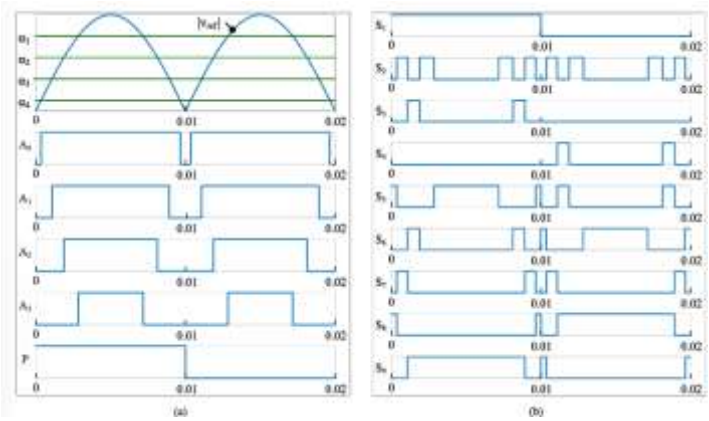

FIGURE 4. PWM switching for NLQB inverter: (a) comparator signals, (b) switching pulse sequence.

$$S_1 = A_3 + A_1.\bar{A}_2 \quad (20)$$

$$S_2 = A_0.\bar{A}_1. + A_2.\bar{A}_3 \quad (21)$$

$$S_3 = P + A_1.\bar{A}_2.\bar{P} \quad (22)$$

$$S_4 = A_2.\bar{A}_3.A_3 \quad (23)$$

$$S_5 = A_1.P + A_2.\bar{P} \quad (24)$$

$$S_6 = \bar{A}_2.P + \bar{A}_2.\bar{P} \quad (25)$$

$$S_7 = A_2.P + A_2.\bar{P} \quad (26)$$

S_8=P (27)

$$S_9 = \bar{A}_0.P + A_0.\bar{P} \quad (28)$$

TABLE 4. Attributes for NLQB topology hardware set-up.

Parameters	Specifications
DC supply	50 V
Capacitance (C_1, C_2)	3300 uF each
Output frequency	50 Hz
Load values	30 Ω - 20 mH
	60 Ω - 40 mH & 30 Ω

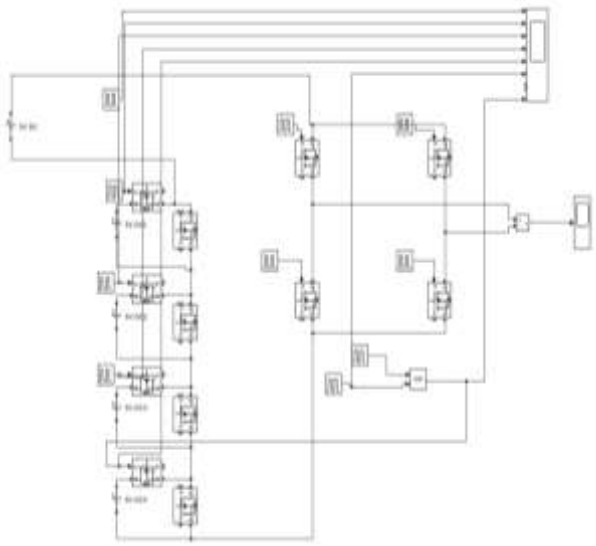

Figure 5. circuit diagram of ELQB

IV. Operational Mechanism of the ELQB Inverter for EV Applications

The working principle of the proposed Eleven-Level Quadruple Boost (ELQB) Inverter is centered around generating a high-quality multilevel AC output voltage from a low-voltage DC input, making it ideal for electric vehicle (EV) applications. Unlike conventional inverters that rely on bulky inductors or transformers for voltage boosting, the ELQB inverter uses a switched-capacitor structure that can boost the input voltage by a factor of four through a strategically controlled charging and discharging mechanism. The inverter incorporates a set of flying capacitors and a carefully arranged combination of active switches to produce eleven distinct voltage levels at the output. These levels range from −4Vin to +4Vin, including intermediate steps, allowing for finer voltage resolution and a significant reduction in total harmonic distortion (THD).

The switching operation is sequenced so that the capacitors charge and discharge in such a way that each contributes incrementally to the total output voltage, depending on the desired level. For instance, to achieve a 5Vin output, the input voltage is combined in series with four charged capacitors. The output polarity is managed using an H-bridge structure, enabling both positive and negative output levels without requiring bidirectional power flow. A unique feature of the ELQB inverter is its inherent self-voltage balancing ability. This eliminates the need for additional sensor circuits or complex control algorithms to monitor and balance the voltage across each capacitor. The symmetric and repetitive nature of the switching cycles ensures that each capacitor naturally maintains its voltage level, enhancing system reliability and efficiency.

Overall, the ELQB inverter not only simplifies the power conversion architecture but also improves system compactness, reduces the component count, and enhances efficiency—making it an excellent candidate for EV systems. The eleven-level output offers smoother waveforms, better motor compatibility, and reduced filter requirements, further reinforcing its suitability for modern high-performance electric drives.

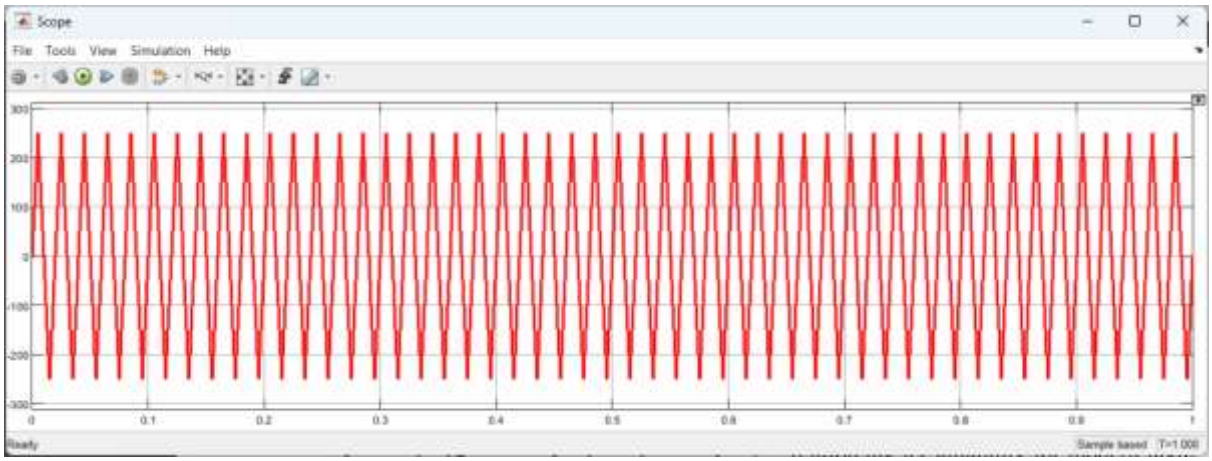

Figure 6. voltage waveform of ELQB

V. FINAL RESULTS

To generate an **eleven-level output voltage waveform**

and reduce the size of the required output filter, this article introduces a **single-phase quadruple boost inverter** tailored for electric vehicle (EV) applications. The proposed inverter is capable of achieving a significant **voltage boost up to four times** the source voltage, making it suitable for generating a **250V output** from a much lower input. One of the standout features of this topology is its **inherent capacitor self-voltage balancing** capability, which eliminates the need for additional sensing or control circuits. The detailed circuit configuration and operating principles of the **Eleven-Level Quadruple Boost (ELQB) Inverter** are thoroughly discussed in this work. A comprehensive cost and component comparison analysis is also performed, highlighting the superiority of the proposed architecture over conventional multilevel inverter (MLI) designs. Furthermore, experimental validations under various load conditions demonstrate the practical effectiveness of the topology. The results affirm the inverter's **high voltage gain, efficiency, and reduced total harmonic distortion (THD)**, making it an ideal choice for compact and efficient EV power interfaces, especially in scenarios with **limited supply voltage but high output demand**.

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