International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 08 Issue: 08 | Aug - 2024 SJIF Rating: 8.448 ISSN: 2582-3930

Design of Energy Efficient Arithmetic VLSI Circuits

P. Sumalatha[1], Dr. T. Ragavandra Vishnu[2]

[1]M. Tech student, Department of ECE, Priyadarshini Institute of Technology and Science for Women, Guntur

[2]Associate Professor, Department of ECE, Priyadarshini Institute of Technology and Science for Women, Guntur

Abstract: Advanced electronics have become an integral part of human lives, from Smartphones in our pockets to the modern vehicles on the road and to the satellites that orbit the earth. Power consumption has become a major constraint in these applications, often employing data- intensive digital signal processing systems and architectures. While enormous transistor density at the nanoscale has been increased in the Very Large-Scale Integration (VLSI) multicore era comparable to Moore's law, improving the performance of computing systems has become extremely difficult. Sustaining technological advancements for such energy-constrained devices has paved the way for new areas in research.

"Approximate Computing (AC)" has become one of the most promising paradigms, a field that has gained significant attention in the quest for energy efficiency in recent years. AC algorithms are numerically approximate rather than accurate. Inherent error resilience is the primary source of motivation behind AC. Recent research demonstrates that error resilience is pervasive in cyber search, deep learning, multimedia, recognition and data mining. Arithmetic units are the fundamental building blocks in most of the data dominated applications at the micro- architectural level of abstraction. AC is optimal for power and area efficient arithmetic circuits.

1. Introduction

The nanoscale miniaturization of modern electronics has resulted in numerous consumer devices spanning a broad spectrum of applications. High performance digital signal processors with embedded integrated circuits are in great demand for portable mobile devices. The steadfast expansion of big data processing, Internet of Things (IoT) and machine learning in addition to Multimedia necessitates a huge amount of data and massive computations at lower power budgets. Energy efficient arithmetic circuits are imperative requirement, that form the fundamental of digital systems.

Figure 1.1 shows two tasks that deal with division between 500 and 21. When asked whether the result of division between 500 and 21 is greater than 10, the human brain would right away respond "Yes," Task division is done but not to the fullest accuracy. However, if the question is whether the result is greater than 23.8, we would likely take a little longer and work even harder. However, system hardware and software typically do computations with consistent accuracy levels every time.

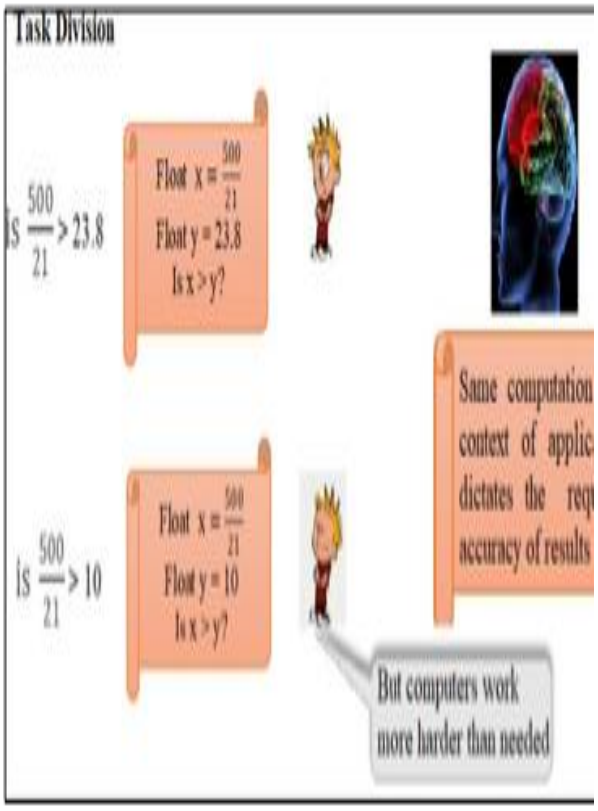


Fig 1.1Task division

In a larger sense, edge devices coupled with battery power driven fog nodes desire minimal power. This demand emerges as we are swiftly approaching an era dominated by a sophisticated networked society built on the efficiency across several error-resilient IoT and cyber-physical systems with cloud factors, various technological requirements infrastructure as its foundation. Facilitating and emphasis on green computing**.** efficient communication between these devices becomes paramount to reduce network latency and energy usage while ensuring that remote processing is more feasible.

2. APPROXIMATE COMPUTING(AC)

Digital Signal Processing (DSP) blocks form the core of various multimedia applications in which the ultimate result is either an image or video targeting people's needs. However, humans have limited perceptual abilities when interpreting a picture or video. Inheriting the advantage, it is possible for the outputs of the existing digital logic circuits to be approximate with a trivial trade-off in accuracy. This field of research is generally known as approximate or error-tolerant computing. AC depends on the ability of computational systems to accept some inaccuracies being executed using approximate designs.

AC primarily depends on inherent error resiliency. Inherent error resilience or tolerance is the property of an application to generate acceptable outputs instead of being accurate, even though some aspects of its underlying computations are approximate or imprecise. Recent research demonstrates that a wide range of applications (≈ 83%) are inherently error-tolerant. AC is well-suited for error-tolerant multimedia applications.

3. NECESSITY FOR APPROXIMATE COMPUTING

The following subsections concisely

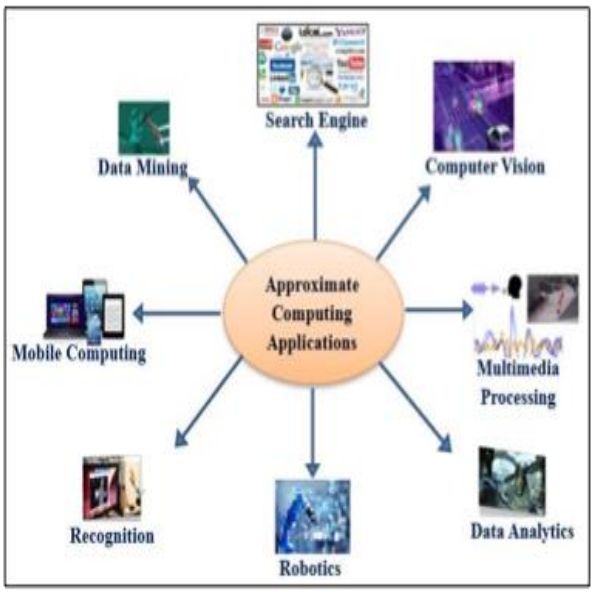


Fig 2. Approximate computing in multimedia application

Noisy and redundant input data: Many DSP systems receive noisy inputs from the outside world. Applications with resilience to noisy inputs also have tolerance to approximations in computations.

- Absence of a Unique Golden Output: In some scenarios, such as those involving web search engines direct answers are not possible, but multiple valid responses are acceptable. A noteworthy example of error resilience is frequently cited as the vast family of Recognition, Mining and Synthesis (RMS) applications. Slightly modifying the outputs of internal operations may not degrade the endresults.
- Limited Human Perception: Due to limitations in human perception, these errors are difficult to distinguish in applications like image, audio and video processing. The majority of the applications that belong to this category are found in the domains of multimedia and telecommunication
- Self-healing: In certain applications involving iterative refinement, errors due to approximations in one iteration can potentially get healed/recovered subsequently. Certain computational patterns favor the mitigation or the rejection of errors.

Fig 3.Various sources of inherent resilience

- Statistical / Probabilistic computation: In this approach, algorithms and techniques are designed to handle uncertainty and variability in data. These applications employ statistical computations that attenuate or cancel errors. This method helps in enhancing the reliability andaccuracy of computations.

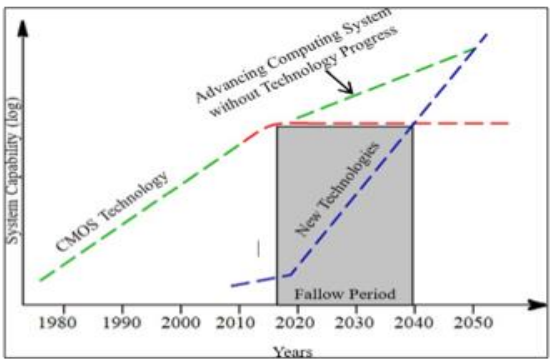


Fig 4. Harvest new gains in the "Fallow Period"

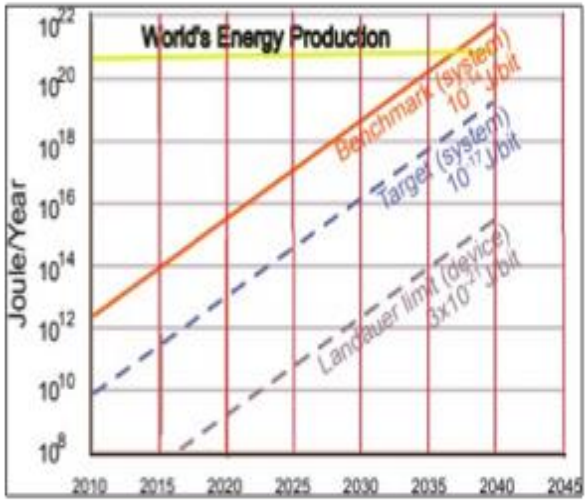


Fig 5. Progress in Energy consumption vs. the Global energyproduction

Approximate computing intentionally introduces trivial errors by emphasizing efficient enhancements in power, delay and circuit complexity across wide range of applications. Data processing has significant challenges in producing the perfect output. For a 'good enough' output that can be acceptable by the end user, accuracy can be condensed at various abstraction levels in the processing circuits.

The effectiveness of AC techniques in the embedded Support Vector Machine, Tensorial kernel circuit in tactile sensing systems is demonstrated by implementing approximate multipliers in the Singular Value Decomposition. AC using an end-to-end Trainable neural Network (AXNet) is suggested in combining dual NNs such as an approximator and a predictor into a comprehensive end-to- end trainable Neural Network (NN) to ensure the approximation quality by using the multi-task learning concept.

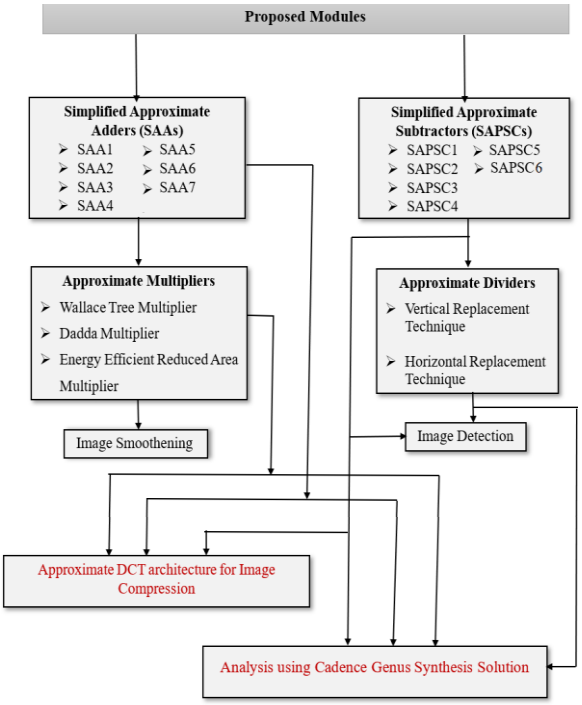


Fig 6. Overview of the proposed modules

4. Existing Approximate Adder Designs

Adders have become a performance bottleneck in the Arithmetic Logic Unit of DSP and general-purpose processors. Conventional designmethodologies aimed at improving the performance of an adder frequently result in more circuit area and power consumption.

Approximations have become essential in adders and are implemented at various abstraction levels. Approximate adders compromise accuracy for an overall efficiency enhancement. Numerous approximate adder designs have been developed by reducing worst-case carry-chains, critical paths and hardware complexity. These approximate adder types include speculative adders, segmentation-based adders, Carry Select Adders

and Approximate Full Adders that are explained in the followingsubsections.

Table 3.1 Truth table of existing approximate FAs

$^{a}\times$ -Represents the inaccurate output

Inputs					InXAA1		InXAA2		InXAA3	
A	B	C	S	Cout	S	Cout	S	Cout	S	Cout
0	0	0	0	0	0	0	0	0	1×	0
0	0	1	1	0	1	1×	1	0	1	0
0	1	0	1	0	1	0	1	0	1	0
0	1	1	0	1	0	1	1×	1	0	1
1	0	0	1	0	1	0		0		0
1	0	1	0	1	0	1		1		1
1	1	0	0	1	0	0×		1		1

Table 3.2. conventional Full Adder.

					SAFA1E		SAFA2E		SAFA3E		SAFA4E	
A	B	C	S	Cout	S	Cout	S	Cout	S	Cout	S	Cout
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	0	1	0	1	0	1	0
0	1	1	0	1	0	1	1×	0×	1×	0×	1×	0×
1	0	0	1	0	1	0	0×	1×	0×	1×	0×	1×
1	0	1	0	1	0	1	0	1	0	1	1×	1
1	1	0	0	1	0	1	0	1	0	1	1×	1
1	1	1	1	1	0×	1	1	1	0×	1	1	1

5. PROPOSED SIMPLIFIED APPROXIMATE ADDERS(SAAs)

Based on the logic complexity reduction seven SAAs have been proposed by simplifying the K-Map of the Exact FA and HA designs. Circuits developed using this method have predictable errors, the designer can fix the number of logic gates based on the accuracy requirements set for a specific application.

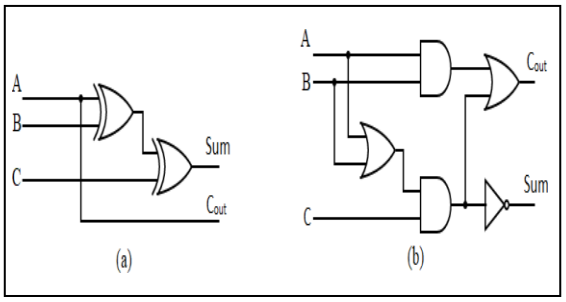


Fig 7. Proposed structure

SAAs are developed with novel logical expressions interpreted from its truth table to generate the Sum (S) and the Carry (Cout) to yield efficient area- delay optimization. In the proposed SAAs, (SAA1-SAA6) represents the approximate FA designs and SAA7 corresponds to an approximate HA design. The inputs of the following proposed SAAs are denoted by A, B and C, while the outputs are denoted by Sum and Cout. SAA3, SAA5 and SAA6 are designed to have errors in both the Sum and Cout.

while SAA1, SAA2 and SAA4 are designed to have errors either in Sum or output Cout.

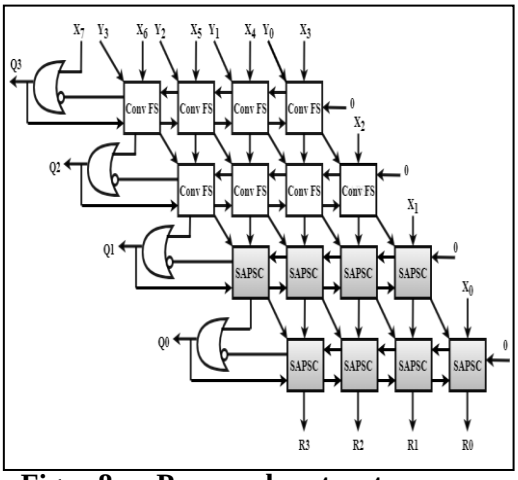
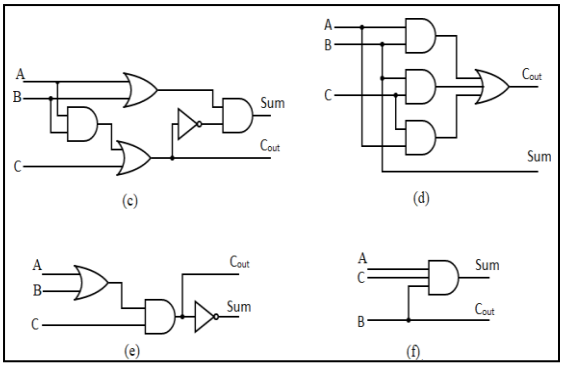


Fig 8. Proposed structure implement

$Sum = (A + B)\mathbf{C}\text{out}'$

$C\text{out} = AB + C$

Gate level architecture of (c) SAA3 (d)



SAA4 (e) SAA5 (f) SAA6

CONCULSION

Considering the extreme For extensive performance evaluation, both the proposed and existing designs are coded in Verilog Hardware Description Language (VHDL) and executed using Cadence Genus Synthesis Solution at 45 nm technology node. Various design metrics such as power, delay and area are considered for analysis. Considering approximate dividers, the proposed ARDXTRs and ARDXHRs exhibit improved performance than the existing designs. ARDXHR2 exclusively achieves a significant reduction in the PDP and in comparison, with the exact design it achieves about 43.98% savings in power.

References:

1. Atul Kumar Maurya and Ganesh Kumar, " Adiabatic Logic: Energy Efficient Technique for VLSI Applications ", International Conference on Computer& Communication Technology (ICCCT) - 2011.
2. Vojin G. Oklobd"zija, Dragan Maksimovi` c, "Pass - Transistor Adiabatic Logic Using Single Power - Clock Supply ", IEEE Transactions on Circuits a nd Systems, Vol. 44, No. 10, October1997.
3. A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low power CMOS digital design,'' IEEE J. Solid - State Circ. , vol. 27, no. 4, pp.473 - 484, Apr. 1992
4. T. Indermauer and M. Horowitz, "Evaluation of Charge Recovery Circuits and Adiabatic Switching for Low Power Design," Technical Digest IEEE Sym. Low Power Electroni cs, SanDiego, pp. 102 - 103, Oct. 2002 .
5. Arsalan, M. Shams, M., "Charge - recovery power clock generators for adiabatic logic circuits", 18th International Conference on VLSI Design, pp. 171 - 174, 3 - 7 January 2005.
6. Dragan Maksimovic et al, "Clocked CMOS adiabatic Logic with Integrated Single Phase Power Clock Supply", IEEE Transactions on VLSI Systems, vol 8, No 4, pp 460 - 463, August 2000.
7. W.C. Athas, L. Svensson, J.G. Koller et ,N.Tzartzanis and E.Y.Chou: "Low - power Digital Systems Bared on Adi abatic - switching Principles". IEEE Transactions on VLSI Systems. Vol. 2, No. 4, pp. 398 - 407 December. 1994.

8. Satyam Mandavilli, Prashanth Paramahans " An Efficient Adiabatic Circuit Design Approach for" International Journal of Recent Trends in Engine ering, Vol 2, No. 1, November 2009 Low Power Applications .
9. A. Vetuli, S. Di Pascoli, and L.M. Reyneri, "Positive feedback inadiabatic logic," Electron.Lett.,vol.32, pp.1867 - 1869, Sept. 1996 .
10. N. Anuar, Y. Takahashi, T. Sekine, "Two phase clocked adiabatic static CMOS logic," proc. IEEE SOCC 2009, pp. 83 - 86, Oct. 2009.
11. N. Anuar, Y. Takahashi, T. Sekine, "Two - Phase clocked adiabatic static CMOS logic and its logic family" Journal of semiconductor technology and science, vol 10, no. 1, Mar. 20 10.