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Design of Energy-Efficient Barrel Shifter and Vedic Multiplier Using Kogge-Stone Adder

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Abstract

This paper presents a detailed design of an energy-efficient barrel shifter and Vedic multiplier integrated with a Kogge-Stone Adder (KSA). The proposed system achieves high-speed computation using parallel prefix structures while reducing power consumption. The design is implemented using Verilog HDL and validated through simulation. The results demonstrate improved delay and efficiency compared to conventional architectures.

Keywords : Vedic multiplier,KSA, Barrel shifter

1. Introduction

In modern digital systems, arithmetic units significantly influence system performance. Multipliers and shifters are widely used in processors, DSP systems, and embedded devices. However, traditional designs suffer from high delay and power consumption.

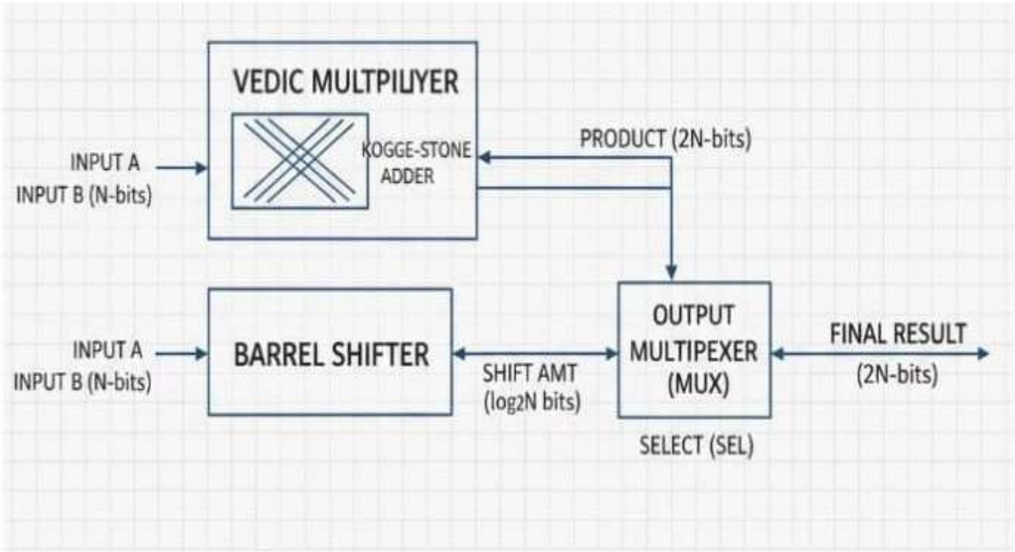
To address these challenges, this paper introduces a combined architecture using Vedic multiplication, barrel shifting, and Kogge-Stone addition. The proposed system focuses on achieving low latency, reduced switching activity, and efficient hardware utilization.

2. Literature Survey

Previous research highlights the effectiveness of parallel prefix adders and Vedic multiplication techniques. Barrel shifters implemented using multiplexers achieve logarithmic delay, while Vedic multipliers enable parallel partial product generation.

Studies indicate that integrating parallel prefix adders such as Brent-Kung and Kogge-Stone significantly improves performance. However, combining these techniques for energy-efficient design remains an area of research.

3. System Level schematic

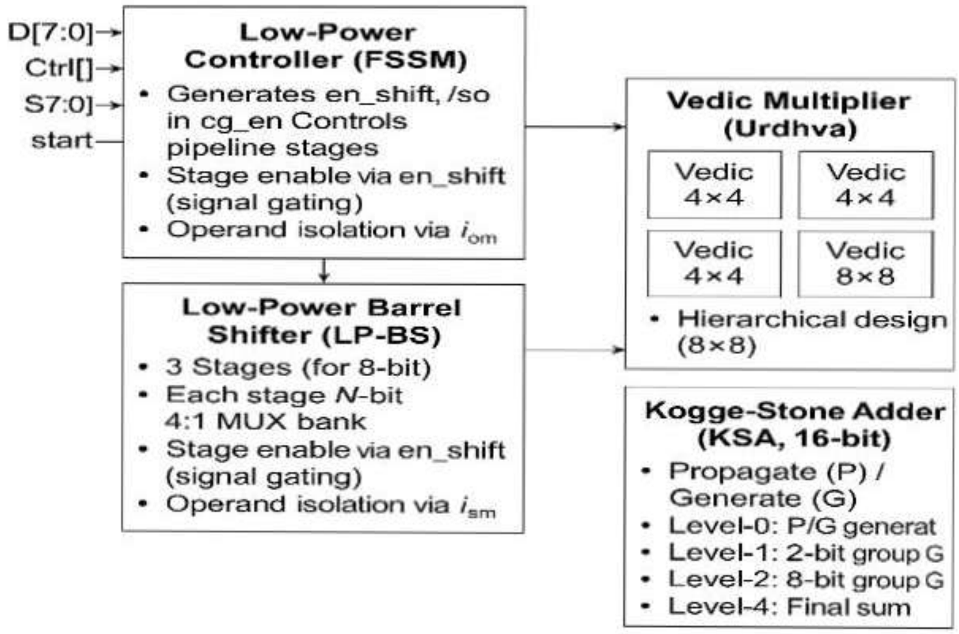


4. Proposed Methodology

The proposed architecture consists of a low-power controller, barrel shifter, Vedic multiplier, and Kogge-Stone Adder. The system is designed using Verilog HDL and simulated using EDA tools.

Key techniques include clock gating, operand isolation, and parallel computation to reduce power consumption and improve speed.

FIG:PROPOSED METHOD



Block Description:

- Barrel Shifter: Performs shift operations in a single cycle.
- Vedic Multiplier: Uses Urdhva-Tiryagbhyam algorithm for fast multiplication.
- Kogge-Stone Adder: Provides fast carry propagation using prefix tree structure.

5. Parameter Analysis

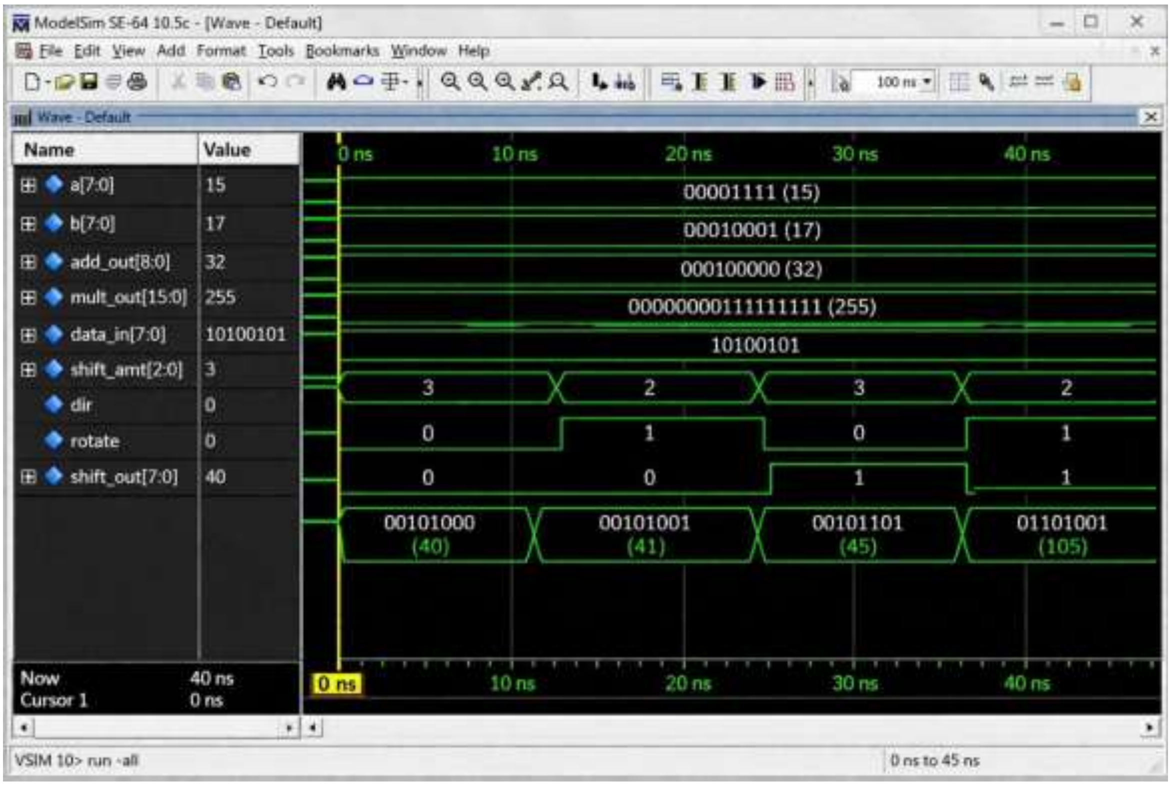
Parameter	Barrel Shifter	Vedic Multiplier + KSA
Delay	O(log n)	O(log n)
Power	Low	Moderate
Speed	High	Very High
Area	Moderate	Moderate-High

The proposed system achieves a balance between speed, power, and area. The logarithmic delay of the KSA significantly improves overall performance.

6. Results and Discussion

Simulation results confirm correct functionality of the system. The Vedic multiplier produces accurate outputs with reduced delay, while the barrel shifter performs efficient single-cycle shifting.

FIG: RESULT



The simulation demonstrates a multi-functional arithmetic and logic unit (ALU) processing fixed inputs and dynamic control signals. The output process is divided into two main categories:

1. Static Arithmetic Outputs

The system performs continuous calculations on two 8-bit inputs, a (15) and b (17). These outputs remain stable throughout the simulation:

Addition (add_out): Computes the 9-bit sum (32).

Multiplication (mult_out): Computes the 16-bit product (255).

2. Dynamic Shifting Logic

The primary output, shift_out, is updated in real-time based on the 8-bit data_in signal and three control parameters:

shift_amt [2:0]: Determines the number of bits to be shifted or rotated (ranges between 2 and 3 in this trace).

dir: Specifies the direction of the operation (set to 0 for Right operations).

rotate: Toggles between a standard Logical/Arithmetic Shift (when 0) and a Rotate operation (when 1).

1. 0–10ns: Performs a Shift Right by 3, resulting in 40.
2. 10–20ns: Switches to a Rotate Right by 2, resulting in 41.
3. 20–30ns: Reverts to a Shift Right by 3, resulting in 45.
4. 30–45ns: Switches to a Rotate Right by 2, resulting in 105.

7. Advantages

- High-speed performance due to parallel processing
- Reduced power consumption
- Scalable architecture
- Efficient hardware utilization

8. Applications

The proposed design is suitable for DSP system

image processing,

embedded processors and

cryptographic applications.

9. Future Scope

Future work includes FPGA implementation,

ASIC design optimization,

and extending the architecture to higher bit-width systems.

10.Conclusion

This paper presents a high-performance and energy-efficient arithmetic system using a barrel shifter, Vedic multiplier, and Kogge-Stone Adder. The results demonstrate improved delay and power efficiency, making the design suitable for modern digital applications.

The design and implementation of an energy-efficient barrel shifter and Vedic multiplier integrated with a Kogge-Stone Adder (KSA) demonstrate significant improvements in high-speed and low-power digital arithmetic systems. The use of the Vedic multiplication technique (Urdhva Tiryakbhyam) enables parallel partial product generation, reducing computational delay compared to conventional multipliers.

11.References

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