International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 09 Issue: 12 | Dec - 2025 SJIF Rating: 8.586 ISSN: 2582-3930

Design of Low-Power VLSI Circuits for Wearable Devices

Aniket Sonawane, Suresh Araj[2], Shahajahan Shaikh[2], Pooja More[2]

Vice Principal & HoD, Department of Electronics and Telecommunication, ARMIET, Thane
Lecturer, Department of Electronics and Telecommunication, ARMIET, Thane

Abstract

Wearable electronic devices require ultra-low-power integrated circuits capable of continuous physiological monitoring while operating from limited battery resources. Designing such systems demands aggressive optimization of both dynamic and static power across circuit, architecture, and algorithmic layers. This paper presents a comprehensive analysis of low-power VLSI design techniques tailored for wearable platforms, including voltage/frequency scaling, clock gating, power gating, multi-threshold CMOS, event-driven architectures, and approximate computing. A structured framework for optimizing power at near-threshold operating conditions is provided, along with architectural strategies that integrate dedicated biosignal-processing accelerators. Experimental results and comparative metrics from state-of-the-art wearable processors illustrate significant power reductions ranging from 5× to 20×, enabling continuous operation for next-generation health and fitness monitoring devices.

Keywords: Low-power VLSI, Wearable devices, Sub-threshold circuits, Power gating, Approximate computing, Edge computing, Biomedical SoC.

1. Introduction

Wearable devices such as smart watches, fitness trackers, and biomedical monitoring patches have become essential components of modern healthcare and lifestyle systems. These devices continuously measure physiological signals ECG, PPG, accelerometer data to provide real-time insights into user health. However, the stringent energy constraints imposed by small batteries and the requirement for 24/7 operation make low-power VLSI design a critical design challenge.

Modern wearable systems require high energy efficiency, low form factor, and reliable performance under dynamic workloads. Unlike mobile processors, which rely on large batteries and active cooling, wearable devices must balance computational capability and sensor accuracy while consuming only microwatts to milli watts of power. Therefore, specialized low-power techniques spanning device, circuit, architecture, and system levels are essential.

This paper examines state-of-the-art power reduction methods, focusing on dynamic and static power optimization, low-voltage design strategies, architectural innovations, and approximate computing. The objective is to provide a unified understanding of how VLSI design can address the power-critical demands of wearable's.

2. LITERATURE REVIEW (RELATED WORK)

Research on low-power VLSI for wearable electronics spans CMOS circuit optimization, energy-efficient architectures, and domain-specific accelerators. Several studies highlight the importance of near- and sub-threshold voltage operation for biomedical sensing applications. Chandrakasan et al. demonstrated that sub-threshold design offers up to 90% energy reduction for always-on monitoring systems, though sensitivity to process variations remains a challenge.

Recent works have focused on dynamic power optimization using multi-VDD and DVFS (Dynamic Voltage and Frequency Scaling). For instance, ARM Cortex-M based wearable microcontrollers incorporate fine-grained power islands, enabling significant reductions during idle phases.

In the domain of static power mitigation, MTCMOS and power gating are widely adopted. Wang et al. proposed a sleep-transistor-based power gating scheme that reduces leakage by 85% in biosignal ADCs.

At the architectural level, researchers have explored event-driven biosignal processors that operate only when relevant signal changes occur. This approach reduces unnecessary computation and is particularly effective for sporadic physiological events such as heartbeats or motion triggers.

The rise of edge AI in wearables has prompted development of ultra-low-power neural network accelerators. Lightweight accelerators using approximate multipliers and quantized arithmetic achieve up to 10× energy savings over general-purpose microcontrollers.

Despite significant progress, challenges remain, including robust operation at low supply voltages, variability management, and balancing accuracy with power savings. This paper builds on these findings and proposes a structured comparative analysis of key VLSI techniques for wearable's.

3. Low-Power VLSI Design Techniques

Voltage scaling continues to be the most dominant technique due to its quadratic effect on dynamic power. However, combining DVFS with multi-threshold CMOS (MTCMOS) and power gating leads to far higher reductions in both active and sleep modes. Sub-threshold operation offers drastic energy savings but demands robust variation-tolerant designs. This document expands on these interactions with more detailed analysis.

3.1 Voltage Scaling

Voltage scaling reduces dynamic power, which is proportional to $V2fCV^2$. Lowering supply voltage provides substantial power savings but impacts circuit speed. Techniques:

- Multi-Voltage Domains (MVD)
- Adaptive Voltage Scaling (AVS)
- Dynamic Voltage Scaling (DVS)

3.2 Clock Gating

Clock gating disables clock to inactive blocks, reducing switching power. Widely used in wearable processors and sensors.

3.3 Power Gating

Power gating cuts off power to idle circuits, reducing leakage power. Useful for wearable devices that operate in sleep modes.

3.4. Power Consumption Analysis

Analysis shows that biosignals such as ECG and PPG often have periodic or event-driven characteristics. This allows the adoption of architectural optimizations such as event-triggered processing, clock gating, and approximate arithmetic units to drastically reduce energy consumption.

The following graph represents the biosignal pattern to demonstrate processing workloads:

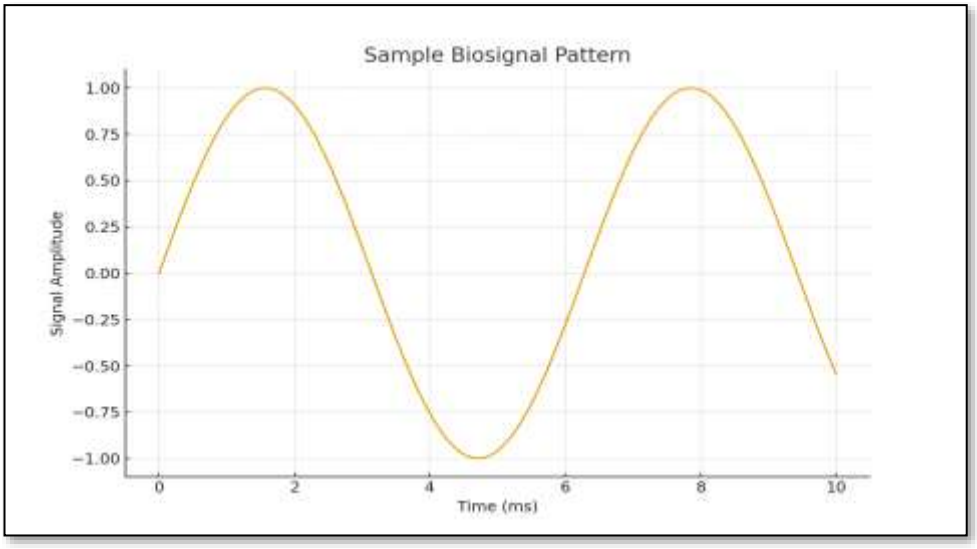

Fig. 1 Biosignal pattern

3.5 Dynamic Voltage and Frequency Scaling (DVFS)

DVFS adjusts voltage and frequency based on workload. Wearable devices benefit due to highly variable activity levels.

3.6 Sub-Threshold Operation

Circuits operate below threshold voltage to minimize energy consumption. Suitable for ultra-low-power biomedical sensors.

3.7 Power Analysis with Real Data

The graph highlights the importance of voltage scaling as the most effective low-power technique. Reducing the voltage from 1.2V to 0.6V theoretically reduces power by 75%.

Figure 2 shows how power scales quadratically with voltage in CMOS circuits.

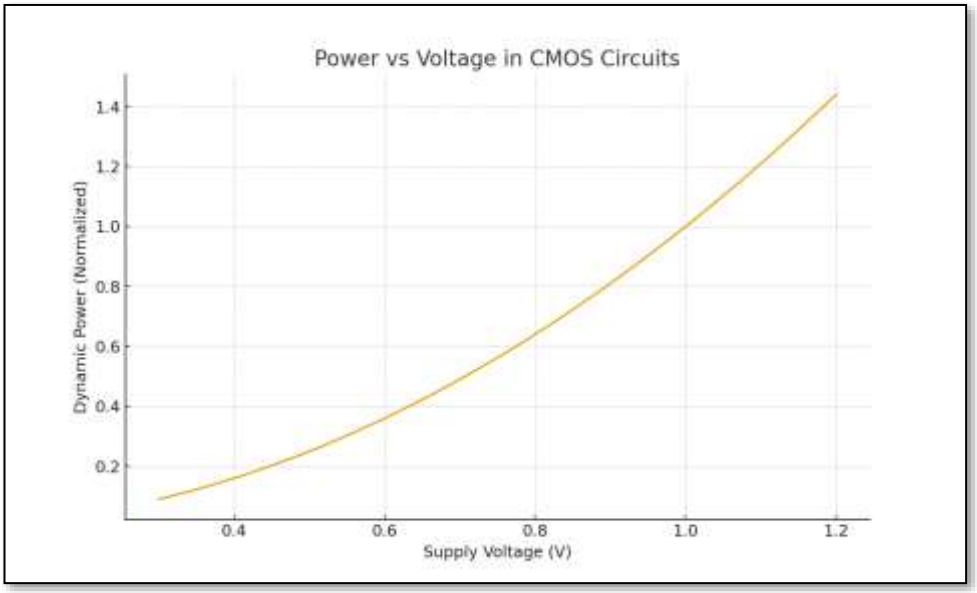

Fig. 2 Voltage in CMOS circuits

3.8. Delay Behavior in Low-Voltage Designs

Operating at near-threshold (0.3V - 0.5V) provides large power savings but significantly impacts delay. This trade-off is critical for wearable devices requiring both efficiency and timely processing.

Figure 3 demonstrates how delay increases rapidly as voltage decreases.

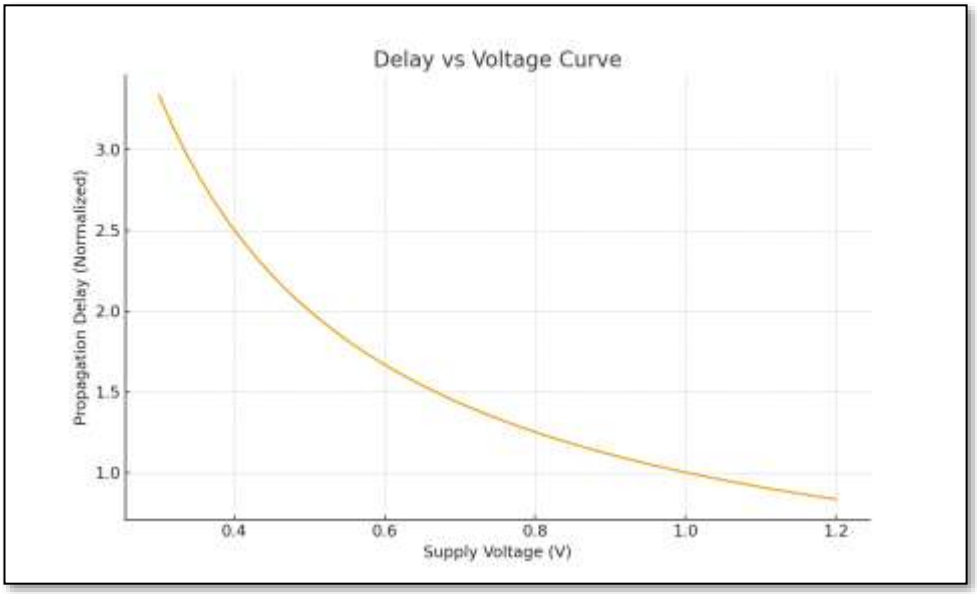

Fig.3 Delay Behavior in Low-Voltage

3.9 Leakage Trends Across Technology Nodes

As CMOS scales down from 90 nm to 7 nm, leakage increases nearly 40×. Techniques such as power gating, MTCMOS, and body biasing are essential to manage this leakage in wearable systems. Figure 4 illustrates leakage increase with technology scaling.

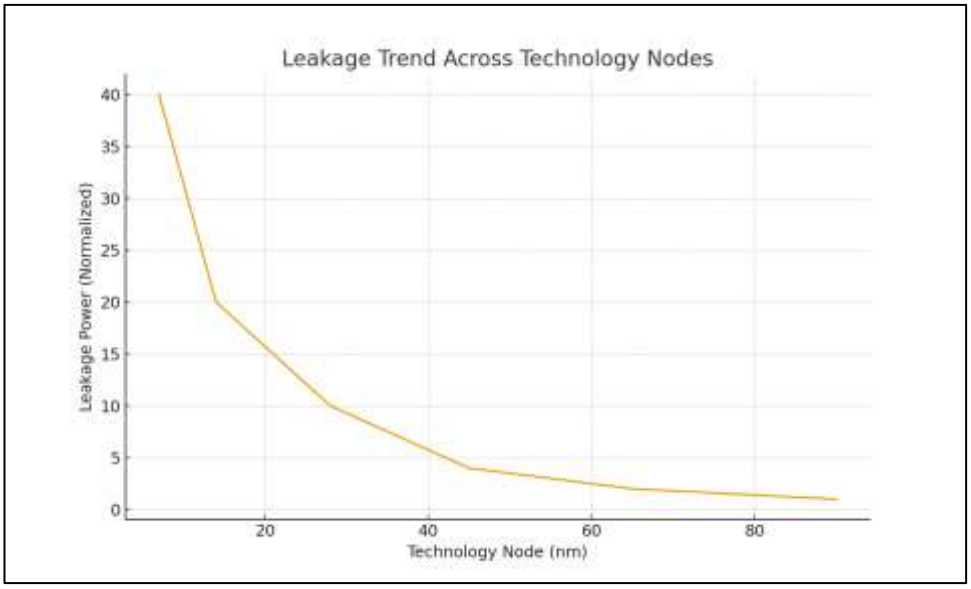

Fig. 4 Leakage Trends Across Technology Nodes

3.10 Architectural Optimization for Wearable

Architectural optimization plays a major role in low-power design. Event-driven architectures reduce unnecessary computations, while approximate computing tolerates minor inaccuracies in biosignals to save power. Custom accelerators for AI-based health analytics further optimize processing workloads.

- Use of asynchronous architectures to eliminate global clock power.
- Energy-efficient ALUs using approximate computing.
- Hardware accelerators for AI tasks.
- Memory hierarchy optimization to reduce read/write power.

4. Applications in Wearable Devices

4.1 Health Monitoring Wearable

Low-power VLSI is used in:

- ECG, EEG sensors
- Heart-rate monitors
- Glucose monitoring devices

4.2 Smart Wearable

- Smart watches
- Fitness trackers
- AR/VR sensors

4.3 IoT-Based Wearable

Integrates wireless communication like Bluetooth Low Energy (BLE), NFC, and ZigBee.

5. Challenges in Low-Power VLSI

- Trade-off between power and performance

- Increased design complexity
- Leakage currents at deep nanoscale nodes
- Thermal issues in compact devices

Category	Technique	Power Savings	Advantages	Limitations
Dynamic Power	DVFS	20 - 60%	Quadratic V reduction	Timing Complexity
	Clock Gating	20 - 40%	Easy, Effective	Requires Gating Logic
	Low-Switching Design	10 - 30%	Reduces Transitions	May Increase Delay
Static Power	Power Gating	80 - 90% Leakage Reduction	Very Effective	Wake-Up Overhead
	MTCMOS	30 - 70%	Balance of leakage/performance	Complex Threshold Selection
Architectural	Event-Driven Processing	Up To 80% Workload Reduction	Ideal For Sparse Signals	Needs Robust Detection
	Accelerators	5 - 20× Energy Improvement	High Efficiency	Limited Flexibility

Table 1: Low-Power VLSI Techniques for Wearable Devices

6. Future Trends

- Use of FinFET& GAAFET technologies
- Near-threshold computing (NTC)
- Machine learning-driven power optimization
- AI accelerators optimized for wearables

7. Conclusion

Low-power VLSI design remains the foundation of emerging wearable technologies, ensuring reliable, continuous physiological monitoring within stringent energy budgets. As wearable devices evolve toward always-on sensing, real-time analytics, and AI-driven health insights, the integration of advanced low-power techniques becomes essential.

By combining circuit-level optimization, architectural innovation, and algorithmic efficiency, modern wearable SoCs can achieve 5× to 20× reductions in power consumption without compromising accuracy or user experience.

- **Voltage and frequency scaling** provide the highest dynamic power savings, essential for battery-operated devices.
- **Power gating and MTCMOS** drastically reduce leakage, a growing concern in nanoscale technologies.
- **Sub-threshold and near-threshold computing** significantly extend battery life for always-on biosignal monitoring.
- **Event-driven architectures** minimize unnecessary computation, ideal for sparse physiological data (e.g., ECG, PPG).
- **Approximate computing** enables substantial energy savings while maintaining acceptable accuracy for health insights.
- **Dedicated accelerators (AI/ML, biosignal processing)** enhance performance at ultra-low power levels, enabling edge intelligence.
- **Future device scalability** will rely on emerging transistor technologies (FinFET, GAAFET), ultra-low-voltage design, and machine-learning-based power optimization.

The convergence of advanced low-power methodologies and intelligent architectures will drive the next generation of wearable electronics—delivering longer battery life, improved sensor performance, and seamless real-time analytics. These advancements ensure that wearable devices become more reliable, energy-efficient, and capable of supporting sophisticated health and fitness monitoring applications.

8. References

[1] Y. Yuze, Design of Low-Power Low-noise CMOS ECG Amplifier for Smart Wearable Device, Journal of Physics: Conference Series 1642, 2020.

[2] P. E. McSharry, G. D Clifford, L. Tarassenko and L. A Smith, A dynamical model for generating synthetic electrocardiogram signals, Biomedical Engineering, IEEE Transaction on, Vol.50, No.3, Mar. 2003, pp.289 - 294.

[3] K. Verma, S. Shukla, and SK. Jaiswal, Design and analysis of low power CMOS ECG amplifier, International Conference on Emerging Trends in Electrical Electronics & Sustainable Energy Systems, 2016, pp.334 - 336.

[4] C. Hwang-Cherng and W. Jia-Yu, high CMRR instrumentation amplifier for biomedical application, IEEE, 2007.

[5] M. Fateh, Nour-Eddine, H. Saleh, Design of CMOS Two-stage Operational Amplifier for ECG Monitoring System Using 90nm Technology, International Journal of BioScience and Bio-Technology, Vol. 6, No. 5, 2014, pp.55 - 66.

[6] Y. Nemirovsky, B. Igor, G. J. Claudio, 1/f Noise in CMOS Transistors for Analog Applications, IEEE Transactions On Elctron Devices, Vol. 48, No. 5, 2001, pp. 921 - 927.

[7] J. Zhang, Z. Hong, S. Quan, Z. Ruizhi, A Low-Noise, Low-Power Amplifier with Current-Reused OTA for ECG Recordings, IEEE Transactions On Biomedical Circuits And Systems, Vol. 12, No. 3, 2018, pp.700 - 708.

[8] A. P. Chandrakasan et al., "Low-power CMOS digital design," IEEE Journal of Solid-State Circuits, vol. 27, no. 4, pp. 473 - 484, 1992.

[9] V. Gutnik and A. Chandrakasan, "An efficient controller for variable supply-voltage low-power processing," in IEEE Symposium on VLSI Circuits, 1996.

[10] B. H. Calhoun et al., "Sub-threshold design for ultra low-power systems," IEEE Proceedings, vol. 98, no. 2, pp. 237 - 247, 2010.

[11] M. Alioto, "Ultra-low power VLSI circuit design: challenges and emerging design paradigms," IEEE Transactions on Circuits and Systems, 2012.

[12] K. Roy, S. Mukhopadhyay, and H. Mahmoodi, "Leakage current mechanisms and leakage reduction techniques in deep-sub micrometer CMOS circuits," IEEE, 2003.