Design of Three Stage Dynamic Comparator with Tail Transistor using 20nm FinFET Technology for ADCs

Monalisa chatterjee[1], Ravish Gupta[2]

[1] *Research Scholar, Department of Electronics & Communication, Dr. CV Raman University, Kota, Bilaspur, Chhattisgarh, India*

[2] *Asst. Professor, Department of Electronics & Communication, Dr. CV Raman University, Kota, Bilaspur, Chhattisgarh, India*

Abstract*— According to this article, one of the key disadvantages is excessive power consumption and offset in CMOS based comparators. At scale down technology, CMOS suffers with short channel effect and leakage current. To address these challenges, FinFET technology is used in threestage dynamic comparators instead of traditional circuit designs. The energy efficiency of FinFET-based dynamic comparators is higher than that of CMOS, and the short channel effect and leakage current are decreased. Furthermore, a new design of FinFET-based three stage dynamic comparators with tail transistors was created and simulated using the cadence virtuoso environment. In comparison to three-stage dynamic comparators without tail transistors, the three-stage dynamic comparator with tail transistor in this approach decreases offset, power consumption, and energy consumption. Both the standard three stage dynamic comparators without tail transistor and the modified three stage dynamic comparators with tail transistor are implemented in the same 20nm FinFET technology for easy comparison. According to simulation results, the modified three stage comparator decreases power consumption by 20% it has a 17% energy efficiency.

Keywords*— CMOS, FinFET, Dynamic comparators, Input referred noise, Power Consumption, Tail transistor.

I. INTRODUCTION

The comparator is an essential element in various types of Analog-to-Digital Converters (ADCs) [1], [2]. The input referred noise, comparator speed, offset, and kickback noise in particular, limit the ADC sampling rate and accuracy in high-resolution high-performance SAR ADCs. In this case, it is critical to create a high-performance comparator. In recent years, there have been several reports of comparator structures. The Strong-ARM latch in [3] and [4] is a wellknown design. It offers a number of advantages, including rail-to-rail outputs, very less static power, and quick contrast to positive feedback [4]. It does, however, have certain restrictions. From the beginning, the speed of regeneration is regulated through the smaller source of current under the latch. The input pair transistors serve as the current source in this case. The current source is restricted due to the input pair's common-mode input of VDD/2, which affects the speed of regeneration. Furthermore, an increased supply voltage is necessary due to the many stacked transistors. These concerns do not exist in two-stage comparators. [5-11]. Consider the 2-satge comparator of Miyahara's [10], whose speed of regeneration is no longer restricted through the limited current source, which is two times bigger than the Strong-ARM latch's VDD/2. Another advantage is a reduction in the number of stacked transistors. The power supply voltage requirement is relaxed as a result of this. Whereas the 2-satge comparator [10] improves speed, it may be enhanced further as follows. The mobility of pMOS holes is restricted (2–3 times that of nMOS electrons) in this usage of the PMOS-based latch, restricting the regeneration speed. The goal of [13] would be to use nMOS transistors for the latch input pair rather than bipolar transistors, which would considerably enhance regeneration speed. Meanwhile, the nMOS transistors for the preamplifier input pair must be kept by [13]. In this [13], the nMOS input pairs can be used for both the first-stage preamplifier and latch-stage, which improves the speed of regeneration by adding an additional preamplifier stage. Furthermore, at the commencement of the comparison, all input combinations operate in the saturation zone, ensuring minimal input referred noise. Voltage gain is provided by the extra preamplifier stage, which assists in boosting regeneration speed and decreasing noise and input referred offset. In terms of input referred noise and speed, the threestage comparator [13] outperforms the three-stage comparator [12]. All of the designs mentioned above are implemented with CMOS technology; in these designs, power and latency are the two key considerations when examining the performance of a comparator.

In VLSI, designers cannot lower all of the factors at once; instead, can only reduce one parameter at a time. The linked elements might be lowered depending on the application or demand. Due to the shortcomings of present technology, the purpose of this article is to address such shortcomings using FinFET technology.

FinFET is an abbreviation for Fin Field Effect Transistor [14]. To put it another way, a FinFET is a multi-gate transistor. The channel length between the source and drain is 20nm. When compared to conventional technologies, FinFET technology provides several advantages. FinFET's come in a variety of configurations. Drive current is strong, channel length is short, and latency is minimal, resulting in faster operation [15]. There is a short channel effect that has been suppressed. Because the channel length is so short, more FinFET's may be embedded in a given area. Recently, designed an ADCs with modified versions of comparators, which are designed with different FinFET technologies to achieve less power consumption and noise [16-17]. In this work, we utilize FinFET libraries and related transistors to implement and analyze comparator architecture. The threestage comparator in this study, implemented in 20nm FinFET technology, improved energy efficiency by 17% compared to standard three-stage

comparators, while the suggested improved version and reduces power consumption by 20%. The following is how this brief is arranged. Section II examines FinFET Characteristics and Modeling, while Section III goes into the conventional dynamic comparators. Section IV examines the modified three-stage comparator. The outcomes of the simulations are shown in Section V. Section VI brings the brief to a conclusion.

II. FINFET CHARACTERSTICS AND MODELLING

FinFET is an abbreviation for Fin Field Effect Transistor. Multi-gate MOS transistors are another name for them. The conducting channel of a FinFET is encircled by a silicon wafer, which serves as the transistor's substrate. The channel length is determined by the device's thickness. It is known as a non-planar transistor. It usually consists of two gates. This double gate transistor is either silicon wafer or SOI based (Silicon on Insulator). The kind of FinFET is determined by the substrate on which it is built. The multi gate FinFET was utilized in this study to suppress or limit offstate leakage current and to enable a good amount of current in the drive or ON state [14]. These multi gates also assist in electrical channel regulation. FinFET technology can be used to solve performance concerns with planner transistors. FinFET plays a key role in ULSI (Ultra Large-Scale Integrated Circuits) devices. Here, FinFET's are two sorts, those are: 1) Single Gate (SG), also known as 3T FinFET's (three terminal), and 2) Multi Gate (MG), also known as 4T FinFET's (four terminal).

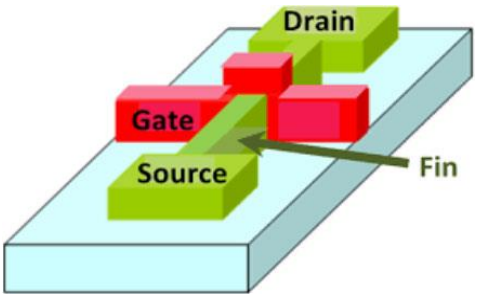

Fig. 1. Structure of FinFET

There are two types of single gate transistors: Bulk FinFET and SOI FinFET are the two types of FinFET. FinFET is the most recent VLSI technology. It has the following advantages due to its multi gate structure: high drive current, short channel length, low power consumption, superior performance, and high speed. The channel length will be reduced even more in the future, to FinFET 10nm.

We used LUT-based Verilog-A models of Tunnel FETs created by the NDCL group at Penn State University and accessible in Nano-hub [15] in this research. The Cadence Virtuoso environment has been inserted into these Verilog-A models. Then, NTFET, PTFET and FinFET device symbols were created and circuits are designed using the device symbols. The device parameters of TFET devices are summarized in Table I.

TABLE I FINFET DEVICE PARAMETERS [15]

Parameters	Si FinFET
Gate Length (L_g)	20nm
EOT (HfO_2)	0.7
Source Doping (cm^{-3})	$1x10^{20}$
Drain Doping	$1x10^{20}$
Body Thickness (T_b)	10nm
Gate work function (eV)	4.55

III. CONVENTIONAL DYNAMIC COMPARATORS

A. Outlining of 2- stage comparator

The Fig.2. presents the 2-stage comparator of Miyahara's. The amplification phase, regeneration phase and reset phase are the three phases of operation. When CLK='0' the comparator outputs are in reset phase. And when CLK = '1', the input signals VIN and VIP are amplified and transmitted to the latch stage. OUTN and OUTP regenerate to GND or VDD during the regeneration phase. In this latch stage designed with pMOS input pair, because of this has provides a slower regeneration speed.

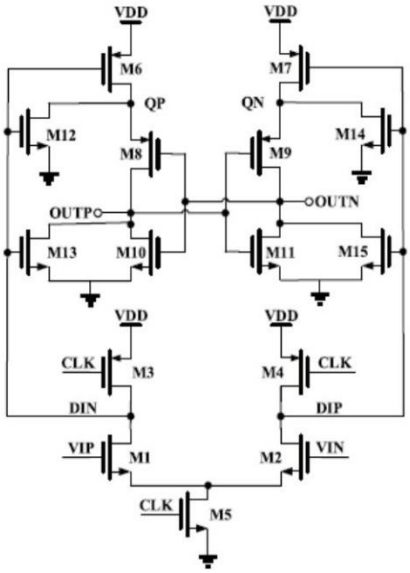

Fig.2. 2- Stage Comparator [10]

B. Outlining of 3- stage comparators

The 3-stage comparators are shown in Fig. 3 and Fig. 4. The three phases of operation, namely the regeneration phase, amplification phase and reset phase are also performed here. When CLK='0', the comparator is in reset phase. The input signal VIN and VIP are amplified and delivered to the latch stage during the amplification phase (CLK = 1). OUTP and OUTN regenerate to VDD and GND respectively, during the regeneration phase. Fig. 3 depicts the three-stage comparator used in this study. The three steps are linked one to the next. The main change from the Miyahara comparator is the addition of a second preamplifier (the second stage). This additional preamplifier serves as an inverter, allowing latch stage to

operate faster by using the M11–M12 transistors of nMOS pair instead of the pMOS pair The additional preamplifier additionally adds voltage gain, increasing speed of regeneration, reducing noise and input referred noise.

Although the additional preamplifier speeds up the process, it also adds to the delay since the amplified signal must pass through two stages instead of one before reaching the latch stage. Overall, 15% of the input referred noise is decreased according to the input pair's assured saturation region, and the 6% of speed is enhanced due to lower parasitic capacitances.

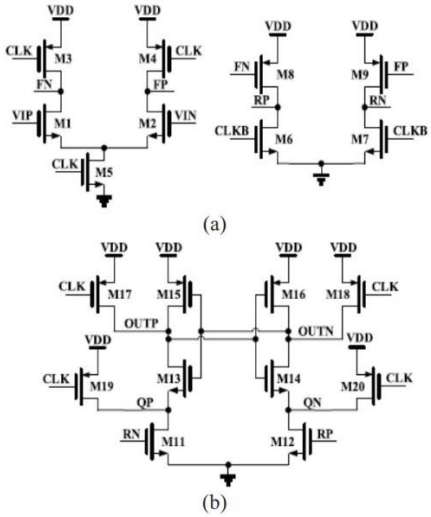

Fig.3. Three-stage comparator (a) First 2- stages of preamplifiers (b) latch stage [13]

This explanation presented a change of a three-stage comparator, as illustrated in Fig. 4, to minimize kickback noise and enhance speed. The main difference between the modified version and the original version in the preceding section is that contains the extra stage of pre-amplifier as shown in Fig. 4(b) as well as Fig. 4(c) shows the extra routes M29–M32 transistors in the latch stage. The pMOS pair M11–M12 transistors are used in the additional first two stages to cancel out the nMOS pair M1–M2 transistors for feedback noise. Furthermore, the additional routes M29–M32 transistors are apply extra signal to the latching nodes OUTP and OUTN, increasing the speed of regeneration and suppressing the noise and input referred offset. In general, the redesigned three-stage comparator has quicker speed, lower kickback noise reduced noise and input referred offset. It's ideal for SAR ADCs with high-speed and high-resolution.

IV. MODIFIED THREE STAGE COMPARATORS WITH TAIL TRANSISTOR

As a result, it's required to evaluate whether the prior three step comparators' higher power usage is justified. As seen in Fig. 3, Its outputs FN and FP connected to GND after the first-stage amplification. As a result, the gate–source voltage of the second-stage input pair M8–9 is equal to VDD. As a consequence, M8–M9 transistors current is strong enough to rapidly pull up RP and RN. As illustrated in Fig. 5, the tail transistor was introduced to the following step (latch) to minimize power usage. The circuit's functioning is as follows: Furthermore, in comparison to the Miyahara comparator's first-stage output load (M6–M7 transistors and M12–15 transistors in Fig. 1), the three-stage comparator's first-stage output load is only M8–M9 transistors in Fig. 3.

The output load is lowered by many orders of magnitude, resulting in faster amplification. When compared to threestage comparators without a tail transistor, however, it improves amplification speed while lowering total power consumption. Fig.4 (d) shows the transient response of 3- stage comparator.

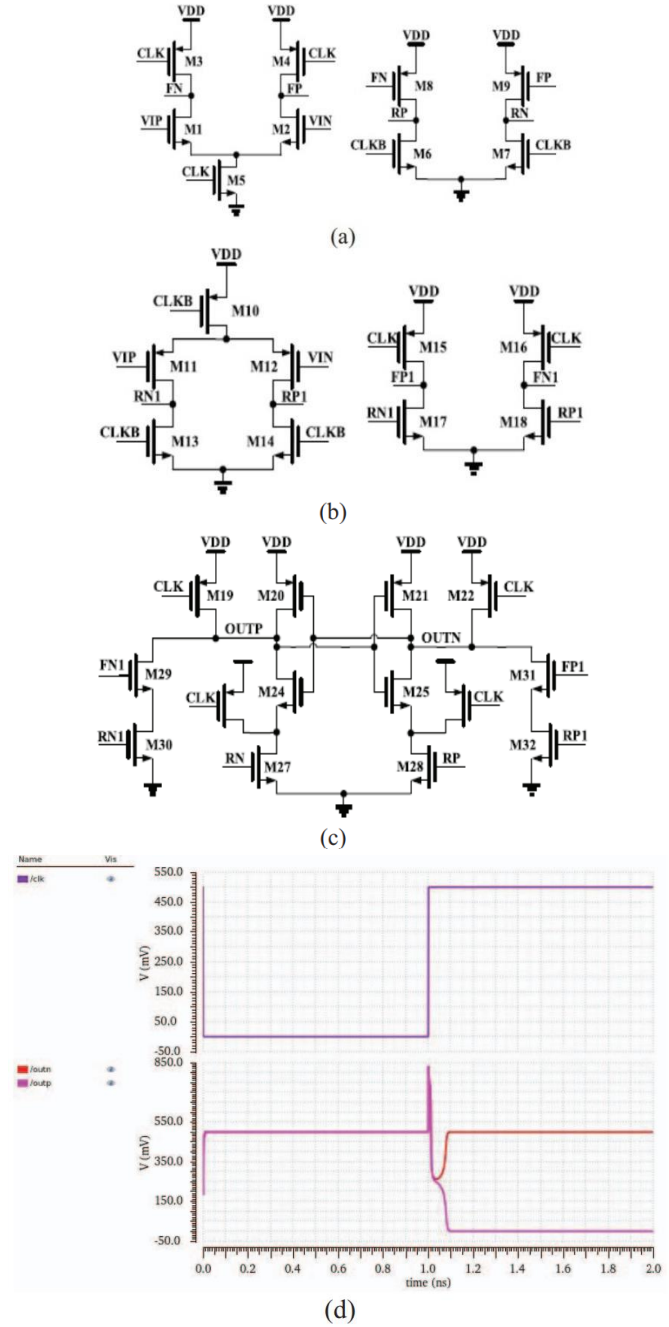

Fig. 4. 3-stage comparator. (a) 2-stages of preamplifiers with nMOS pair. (b) another 2-stages of preamplifiers with pMOS pair. (c) latch stage [13] (d) Transient response.

The three-stage comparator's transient simulation is shown in Figure 5 (b) at 1mV voltage difference in between input pair. First, rather than the first-stage output, the gate of M6–M7 transistors are shown in Fig. 3 is linked to CLKB. The parasitic

capacitance at the first-stage output is reduced as a result. Second, rather than being linked to the second-stage output, P3-gate is connected to CLK. The parasitic capacitance at the second-stage output is reduced as a result. Finally, the parasitic capacitance is reduced in initial stage. More crucially, it ensures that the M1–2 drain is at VDD at the start of the comparison. This is significant due to the input pair's saturation zone assists in the reduction of input referred noise.

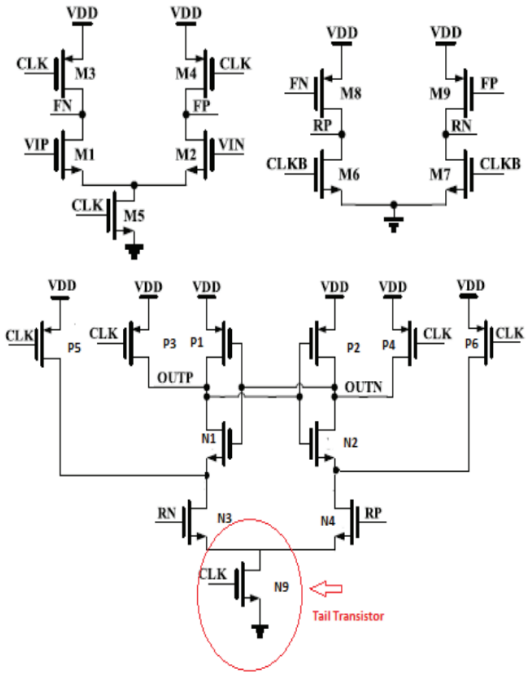

Fig. 5(a). Modified three stage comparator of Fig.3 with tail transistor

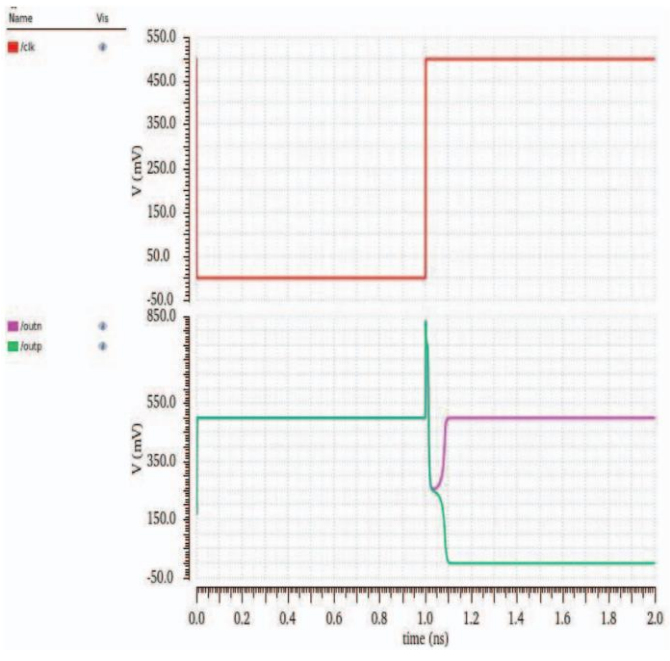

Fig. 5(b) Transient response of three stage comparator with tail transistor

When the tail transistor is used in the latch stage, there is no static path between VDD and GND when CLK='0,' which reduces power consumption and improves the overall energy efficiency of the comparator. As seen in Fig 5(c), increasing the tail transistor width reduces the amplification delay. As illustrated in Fig.6, the tail transistor was also added to the three-stage comparator (Fig. 4).

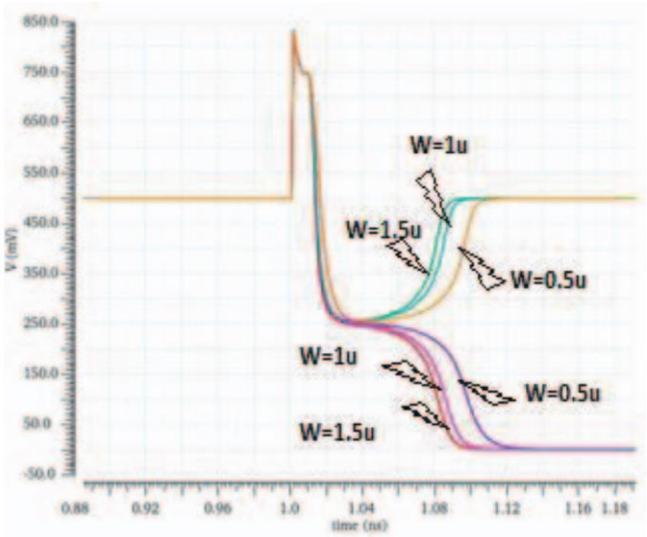

Fig.5(c) Transient response of three stage comparator with tail transistor.

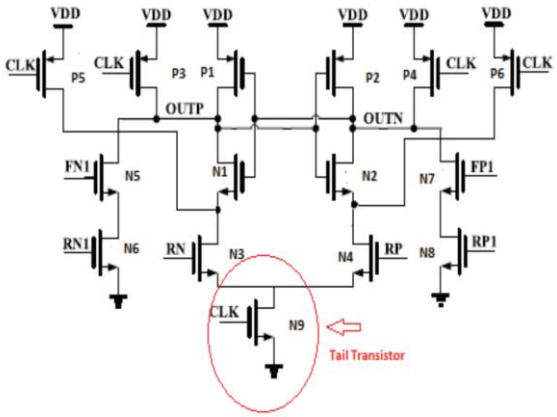

Fig.6(a). Modified three stage comparator of Fig.4 with tail transistor

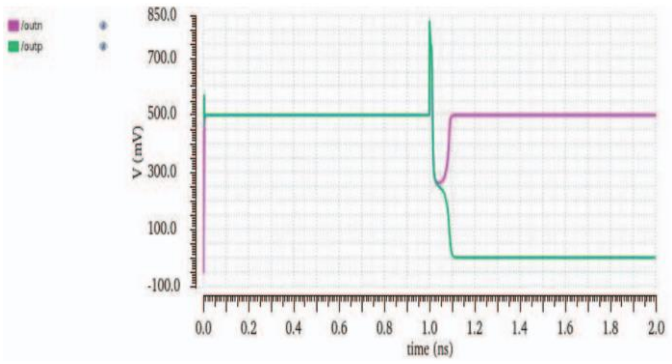

Fig. 6(b) Transient response of three stage comparator (Fig.4) with tail transistor

The following circuit operates as follows. When CLK is 0 and CLKB is 1, during reset phase. The Fig. 4 shows, RP1 and RN1 are set to GND, whereas the FP1 and FN1 are set to VDD. This disables N6, N8, and N9 in Fig. 6, guaranteeing that the additional route N5-9 is free of static current. CLK climbs to 1 and CLKB falls to 0 during the amplification phase. Fig. 6 shows how RP1 and RN1 cause VDD.

comparators without tail transistor by 20%, 24.5% of Fig.3 and Fig.4 respectively. Meanwhile, the delay of 3-stage comparators with tail transistor is higher than the 3-stage comparators without tail transistor by 2.4%, 14% of Fig.3 and Fig.4 respectively. The energy efficiency of 3-stage comparators with tail transistor is higher than the 3-stage comparators without tail transistor by 17%, 10% of Fig.3 and Fig.4 respectively.

TABLE II COMPARISONS OF THE THREE STAGE COMPARATORS WITH AND WITHOUT TAIL TRANSISTOR

Input Voltage Difference	3-stage comparators without tail transistor						3-stage comparator with tail transistor					
	Fig.3			Fig.4.			Fig.5.			Fig.6.		
	Power (uW)	Delay (pS)	Energy (fJ)	Power (uW)	Delay (pS)	Energy (fJ)	Power (uW)	Delay (pS)	Energy (fJ)	Power (uW)	Delay (pS)	Energy (fJ)
1mV	1.92	80	0.154	2.65	73	0.19	1.55	82	0.13	2	85	0.17
5mV	1.9	68	0.130	2.65	58	0.15	1.55	70	0.11	1.99	70	0.14
10mV	1.9	56	0.11	2.67	46	0.12	1.53	60	0.09	1.99	60	0.12
20mV	1.89	44	0.083	2.7	30	0.08	1.51	44	0.06	2.1	50	0.11
40mV	1.89	36	0.068	2.8	30	0.084	1.5	36	0.05	2.15	32	0.07
60mV	1.88	32	0.06	3	30	0.09	1.5	32	0.045	2.35	30	0.07
80mV	1.87	30	0.059	3.1	27	0.083	1.5	28	0.04	2.4	28	0.07
100mv	1.85	30	0.055	3.1	25	0.077	1.5	28	0.04	2.45	28	0.07

Then FN1 and FP1 become GND. The additional routes in Fig. 6 are switched on for a brief duration, since the RP1 and RN1 raising occurs before the FP1 and FN1 falling, a differential current is drawn from the latching nodes OUTN and OUTP.

This creates a voltage difference between OUTN and OUTP, which speeds up regeneration phase while lowering comparator noise and input offset. The additional paths in Fig. 6 are switched off again once FN1 and FP1 connected to GND to prevent the static current. In this the extra tail transistor provides the less power consumption compared to three stage comparator (Fig. 4). Fig 6(b) shows the transient response of modified three stage comparator of Fig.4 with tail transistor at 1mV voltage difference in between two inputs. With the variation of tail transistor width, it reduced the amplification delay as show in Table III.

V. RESULTS AND DISCUSSION

This section contrasts the proposed three-stage comparators with the conventional there-stage comparators without tail transistor. For fair comparison, all comparators are simulated with using of same 20-nm FinFET technology. The design of all comparators is also used the same transistor aspect ratio (1u/20nm), so that other specifications can be compared. Table II provides the contrast of this work with the conventional designs. As can be seen, the 3-stage comparators with tail transistor have the smallest delay at various input volage difference. The modified comparators have the power consumption and energy consumptions are lower than [13], without circuit complexity.

Table II presents, the power consumption of 3-stage comparators with tail transistor is smaller than the 3-stage

TABLE III comparisons of the three stage comparators with various widths of tail transistor

Width (um)	3-stage comparator with tail transistor					
	Fig.5.			Fig.6.		
	Power (uW)	Delay (pS)	Energy (fJ)	Power (uW)	Delay (pS)	Energy (fJ)
0.5	1.54	87	0.14	1.99	89	0.18
1	1.55	82	0.13	2	85	0.17
1.5	1.56	75	0.11	2.1	78	0.16

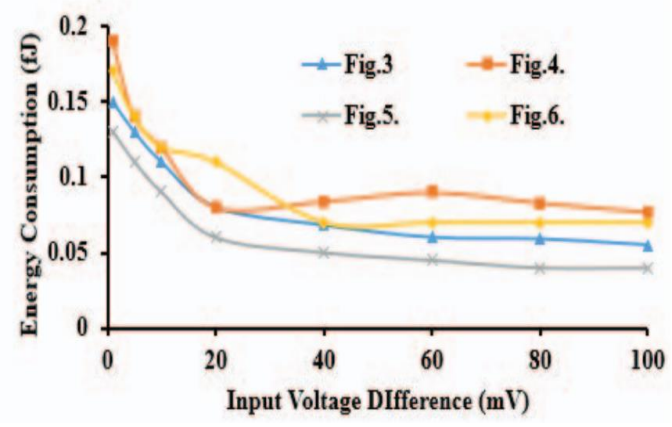

Fig.7. shows the Energy consumption of different three stage comparators. Table III represents the power, delay and energy of three stage comparators with various widths of tail transistor at 1mV input voltage difference.

VI. CONCLUSION

In this paper, designed an FinFET based three-stage dynamic comparators instead of CMOS based circuit designs to improve the overall energy efficiency. Moreover, utilizing the cadence virtuoso environment, a new design of FinFETbased three-stage dynamic comparators with tail transistors was constructed and simulated. In this technique, the threestage dynamic comparator with tail transistor reduces input referred noise, power consumption, and speed when compared to three-stage dynamic comparators without tail transistors. For ease of comparison, both the regular three stage dynamic comparators without tail transistor and the modified three stage dynamic comparators with tail transistor are built in 20nm FinFET technology. The modified threestage comparator reduces power usage by 20% and it has enhanced a 17% energy efficiency, according to simulation results.

REFERENCES

[1] H. S. Bindra, C. E. Lokin, D. Schinkel, A.-J. Annema, and B. Nauta, "A 1.2-V dynamic bias latch-type comparator in 65-nm CMOS with 0.4-mV input noise," IEEE J. Solid-State Circuits, vol. 53, no. 7, pp. 1902–1912, Jul. 2018.

[2] P. Harpe, E. Cantatore, and A. van Roermund, "A 2.2/2.7fJ/conversionstep 10/12b 40kS/s SAR ADC with data-driven noise reduction," in Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2013, pp. 270–271.

[3] B. Razavi, "The StrongARM latch [A circuit for all Seasons]," IEEE Solid StateCircuits Mag., vol. 7, no. 2, pp. 12–17, Spring 2015.

[4] Y. T. Wang et al., "An 8-bit 150-MHz CMOS A/D converter," IEEE J. Solid-State Circuits, vol. 35, no. 3, pp. 308–317, Mar. 2000.

[5] M. Abbas, Y. Furukawa, S. Komatsu, J. Y. Takahiro, and K. Asada, "Clocked comparator for high-speed applications in 65nm technology," in Proc. IEEE Asian Solid-State Circuits Conf., Nov. 2010, pp. 1–4.

[6] S. Babayan-Mashhadi and R. Lotfi, "Analysis and design of a lowvoltage low-power double-tail comparator," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 22, no. 2, pp. 343–352, Feb. 2014.

[7] J. Lu and J. Holleman, "A low-power high-precision comparator with time-domain bulk-tuned offset cancellation," IEEE Trans. Circuits Syst.I, Reg. Papers, vol. 60, no. 5, pp. 1158–1167, May 2013.

[8] D. Shinkel et al., "A double-tail latch-type voltage sense amplifier with 18ps setup+hold time," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2007, pp. 314–315.

[9] M. van Elzakker et al., "A 10-bit charge-redistribution ADC consuming 1.9 µW at 1 MS/s," IEEE J. Solid-State Circuits, vol. 45, no. 5, pp. 1007–1015, May 2010.

[10] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise selfcalibrating dynamic comparator for high-speed ADCs," in Proc. IEEE Asian Solid-State Circuits Conf., Nov. 2008, pp. 269–272.

[11] M. Brandolini et al., "A 5 GS/s 150 mW 10 b SHA-less pipelined/SAR hybrid ADC for direct-sampling systems in 28 nm CMOS," IEEE J. Solid-State Circuits, vol. 50, no. 12, pp. 2922–2934, Dec. 2015.

[12] H. Zhuang, W. Cao, X. Peng X, H. E. Tang . A Three-Stage Comparator and Its Modified Version With Fast Speed and Low Kickback," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 29, no. 7, July 2021.

[13] D. Hisamoto, W.C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.J. King, J. Bokor, C. Hu, "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," IEEE transactions on electron devices, vol. 47, no. 12, pp. 2320-2325, Dec. 2000.

[14] H. Liu, M. Cotter, S. Datta, V. Narayanan, "Technology assessment of Si and III-V FinFETs and III-V tunnel FETs from soft error rate perspective," International Electron Devices Meeting, pp. 25-5, Dec 2012, IEEE.

[15] D. Luu, L. Kull, T. Toifl, C. Menolfi, M. Brändli, P.A. Francese, T. Morf, M. Kossel, H. Yueksel, A. Cevrero, I. Ozkaya, A 12-bit 300- MS/s SAR ADC with inverter-based preamplifier and common-moderegulation DAC in 14-nm CMOS FinFET". IEEE Journal of SolidState Circuits, vol. 53, no.11, pp.3268-3279, Nov 2018.

[16] D. Dermit, M. Shrivas, K. Bunsen, J.L. Benites, J. Craninckx, E. Martens, "A 1.67-GSps TI 10-bit ping-pong SAR ADC with 51-dB SNDR in 16-nm FinFET", IEEE Solid-State Circuits Letters, vol. 3, pp.150-153, July 2020.