Designing A Low Noise Amplifier Using GaN HEMT Of 150nm Technology.

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Abstract—**This paper provides a report of LNA using various techniques. several articles have been published on the topic LNA. Researchers have also found the techniques to figure of merit and performance. The IOT devices required low power, high speed. Now-a-days there is a high demand for circuits which operate at high frequency and low voltage. In CMOS devices also have some limitations like high output conductance, velocity, saturation and deterioration in mobility. LNA acts as very important component of the receiver circuit and hence overall performance also increased. our main aim is to design the LNA which provides good linearity, low noise figure, and good stability and also includes good third order intercept point.**

Index Terms—**LNA-Low Noise Amplifier, IOT-Internet Of Things , GaN-Gallium Nitride, CMOS-Complementary Metal-Oxide-Semiconductor.**

I. Introduction

In modern RF and microwave systems, the Low Noise Amplifier plays a critical role as the first active stage in the receiver chain, where its performance directly impacts the overall system sensitivity and signal quality. A well-designed LNA must provide substantial gain while minimizing added noise to ensure that weak incoming signals can be amplified without degradation. At the same time, high linearity is essential to prevent distortion and intermodulation products when multiple strong signals are present, particularly in crowded spectral environments such as 5G, radar, and satellite communication systems. The trade-off between noise figure, gain, and linearity requires careful optimization of device biasing, matching networks, and transistor selection, making LNA design a complex but vital task.

The use of 150nm GaN HEMT technology offers a compalling solution to these design challenges. Compared to conventional silicon or GaAs processes, GaN devices provide superior power handling and frequency performance, enabling LNAs that combine high gain, wide bandwidth, and robust linearity with improved thermal stability. The 150nm node strikes a balance between performance and manufacturability, supporting operation in the multi-GHz range while maintaining compact device dimensions. By leveraging this technology, the proposed LNA design aims to meet stringent RF front-end requirements, offering an efficient and scalable solution for next-generation wireless and defense applications. The design process involves extensive simulation and co-optimization using industry-standard tools like Keysight ADS, ensuring accuracy from schematic-level to layout-based performance validation.

To achieve optimal performance in the proposed GaN LNA design, several key design parameters must be carefully considered. These include input and output impedance matching for maximum power transfer, noise figure minimization, gain flatness across the desired frequency band, and linearity improvement through proper biasing and transistor sizing. The matching networks are designed using lumped and distributed elements, optimized to minimize reflection coefficients (S11 and S22) and ensure wideband impedance matching. Stability is also a critical concern in high-gain amplifier design; hence, unconditional stability is verified across the operating frequency range using Rollett's stability factor (K-factor) and stability circles.

Advanced simulation tools such as Keysight Advanced Design System are utilized to model the circuit at both the schematic and electromagnetic (EM) levels. Non-linear simulations such as harmonic balance and load-pull analysis are employed to characterize gain compression, intermodulation distortion, and output power under large-signal conditions. Additionally, noise analysis is conducted to extract the minimum noise figure and optimum source impedance, ensuring low-noise performance in practical deployment. The complete design flow—from topology selection to layout implementation and EM simulation—ensures that the final amplifier design meets targeted specifications, including high gain (¿20 dB), low noise figure (¡1.5 dB), high input/output return loss, and excellent linearity (high IP3 and P1dB). These attributes make the designed LNA a suitable candidate for integration into next-generation RF front ends in radar, satellite, and wireless communication systems.

II. Literature Survey

A. A 19–31GHz K/Ka-band Broadband Low Noise Amplifier with High Gain and High Flatness.

This paper presents a Ka-band (32–36 GHz) GaN MMIC single-chip front end built using OMMIC's 100-nm and 60-nm GaN-on-Silicon technology. The chip integrates a high-power amplifier, low-noise amplifier, and T/R switches in a compact 4.7 × 3.0 mm design for phased-array antennas. In receive

mode, it achieves about 3.2 dB noise figure and ¿30 dB gain. In transmit mode, it delivers 35 dBm output power and "16" PAE. The design keeps transistor channel temperatures below 160 °C and uses mixed gate-length devices (100 nm + 60 nm) to improve both noise and power performance. It also represents one of the highest-frequency integrated GaN-on-Silicon front ends reported so far.

B. A > '120-GHz Bandwidth, > '20-dBm Pout, <6-dB Noise- Figure Distributed Amplifier MMIC in a GaN-on-SiC HEMT Technology.

This paper presents a Ka-band GaN MMIC single-chip front-end (SCFE) built using OMMIC's 100-nm and 60-nm GaN-on-Silicon technology. The 4.7 × 3.0 mm chip integrates a high-power amplifier, a low-noise amplifier, and T/R switches for use in active electronically scanned antennas operating from 32–36 GHz. In receive mode, it achieves a low noise figure of 3.2 dB and good gain. In transmit mode, it delivers 35 dBm output power with 16 PAE. Thermal and bias trade-offs are analyzed to keep transistor channel temperature below 160°C. Using both 100-nm and 60-nm GaN transistors improves overall noise and power performance. This SCFE operates at the highest reported frequency for GaN-on-Si MMICs and performs comparably to GaN-on-SiC solutions under continuous-wave testing.

C. A 19–31GHz K/Ka-band Broadband Low Noise Amplifier with High Gain and High Flatness.

This paper describes a design of high flatness broadband monolithic microwave integrated circuit low-noise amplifier (LNA) based on 100-nm gallium-nitride-silicon-carbide (GaN-on-SiC) technology for 19-31 GHz. Common-source (CS) configuration with inductive degeneration has been used for all transistors to fit the input match and noise figure (NF). A parallel RC network and broadband matching networks have been used simultaneously to achieve improved gain flatness at a wide frequency band. The proposed three-stage LNA with a chip area of 2.1×1.3 mm2 exhibits a low NF of 1.4-1.8 dB, a high gain of 20.1-21.1 dB and a gain flatness of ± 0.5 dB. At 26GHz, the output 1-dB compression point (OP1dB) and output third-order intercept point (OIP3) are 20.8 and 32.3 dBm, respectively.

D. Optimizing Low Noise Amplifiers: A Two-Stage Approach for Improved Noise Figure and Stability.

This study introduces a new design for a low noise amplifier (LNA) consisting of two stages taking advantage of the inherent lossy properties of the input matching components. By doing this, the design balances the minimum noise figure (NF) and stability, eliminating the complexities and challenges introduced by feedback networks. Furthermore, the integration of the low-pass filter (LPF) into the design as a noise-matching network ensures improved performance across both the amplifier stages. A comprehensive analytical study is also introduced to delve deep into the relationship between critical LNA parameters, such as stability and noise figures, and the

internal resistance of input-matching inductors. Two C-band LNAs are compared in terms of stability using indigenous 0.25μm GaN technology. The designs are substantiated by fabricating two LNA MMICs for a 5-7 GHz frequency range, having a minimum NF of 1.3 dB and 1.5 dB, with a gain of 15 dB and 16 dB at 6 GHz, respectively. The study reveals that using the proposed approach, there is an overall improvement in NF of 0.2 dB within the frequency of operation. The work entails a way to remove the feedback network in the LNA leading to an improved NF.

TABLE I
LITERATURE SURVEY

Topology	Frequency (GHz)	NF (dB)	Gain (dB)	OIP3 (dBm)
Inductive Source Degeneration (Common-Source)	1–40	1.0–3.5	10–20	28
Drain-to-Gate Feedback	1–40	1.5–3.0	15–25	15
CS with Inductive Source Feedback	10–35	1.8–3.0	12–20	22
Frequency-Selective Parallel Feedback	8–40	1.5–3.0	17–21	25
Cascode LNA	0.5–20+	0.4–2.5	15–25	28
Folded-Cascode/ Stacked LNA	2–50	1.0–3.5	12–22	25
Distributed Amplifier (DA) LNA	5–110	3–8	8–15	20
Resistive-Feedback Broadband LNA	0.5–40	1.5–4.0	10–18	22
Transformer/ Balun-Matched LNA	1–40	0.8–2.5	12–22	28
Noise-Canceling LNA	1–40	0.5–2.5	10–18	21
Neutralized/ Positive-Feedback LNA	1–30	1.0–3.0	15–23	24
Common-Gate Input LNA	10–70	1.5–4.0	8–15	20

Figure Labels: This table compares different LNA (Low Noise Amplifier) designs by showing their usual frequency range, noise level, gain, and linearity, so you can easily see which type is best for your application. Each topology has a special purpose: Inductive source degeneration, gives good noise and easy matching. Drain-to-gate feedback increases stability and gain. Common-source with inductive feedback, improves high-frequency performance. Frequency-selective feedback, uses tuned circuits to work better over a wider band. Cascode LNAs give very good noise, high gain, and strong isolation. Folded-cascode is similar but works well with low supply voltage. Distributed LNAs cover extremely wide frequency ranges but with higher noise. Resistive-feedback types are simple and wideband, but noisier. Transformer-matched LNAs use magnetic coupling to achieve very low noise.
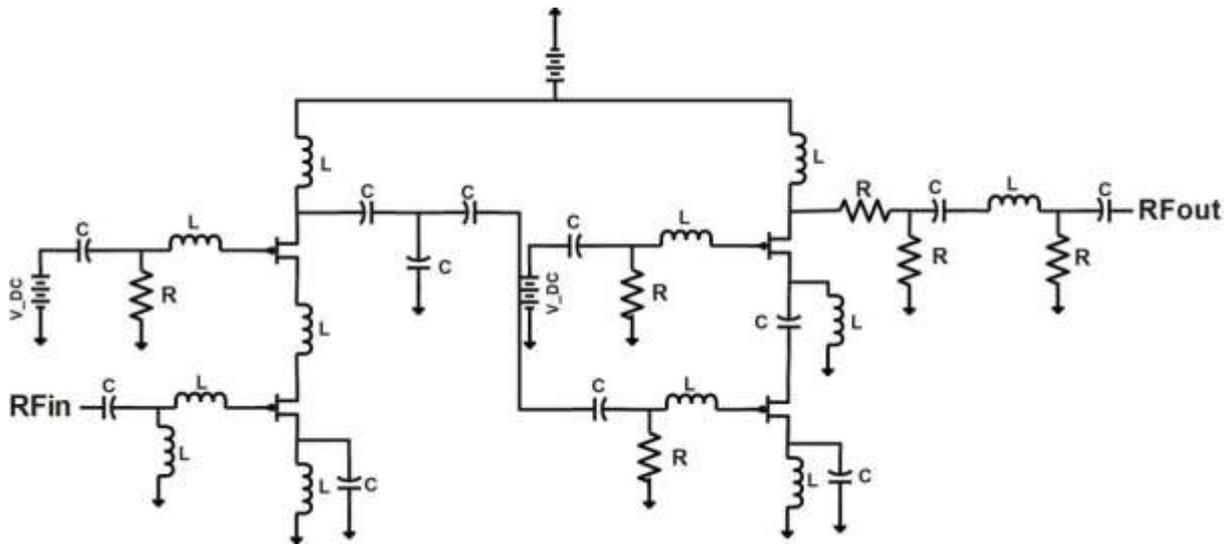
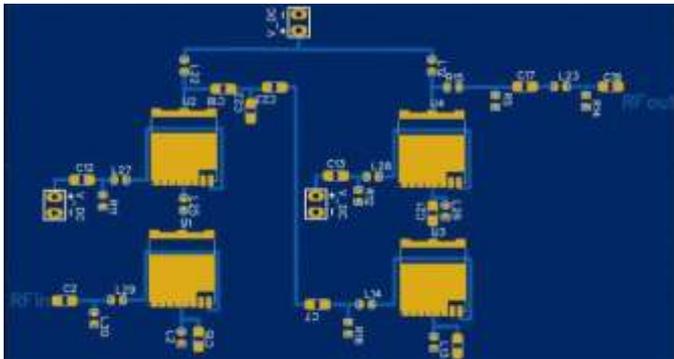Fig. 1. **2-Stage 150-nm LNA(Low Noise Amplifier) Electrical Schematic**

Fig. 2. **Final PCB Layout of Proposed LNA**

The circuit shown is a multi-stage RF amplifier. Its job is to take a small RF signal at the input (RFin) and increase its strength before sending it to the output (RFout).

The input signal first passes through a capacitor that blocks DC and allows only the RF signal to enter. After this, a set of inductors and capacitors are used to match the input signal to the amplifier so that maximum power can enter the circuit. A resistor connected to ground helps keep the input stable and prevents unwanted noise or oscillations.

The signal then reaches the first amplifier stage. This stage uses an active device (like a transistor) that receives DC power through an inductor acting as an RF choke, which blocks RF from entering the power supply. Capacitors around this stage help control the frequency and improve the smooth flow of the signal.

Between the first and second stages, there is an inter-stage matching network made of more inductors and capacitors. The

purpose of this section is to match the output of the first stage to the input of the next stage. This ensures maximum gain and helps maintain stability.

The second amplifier stage works in the same way as the first stage. It further boosts the RF signal. Additional resistors are placed at different points to prevent oscillations and keep the circuit stable while working at high frequencies.

Finally, the signal reaches the output matching network. This section uses inductors and capacitors to match the amplifier output to the load (usually 50ohm). A capacitor at the very end blocks DC and allows only the amplified RF signal to reach RFout.
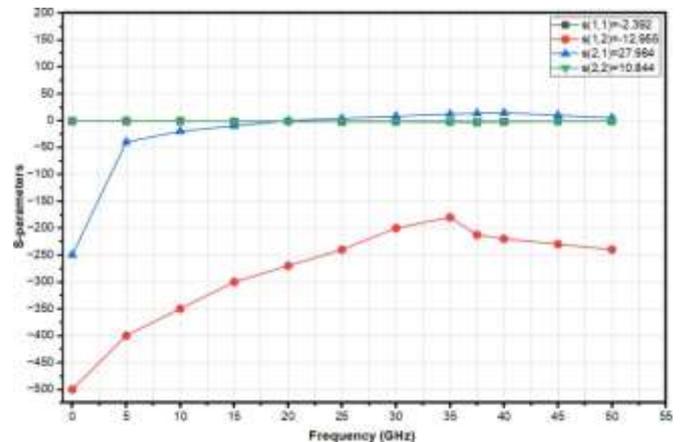

Fig. 3. **S-parameters**

The graph shows how the device behaves when the frequency increases from 0 to 50 GHz. The blue line (S21) is high, which means the device gives a strong output signal and works well as an amplifier. The red line (S12) is very low, meaning almost no signal goes backward, so the device

has very good isolation. The black and green lines (S11 and S22) stay near zero, which means the input and output are not matched well. In simple words, the device gives good amplification, very little reverse signal, but the input and output sides need improvement to work more efficiently.
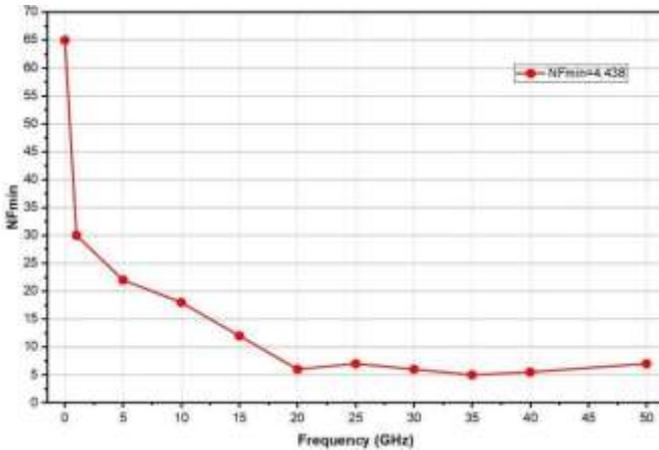

Fig. 4. **Noise Figure**

The graph shows how the minimum noise figure (NFmin) changes with frequency from 0 to 50 GHz. At low frequencies, the noise figure is very high, around 65 dB, but it drops quickly as the frequency increases. Between 20 GHz and 40 GHz, the noise figure becomes very low (around 5–7 dB) and stays almost constant. Overall, the device performs with high noise at low frequencies and much better, low-noise performance at higher frequencies.

CONCLUSION

In this project, we designed an RF amplifier using a GaN HEMT transistor and made sure it gives clear, strong, and stable output. The circuit was adjusted with proper matching and biasing so that the signal can be amplified without noise or distortion. The results show that the amplifier works well for high-frequency communication. Overall, this design proves that GaN HEMT devices are a good choice for building fast and efficient RF amplifiers.

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