Designing Half-Adder with CMOS Technology using Artificial Neural Network with Verilog Implementation

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Abstract: In this study we want to design a Half-Adder with the help of Artificial Neural Network and design will be made by Complementary metal oxide semiconductor(CMOS).When we design any COMS circuit always we keep in mind that should be in minimum at cost .In this study we have used multi layer ANN to design the circuit. In our study neurons are treated like transistors and weights are used to adjust the value; like negative value as an inverter.

Keywords: Half Adder, Complementary Metal Oxide Semiconductor, Artificial Neural Network, Verilog HDL

Introduction :

Modern technologies are quite busy to design the circuitry which is very intelligent. It is possible to design an in intelligent computing device like Half - Adder with the help of ANN. In the field off ANN .Artificial Intelligence can be used in the area of transportation, banking, agriculture, hand writing reorganization, speech reorganization and other many fields. To develop a Neural system in the area of digital circuits make hardware simple[1].Machine simulation is now very much important topic for the researchers. Machine simulation is now applicable in various sector of society like bank, post office, publishing house, libraries etc.[2].Implementing circuit in VLSI Design is very useful because it causes low power consumption and less program code for software[6].

Design of AND Gate: In our research we are designing an AND GATE in CMOS. To design an AND gate in CMOS circuit we need eight transistors. First four transistor are pull up and pull down transistors .Pull up transistors are basically Pchannel metal–oxide–semiconductor(PMOS) and pull down transistor are N-type metal-oxide-semiconductor (NMOS). NMOS will be in serial and PMOS will be in parallel . NMOS is connected to the drain voltage Vss and PMOS is connected source voltage Vdd.

A digital logic device known as a half adder can add two binary values, each containing one bit in binary. Its two inputs are A and B, and its two outputs are SUM and CARRY. The least significant bit (LSB) of the result is the SUM output, whereas the most significant bit (MSB) is the CARRY output, which indicates if there was a carry-over from the addition of the two inputs. The half adder, for instance, can be constructed using XOR and AND gates.Okay, let's get into the details of how the half-adder circuit works:A basic building block for circuits with more complex adder functionalities, such as full adders and multiple-bit adders, is the half adder. It sums the binary values of A and B, two single-bit inputs.To add two numbers, a combinational circuit known as a half adder is utilized.The half adder's truth table:The half adder is the most basic adder circuit. The half adder, a type of combinational arithmetic circuit, adds two numbers and produces a carry bit (c) as well as a sum bit (s). To add two bits, a combination circuit called a half adder is utilized. Genend and addend bits are the input variables, and sum and carry bits are the output variables. A and B are the input bits.The X-OR of the two input bits, A and B, in this instance, is sum bit (s). It is evident from a half adder's operation that one AND gate and one X-OR gate must be constructed.

INPUTS		OUTPUTS	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

For the Half adder Karnaugh –map becomes:

For sum:

	1
1	

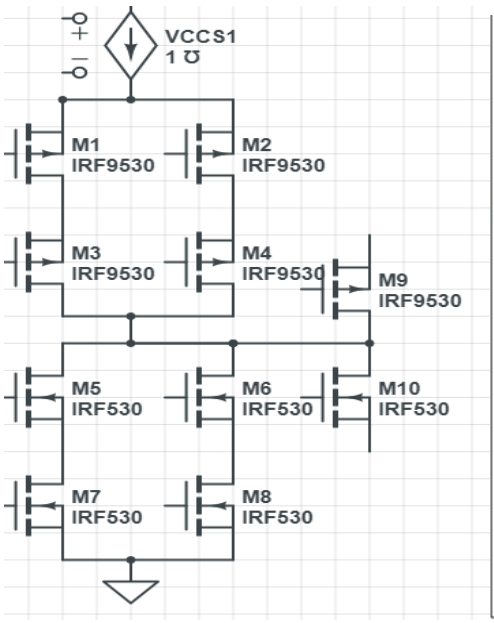
So the equation for sum Sum=A EXOR B----------(1)

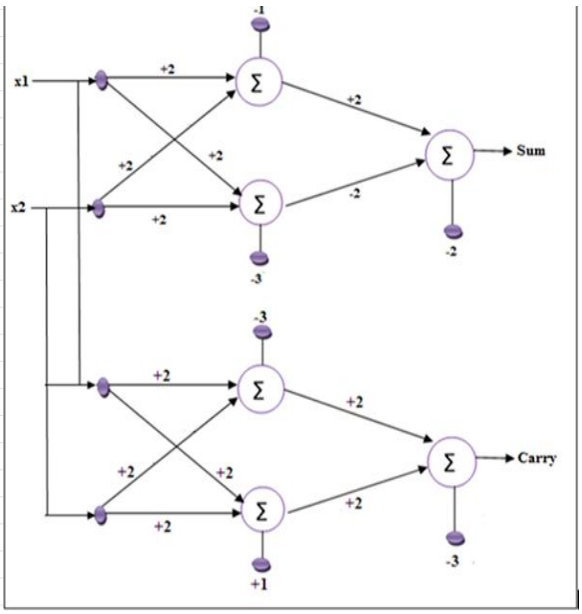
For carry:

	1

So the equation becomes:

Carry = A&B----------(2)





Now the CMOS circuit design for half adder

The Neural Network design of Half Adder with adding weight

For the transistors equstions are…

T1=X1*-2+x2*(-2)……..(3)

T2=X1*-2+x2*(-2)……..(4)

T3=X1*-2+x2*(-2)……..(5)

T4=X1*-2+x2*(-2)……..(6)

T5=T1*(-2)+T2*(-2)……..(7)

T6=T3*(-2)+T4*(-2)……(8)

Mythology to design Artificial Neural Network for the CMOS Half Adder Gate Circuit :

There are two inputs in Half Adder gate that is x1 and x2.Depending on truth table 0 will be inserted -1 and 1 is will be set as 1.Source voltage Vdd is always 1 and drain voltage Vss is always 0.In our study we are working with Artificial Neural Network so we have to adjust weights. Weights are can be set as 1 and -1.

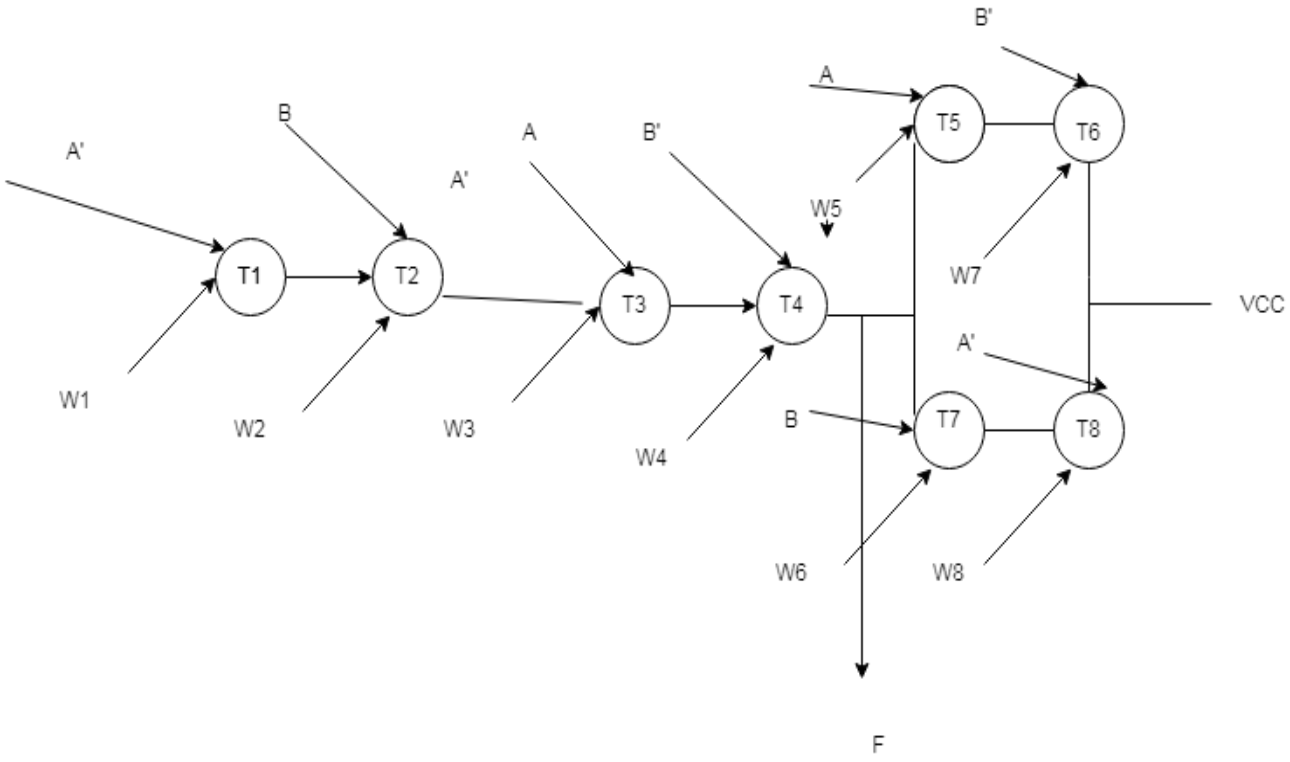


Figure: Half Adder Sum part ANN Design

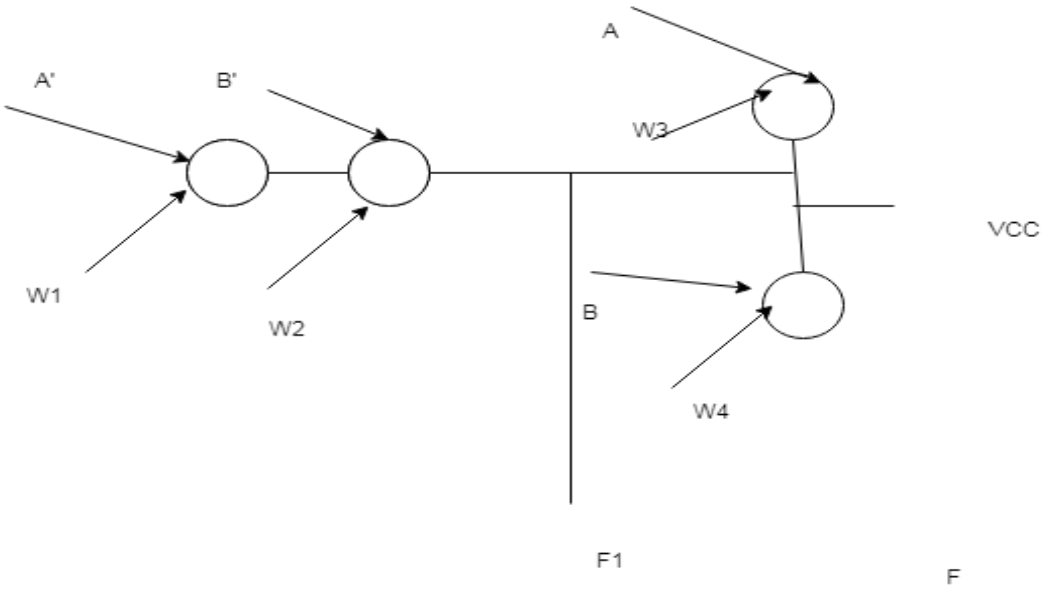
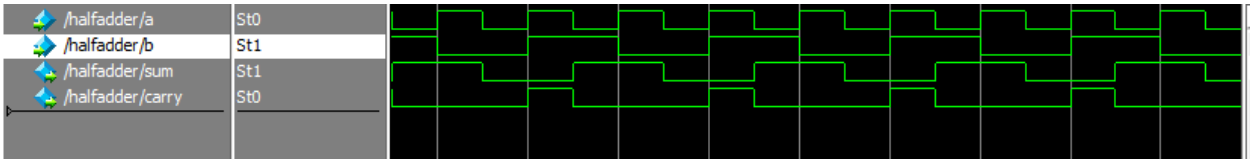


Figure:Carry Part Design for ANN

Result and Analysis:

Verilog Code's output for Half Adder:



Applying Sigmoid and Relu Function in R Programming Language :

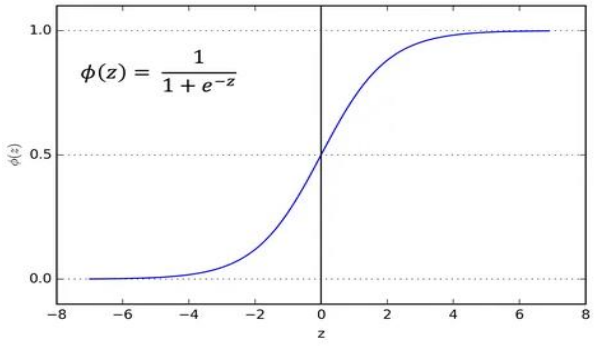
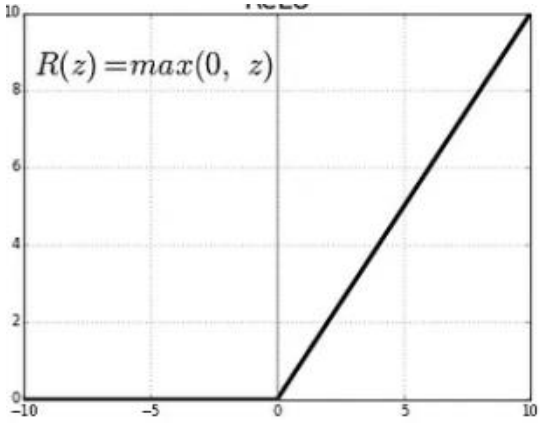


Fig: Sigmoid Function



Conclusion:

Now a days it is a trend to implement the Artificial Neural Network by COMS circuits cause it will be hardware controlled. We will get a circuit which can think. So if we can implement ANN in CMOS circuit then total circuit will become more intelligent comparison to present digital and analog circuits.

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