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Digital Twin Enabled Smart E Fuse with Battery SOC and Harness Health Monitoring

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Abstract - This paper proposes a four-channel smart electronic fuse box for 12 V auxiliary loads with battery state-of-charge and wiring-harness condition monitoring. Each branch uses a power MOSFET as a resettable switching and protection element. Two branches supply LED loads and two branches supply DC motors. Current and MOSFET temperature are measured for every branch. Bus sensing supports battery state-of-charge estimation, while paired voltage measurements across a controlled connector test section quantify harness voltage drop. An ESP32 performs acquisition, calibration, local overcurrent and overtemperature protection, gate control, diagnostics, and UART transmission. When state of charge falls below calibrated limits, the controller sheds selected high-power motor loads while retaining essential low-power loads. A PC application maintains synchronized digital-twin objects, records time-series data, displays all measured parameters, classifies harness condition from good to critical, and evaluates an AI anomaly score. The architecture keeps deterministic protection on the embedded controller so loss of the PC or serial connection cannot prevent a trip. The proposed validation covers normal loading, LED overload, motor startup, motor stall, progressive heating, sensor faults, and communication interruption. The design provides a repeatable laboratory platform for selective protection and predictive condition-monitoring research.

Key Words: electronic fuse, MOSFET protection, ESP32, battery state of charge, load shedding, harness health, voltage-drop monitoring, digital twin, anomaly detection

1. INTRODUCTION

Low-voltage electrical distribution uses fuses to interrupt excessive current, but a conventional fuse provides little information before it opens and must be replaced after operation. An electronic fuse replaces the melting element with a controlled semiconductor switch and can combine branch isolation with sensing, diagnostics, and reset logic. This capability is useful in auxiliary power systems containing lighting, motors, and other loads whose normal current profiles differ.

The proposed prototype contains four independent 12 V channels. Channels 1 and 2 drive LED loads, whereas Channels 3 and 4 drive DC motors. Every channel measures branch current and the temperature near its MOSFET. Battery voltage and current support state-of-charge estimation. Additional voltage-sensing points on the two sides of a connector test section measure the small drop produced by wiring and contact resistance. The test section uses switch-selected series resistors to reproduce increasing connector degradation without relying on uncontrolled corrosion.

The system divides responsibility between an ESP32 and a PC. The ESP32 executes the time-critical protection path and transmits validated measurement frames through UART. The PC stores the data and updates a digital twin of each protected branch. This split allows computationally richer visualization and prediction without making the immediate trip action dependent on the PC.

The main contribution is a compact experimental architecture that unifies four-channel MOSFET protection, battery-aware load shedding, harness voltage-drop diagnostics, embedded acquisition, a defined UART interface, branch-level digital twins, and AI-assisted condition assessment. The work is presented as a laboratory design and validation framework rather than an automotive-qualified controller.

2. RELATED WORK

Power MOSFETs support fast switching and low conduction loss when the selected device has adequate drain voltage, current, safe-operating-area, gate, and thermal margins. A practical e-fuse also needs a gate-control path that establishes a default-off state, limits switching transients, and turns the MOSFET off rapidly during a fault. Motor branches require special attention because startup and stall currents can be substantially higher than the steady operating current.

The ESP32 family provides timers, serial interfaces, and general-purpose input and output resources suitable for coordinated acquisition and control [1]. The original ESP32 also includes multiple ADC channels, but an external ADC can improve repeatability and avoid constraints associated with multiplexing and on-chip ADC behavior. The ADS1115 is a four-channel, 16-bit, I2C-compatible converter with a programmable gain stage and a maximum data rate of 860 samples per second [2]. Two devices can therefore acquire four current and four temperature signals.

Digital-twin research links a physical asset with a computational representation that is updated from measured data. Tao et al. describe data-driven synchronization across product design, manufacturing, and service [3]. In this prototype, the twin is intentionally smaller: four branch objects hold measured, estimated, commanded, diagnostic, and predicted state. For anomaly analysis, Isolation Forest is attractive as a baseline because it isolates unusual observations without requiring a complete set of labelled fault examples [4].

3. PROPOSED SYSTEM ARCHITECTURE

The architecture contains a protected 12 V battery input, bus-voltage and battery-current sensing, four parallel output branches, a controllable harness-degradation test section, an ESP32 controller, a UART interface, and a PC application. Each branch includes a MOSFET power switch, gate-control

components, a current-sensing element, a temperature sensor positioned close to the MOSFET, transient suppression suited to the load, and a connector for the LED or motor. Two voltage-sensing nodes placed upstream and downstream of the harness test section provide the differential voltage used for contact-resistance assessment.

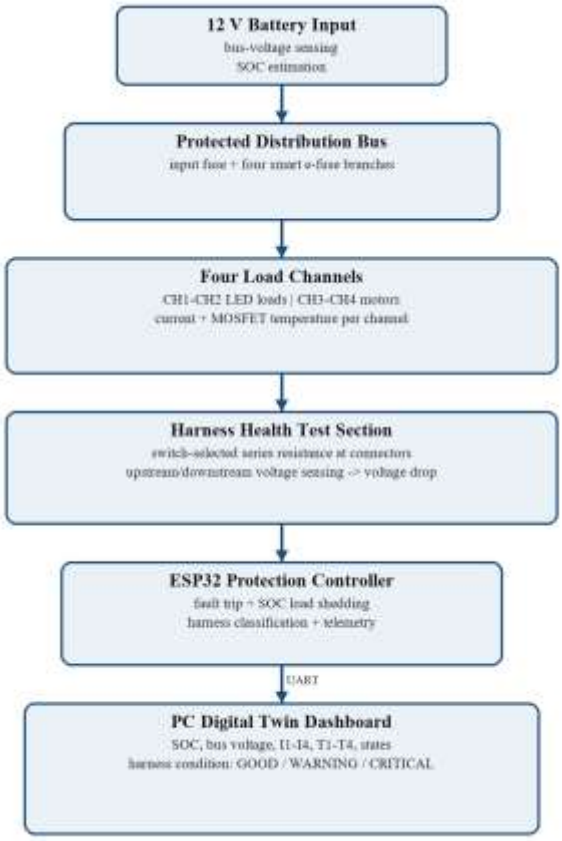


Fig. 1: Block diagram with SOC estimation, load shedding, and harness-health monitoring

Table -1: Four channel allocation

Channel	Load and monitored state
CH1	12 V LED 1; current I1; MOSFET temperature T1
CH2	12 V LED 2; current I2; MOSFET temperature T2
CH3	12 V DC motor 1; I3 and T3; high-power load-shedding priority 1
CH4	12 V DC motor 2; I4 and T4; high-power load-shedding priority 2

The embedded and PC layers exchange two classes of information. Telemetry frames travel from the ESP32 to the PC and contain calibrated branch values, battery voltage, estimated SOC, harness voltage drop, harness condition, load-shedding state, fault reason, and diagnostic flags. Commands from the PC request enable, disable, reset, identification, or configuration operations. The ESP32 validates every command and applies local interlocks before changing a gate output.

4. HARDWARE DESIGN

The MOSFET for each channel is selected from the maximum supply voltage, expected continuous load current, motor stall current, transient stress, on-state resistance, safe-operating-area curve, package thermal resistance, and available heat sinking. The conduction-loss estimate uses Pcond = I squared multiplied by RDS(on). This estimate establishes a first thermal check, while the final design must use the resistance at the expected junction temperature and the actual duty cycle.

A high-side arrangement maintains the load ground near system ground but requires a suitable driver for an N-channel MOSFET. A low-side arrangement is simpler but can disturb ground-referenced loads and measurements. The selected topology must therefore be stated on the schematic and tested with the actual LED modules and motors. A physical input fuse remains necessary to protect wiring and contain faults that bypass firmware control.

Each current channel needs a range that covers normal operation and the controlled fault test. Hall-effect sensing offers galvanic separation and low insertion loss, while a shunt and amplifier can provide higher precision at the cost of dissipation and common-mode design effort. The temperature sensor may be an NTC thermistor or a digital sensor. An NTC attached to the MOSFET tab or heat spreader gives a compact relative thermal indicator, but calibration and thermal lag must be considered.

Battery SOC may be estimated by coulomb counting from battery current and corrected using rested open-circuit voltage [6]. Coulomb counting requires a known usable capacity, current-sensor offset calibration, elapsed-time integration, and bounded correction because offset error accumulates. For a short laboratory demonstration, an explicitly labelled voltage-based SOC approximation may be used, but the thresholds must be calibrated for the selected battery chemistry and must not be presented as a chemistry-independent value.

Harness degradation is simulated with switch-selected low-value power resistors in series with a representative connector and load path. Separate voltage sensors measure the potentials before and after this section. The controller calculates Vdrop = Vupstream - Vdownstream and, only when current is high enough for a reliable estimate, calculates equivalent resistance Rh = Vdrop divided by I. Resistor ratings, switching devices, wiring, and test duration must be selected for the expected I squared R dissipation. This arrangement represents increased contact resistance caused by loose, oxidized, or corroded connections, which can raise electrical contact resistance [7].

The motor outputs require a flyback or recirculation path and may also require a transient-voltage suppressor or snubber. Bulk capacitance should not defeat the intended branch isolation. High-current traces and wires must use adequate cross-section, short return paths, reliable terminals, and strain relief. The ESP32 supply requires protected conversion from 12 V, local decoupling, and a grounding plan that separates switching currents from sensitive measurement returns.

5. EMBEDDED CONTROL AND PROTECTION

At startup, firmware configures all gate outputs in the off state, initializes the ADC and UART, loads calibration coefficients and battery capacity, verifies sensor plausibility, and announces its revision. A periodic task samples branch currents and temperatures, battery voltage and current, and harness sensing nodes. Median rejection can remove isolated spikes, while a low-pass filter reduces noise for display and prediction. The protection path retains access to unfiltered or lightly filtered peaks so smoothing cannot conceal a short fault.

Each branch follows an explicit state machine: OFF, SELF TEST, ACTIVE, WARNING, TRIPPED, COOLDOWN, and RESET PENDING. The current logic may use an

instantaneous severe-fault threshold and a lower threshold with a persistence timer. Motor channels include a bounded startup window based on measured inrush. LED channels do not need the same allowance. Temperature logic uses warning and trip limits with hysteresis and cooldown. Implausible sensor values force a diagnostic state and a conservative output policy.

The embedded controller records the first trip cause, peak current, temperature, elapsed time, and sequence number. If current and temperature faults occur together, the firmware preserves both flags while prioritizing rapid gate turn-off. A hardware watchdog returns outputs to a defined safe state if the control task stops executing.

Battery management uses configurable SOC bands with hysteresis. In NORMAL, all authorized channels may operate. In LOW SOC, the controller disconnects the first-priority motor and blocks its restart. In CRITICAL SOC, both motor channels are disconnected while essential LED channels remain available unless their own protection limits are exceeded. Exact SOC limits are calibration parameters chosen for the battery chemistry, capacity, and demonstration objective; they are not hard-coded universal values.

Harness condition is classified from filtered voltage drop and equivalent resistance as GOOD, WARNING, POOR, or CRITICAL. Classification is enabled only above a minimum diagnostic current, uses persistence timers and hysteresis, and distinguishes an open load from a resistive connection. A CRITICAL condition can inhibit or isolate the affected high-current path according to the configured safety policy.

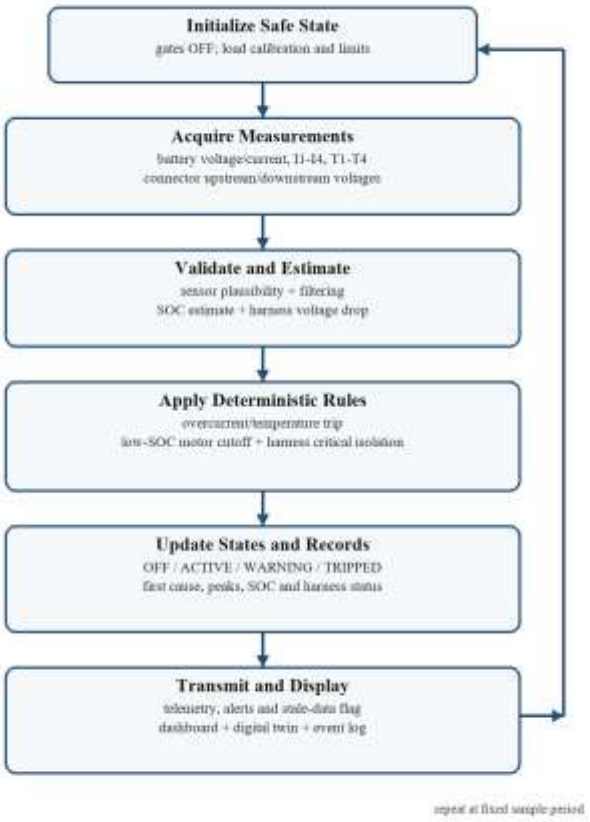


Fig. 2: Updated embedded measurement, protection, load-shedding, and reporting flow

6. UART DATA INTERFACE

The serial protocol uses a fixed start marker followed by a version, message type, sequence number, payload length, sample timestamp, measurement payload, state bytes, fault flags, and a cyclic redundancy check. Integer scaling avoids dependence on floating-point byte representation. A receiver that detects an invalid length or checksum discards bytes until it finds the next valid start marker.

Table -2: Proposed telemetry frame

Field	Purpose
Start and version	Frame synchronization and format identification
Sequence and time	Loss detection and sample ordering
I1 to I4	Scaled calibrated branch currents
T1 to T4	Scaled MOSFET temperatures
VBAT, IBAT, SOC	Battery measurements and state-of-charge estimate
VUP, VDOWN, VDROP	Harness sensing nodes and calculated voltage drop
Harness and shed state	Condition class and battery-based load availability
State and fault	Four channel state and diagnostic information
CRC	Payload integrity check

The ESP32 continues protection if UART communication stops. The PC uses a timeout to mark its displayed state as stale and blocks commands that depend on fresh data. This behavior prevents a frozen dashboard value from appearing to be a live measurement.

7. DIGITAL TWIN AND AI METHOD

The PC application creates one virtual object per physical branch and shared objects for the battery and harness. Each branch object contains load type, measured current, measured temperature, commanded state, actual state, protection thresholds, load-shedding reason, latest fault reason, communication quality, rolling features, anomaly score, and risk category. The battery object contains voltage, current, estimated SOC, SOC band, and active shedding policy. The harness object contains upstream voltage, downstream voltage, voltage drop, diagnostic current, estimated resistance, and the GOOD, WARNING, POOR, or CRITICAL condition.

The dashboard displays battery voltage, battery current, SOC percentage and band, I1-I4, T1-T4, all channel states, motor load-shedding status, harness voltage drop and estimated resistance, harness condition, communication freshness, active alarms, anomaly score, and the most recent event. Color is supplemented with text labels so GOOD through CRITICAL states remain unambiguous. Trend plots allow the user to correlate SOC, load current, connector drop, and temperature over time.

Feature extraction operates on load-specific time windows. Candidate features include mean current, peak current, standard deviation, current slope, temperature, temperature slope, SOC slope, time above warning current, event count, startup duration, harness voltage drop, estimated contact resistance, and the difference between measured and first-order thermal estimates. LED and motor channels require separate baselines because their normal signatures differ.

The initial model should combine deterministic engineering limits with a data-driven anomaly score. Isolation Forest can learn the distribution of normal windows and identify uncommon combinations [4]. After the test bench produces sufficient labelled examples, a supervised model such as Random Forest may classify overload, stall, heating, and sensor-fault conditions [5]. Training and test data must be separated by complete experimental runs to reduce leakage between adjacent time windows.

The AI model cannot command an unsafe continuation or override a deterministic trip. Its output supports warning, prioritization, and maintenance analysis. Model evaluation should report precision, recall, false-alarm rate, confusion matrix, and warning lead time. Threshold selection must reflect the higher cost of missed thermal or stall faults while controlling nuisance alerts.

8. EXPERIMENTAL VALIDATION

The test setup uses a current-limited 12 V battery or battery emulator, an independent input fuse, emergency disconnection, four protected outputs, two rated LED loads, two rated DC motors, reference current and voltage measurements, a temperature reference, and a switch-selected series-resistor harness emulator. Tests begin at low energy and use supervised fault insertion. The enclosure and conductors must contain the maximum credible test fault.

Table -3: Validation matrix

Test	Required evidence
Normal LEDs	Stable current, acceptable temperature, no nuisance trip
LED overload	Selective trip and retained fault record
Motor start	Inrush captured without false trip
Motor stall	Prompt trip, peak record, and correct channel identity
Progressive heat	Warning before thermal trip and controlled cooldown
Sensor fault	Diagnostic flag and conservative output state
UART loss	Local protection continues; PC state becomes stale
SOC thresholds	Correct SOC band, hysteresis, motor shedding order, and restart blocking
Harness resistance steps	Measured drop tracks inserted resistance; condition advances from GOOD to CRITICAL
Low diagnostic current	Harness classification suppressed or marked unavailable

Calibration records the zero-current offset and gain of each current channel at several known points. Temperature calibration compares each mounted sensor with a reference near ambient and at a safe elevated temperature. Voltage channels are calibrated at multiple points with a reference meter. SOC validation compares accumulated ampere-hours and voltage-based correction against controlled charge and discharge steps. Harness validation applies known series-resistance values and compares calculated voltage drop and resistance with reference measurements. Every calibration coefficient is stored with channel identity, date, and revision.

Protection timing should be measured from the physical onset of the fault to gate turn-off and separately to PC notification. This separation distinguishes local safety response from reporting latency. Four-channel concurrency testing operates multiple loads at once and confirms that one trip does not corrupt the identity or measurements of the remaining branches.

9. RESULTS AND DISCUSSION

The design establishes measurable acceptance criteria but does not claim final numerical performance before hardware testing. A successful LED test should show steady current and moderate MOSFET temperature, followed by selective disconnection when the imposed current exceeds the approved threshold. A successful motor-start test should capture inrush without nuisance tripping, whereas a stall test should exceed the load-specific persistence rule and open only the affected branch.

Thermal validation should show a rising temperature trend under controlled heating, a warning below the trip threshold, a trip at the approved limit, and restart only after cooldown and hysteresis conditions are satisfied. Sensor-disconnect tests should generate a diagnostic fault rather than a plausible but incorrect measurement. During UART interruption, the ESP32 should continue protection and the PC should clearly show stale data.

SOC validation should demonstrate stable band transitions, the specified motor-shedding order, hysteresis that prevents rapid cycling near a threshold, and controlled restoration after SOC recovery. Harness tests should show increasing

measured drop as series resistance is added, correct condition changes from GOOD toward CRITICAL, and no resistance classification when diagnostic current is too small. The dashboard should agree with reference instruments and preserve the event sequence.

The predictive model should be judged by its behavior across complete runs. An alarm that appears only after a deterministic trip has no useful warning lead time. Conversely, an early score that repeatedly alarms during normal motor startup creates nuisance alerts. The final model therefore requires load-specific features, calibrated probability or score thresholds, and documented failure cases. These results will determine whether the digital twin adds value beyond visualization and event logging.

10. SAFETY AND IMPLEMENTATION LIMITS

The prototype is not an automotive-qualified electronic control unit. Vehicle deployment would require automotive-grade switches and sensors, protected and possibly isolated communications, electromagnetic-compatibility testing, environmental qualification, endurance testing, cybersecurity controls, and functional-safety engineering consistent with the intended safety goal. The laboratory device must never be used as the sole protective element for a hazardous load.

SOC accuracy depends on battery chemistry, capacity, temperature, ageing, current-sensor offset, and the availability of rested-voltage correction. The demonstrator therefore treats SOC as an estimated control input and validates thresholds conservatively. Harness resistance must not be calculated near zero current, where sensor offset can dominate the result. The series-resistor emulator reproduces electrical resistance and heating effects but does not reproduce every mechanical or chemical effect of real corrosion.

11. CONCLUSION

This paper presented a four-channel smart e-fuse architecture that protects two LED loads and two DC motors with independent MOSFET switches. Current and MOSFET temperature are measured on every channel, battery measurements support SOC estimation and priority-based motor load shedding, and paired voltage measurements identify added harness resistance. The ESP32 performs deterministic protection and transfers structured data over UART, while the PC maintains synchronized branch, battery, and harness digital twins.

The principal design decision is to keep the trip, low-SOC shedding, and critical-harness response independent of communication and AI prediction. This makes the platform suitable for controlled experiments in selective protection, motor-stall detection, thermal monitoring, battery-aware energy management, connector degradation detection, serial data integrity, and predictive warning. The dashboard makes all parameters and the GOOD-to-CRITICAL harness condition visible, while the proposed validation matrix defines the evidence required before numerical performance claims are made.

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