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Distributed Arithmetic for FIR Filter Implementation on FPGA

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ABSTRACT: This Project describes the implementation of FIR filters on FPGA based on traditional method costs considerable hardware resources, which goes against the decrease of circuit scale and the increase of system speed. It is very well known that the FIR filter consists of Delay elements, Multipliers and Adders. Because of usage of Multipliers in our design gives rise to 2 demerits that are (I) Increase in Area and (II) Increase in the Delay which ultimately results in low performance (Less speed). A new design and implementation of FIR filters using Distributed Arithmetic is provided in this project to solve this problem. Distributed Arithmetic structure is used to increase the resource usage while pipeline structure is also used to increase the system speed. In addition, the divided LUT method is also used to decrease the required memory units. The simulation results indicate that FIR filters using Distributed Arithmetic can work stable with high speed and can save almost 50 percent hardware recourses to decrease the circuit scale, and can be applied to a variety of areas for its great flexibility and high reliability.

Keywords: FIR Filter, FPGA, Look-Up Table, Multipliers and Adders, Distributed Arithmetic.

I. INTRODUCTION

A typical digital implementation will require K multiply-and-accumulate (MAC) operations, which are expensive to compute in hardware due to logic complexity, area usage, and throughput. Alternatively, the MAC operations may be replaced by a series of look-up-table (LUT) accesses and summations. Such an implementation of the filter, known as distributed arithmetic (DA), achieves higher throughput and lower logic complexity at the cost of increased memory usage. Recent advances in memory design technology have resulted in shrinking memory sizes, making

this trade-off an attractive option. Many DSP applications require linear filters that can adapt to changes in the input signals.

Digital Signal Processing (DSP) has been increasing in popularity due to the declining cost of general purpose computers and Application Specific hardware. Since many telephony and data communications applications have been moving to digital, the need for digital filtering methods continues to grow. Along with the advancement in Very Large Scale Integration (VLSI) technology and the DSP has become increasingly popular over the years, the high speed realization of FIR digital filters with less power consumption has become much more demanding. Since the complexity of implementation grows with the filter order and the precision of computation, these filters with desired level of accuracy is a challenging task. Several attempts have, therefore, been made to develop dedicated and reconfigurable architectures for realization of FIR filters in Application Specific Integrated Circuits (ASIC) and Field-Programmable Gate Arrays (FPGA) platforms.

II. OBJECTIVE

The implementation of FIR filters on FPGA based on traditional method costs considerable hardware resources, which goes against the decrease of circuit scale and the increase of system speed.

LITERATURE SURVEY

1. **B.N Mohan Kumar, H.G Rangaraju, "Array Multiplier and CIA based FIR Filter for DSP applications,"** ***2021 Special Issue of First International Conference on Engineering, Science, and Technology (ICEST),*** **2021, pp. 52-59, doi: 10.47392/irjash.2021.020** - B.N Mohan Kumar [1] For adding the output of the PE in this study, the Carry Increment Adder (CIA) in the accumulator is used. The AM-CIA-FIR filter is the name of the suggested approach. According to the experiment's findings, the AM-CIA-FIR filter design uses 14.01% less FPGA resources than the PSA-FIR filter.

2. **Pranay Anand Tiwari & Dr. Rajani K. A. Rao, A. Kumar and N. Purohit, "Efficient Implementation for 3-Parallel Linear-Phase FIR Digital Odd Length Filters,"** ***2020 IEEE 4th Conference on Information & Communication Technology (CICT),*** **2020, pp. 1-6, doi: 10.1109/CICT51604.2020.9312116. - K. Anjali Rao. [2]** They proposed 3-parallel finite impulse response (FIR) structures in this study by using fast FIR algorithms and polyphase coefficient symmetry (FFAs). The

proposed FFA-based structure performs better than similar existing structures when compared to the quantity of multipliers needed.

3. **R. Vinay, T. S. V. S. Vijayakumar, L. M. Saini and B. Singh, "Power efficient FIR filter Architecture using Distributed Arithmetic Algorithm,"** ***2020 First IEEE International Conference on Measurement, Instrumentation, Control and Automation (ICMICA),*** **2020, pp. 1-4, doi: 10.1109/ICMICA48462.2020.9242720.-**
Ratnala Vinay. [3] In order to identify the most energy-effective system, two MAC ways are—the Multiple Constant Multiplication (MCM) system and the Distributed Arithmetic (DA) system—are computed in this study utilizing simulation and synthesis tools. They discover that DA is a memory- and power-effective system that uses fewer memory units, reducing the complexity of the filter's design.

III. MAC FIR FILTER ARCHITECTURE

FIR filter have variety of alternative form of implementation those are listed below.

1) Direct form structure
2) Cascade form
3) Frequency sampling
5) Lattice structure
5) Linear phase FIR filter

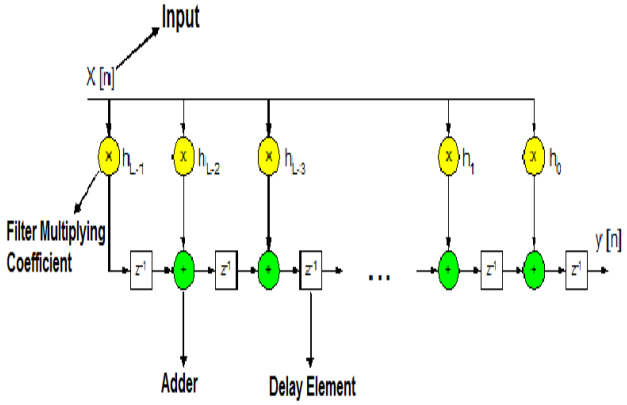


Fig FIR filter implementation with MAC architecture

Multiply-Accumulate (MAC) - In a FIR context, a "MAC" is the operation of multiplying a coefficient by the corresponding delayed data sample and accumulating the result. FIRs usually require one MAC per tap. Most DSP microprocessors implement the MAC operation in a single instruction cycle.

IMPLEMENTATION OF BASIC LUT

Look-up table is a storage device. It stores the filter coefficient values. The divided LUT method is also used to decrease the required memory units. Pipeline structure is also used to increase the system speed. As we are supposed to design 31-order filter, with the increase of filter order, the scale of LUT will increase dramatically, which will cost more time to look up the table and more

memory to store the values. Therefore, we can divide the LUT unit into four small LUT units to solve this problem. Coefficient values of small LUT are given.

$b_3b_2b_1b_0$	Data
0000	0
0001	h[0]
0010	h[1]
0011	h[0] + h[1]
0100	h[2]
0101	h[0] + h[2]
0110	h[1] + h[2]
0111	h[0] + h[1] + h[2]
1000	h[3]
1001	h[0] + h[3]
1010	h[1] + h[3]
1011	h[0] + h[1] + h[3]
1100	h[2] + h[3]
1101	h[0] + h[2] + h[3]
1110	h[1] + h[2] + h[3]
1111	h[0] + h[1] + h[2] + h[3]

FIR FILTER IMPLIMANTAION USING DA WITH BASIC LUT STRUCTURE

Distributed Arithmetic is one of the most well-known methods of implementing FIR filters. The DA solves the computation of the inner product equation when the coefficients are pre knowledge, as happens in FIR filters. An FIR filter of length K is described as:

$$y[n] = \sum_{k=0}^{k-1} h[k]x[n-k]$$

Where h[k] is the filter coefficient and x[k] is the input data. For the convenience of analysis, x'[k] =x [n - k] is used for modifying the equation (1) and we have:

$$y = \sum_{k=0}^{k-1} h[k].x'[k]$$

Then we use B-bit two's complement binary numbers to represent the input data:

$$X'[k] = -2^{B}.x_B[k] + \sum_{b=0}^{B-1} x_b[k].2^b$$

Where $X_b[k]$ denoted the b^{th} of $X_b[k]$, $X_b[k] \in \{0, 1\}$.

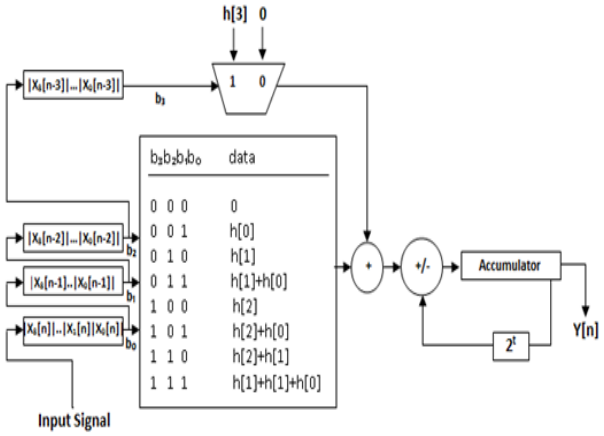


Fig- Proposed DA architecture for a 5-tap filter

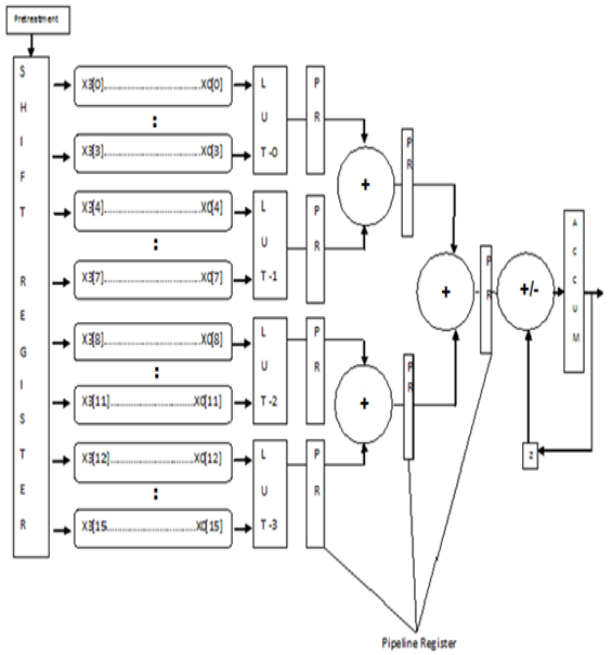
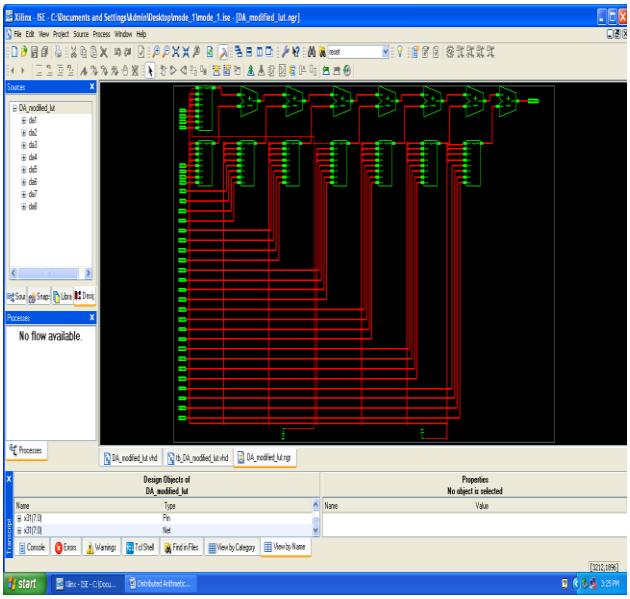
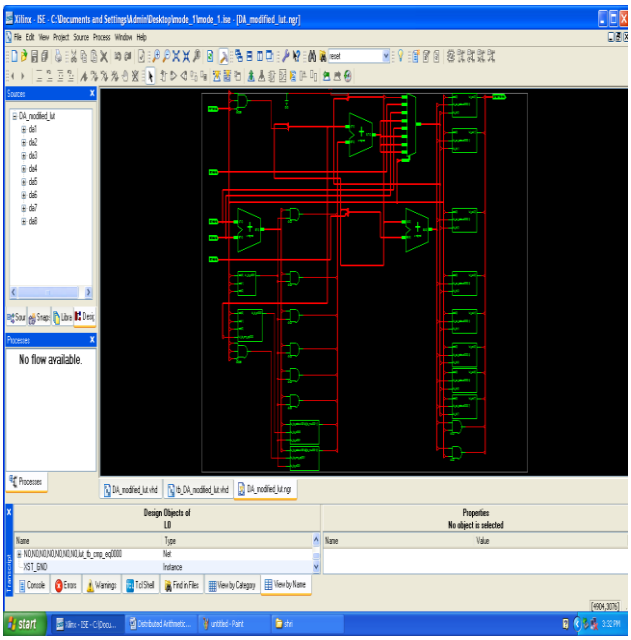


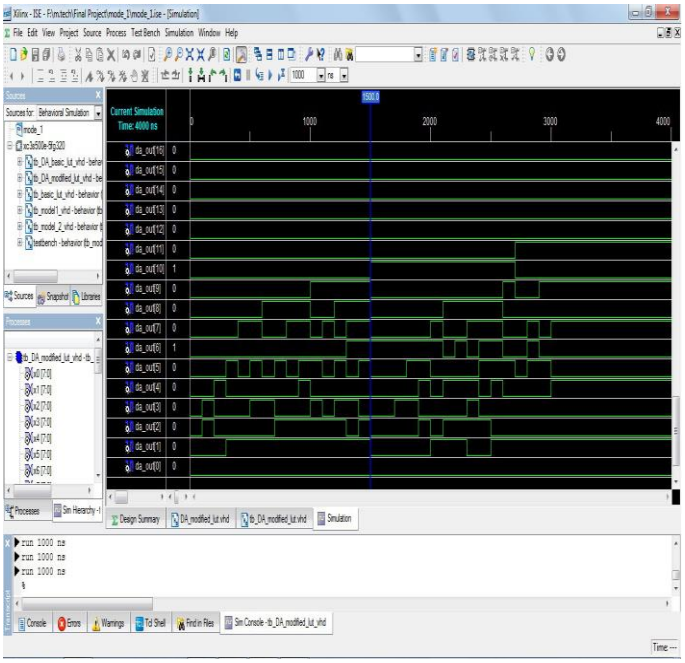
Fig: Structure of 15-Tab FIR filter based on Distributed Arithmetic

IV. IMPLEMENTATION & SYNTHESIS REPORT





These are the Design Summary of Basic LUT .This is show the memory allocation of the Basic LUT.



After all implementation and simulation result of the basic LUT and modified LUT result .according to print diagram 7.8 and 7.9 these are the diagram of Basic LUT and modified LUT . these wave from result are same that mean basic LUT work with large memory space and modified LUT work with small memory space so that wave result of both LUTs are same.

After that according to the design summary result, we take print diagram 7.10 and 7.11. These are the diagrams of Basic LUT and modified LUT.

This project reports the proposed DA architectures for high-order filter. The architectures reduce the memory usage by half at every iteration of LUT reduction at the cost of the limited decrease of the system frequency. We also divide the high-order filters into several groups of small filters; hence we can reduce the LUT size also. As to get the high speed implementation of FIR filters, a full-parallel version of the DA architecture is adopted. We have successfully implemented a high-efficient 31-tap full-parallel DA filter, using both an original DA architecture and a modified DA architecture on a 5VLX50FF668 FPGA device.

V. REFERENCES

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