Enhanced Noise Shaping ADC With Single Fan out Gated Delay Cells

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***Abstract*—In modern high-speed data acquisition systems, achieving a high Signal-to-Noise Ratio (SNR) and low Total Har- monic Distortion (THD) is critical. This paper presents a novel time-domain reconfigurable second-order noise-shaping Analog- to-Digital Converter (ADC) architecture that incorporates single fan-out gated delay cells to enhance performance. The proposed ADC leverages time-domain techniques to achieve superior noise shaping characteristics while maintaining flexibility in its con- figuration. The key innovation in our design is the use of gated delay cells with a single fan-out, which enables precise control over timing and reduces power consumption. These delay cells are integral to the ADC's ability to reconfigure its operation based on the specific requirements of different signal conditions. This adaptability is crucial for optimizing performance across various applications, from low-power sensor interfaces to high- speed communication systems.**

Simulation results demonstrate that the ADC achieves sig- nificant improvements in SNR and THD compared to con- ventional architectures. The design also exhibits robustness to variations in operating conditions and process variations, making it suitable for integration into diverse electronic systems. The proposed architecture represents a substantial advancement in ADC technology, combining reconfigurability with effective noise shaping to meet the demanding requirements of modern high- performance applications.

***Index Terms*—Keywords—Analog-to-Digital Converter (ADC), Noise Shaping, Single Fan-Out Gated Delay Cells, Signal In- tegrity, Timing Jitter, Sigma-Delta Modulator.**

I. INTRODUCTION

Less power is used in the CMOS process because to its geometric scalability. However, in the interim, conventional analog circuit design is made more difficult by the reduced intrinsic gain of nanoscale transistors and signal swing at low power supply voltages. One example of this is the operational transconductance amplifier (OTA), which is widely used in analog-to-digital converters (ADCs).[1] Time-domain ADCs are becoming completely developed and appropriate for the dominant nanoscale CMOS technologies. They replace con- ventional analog blocks with digital-based blocks and process time signals. At ultralow supply, two inverter-based noise shaping ADCs are proposed by Catania et al. and Lv et al. A report describes the primarily digital implementation of a time-register based noise shaping time-to-digital converter (TDC).An electronic circuit known as a time-to-digital con- verter (TDC) quantizes

the interval of time between two events in order to express it as a digital code. TDCs have a long history of use in a variety of applications, including timing jitter and time-of-flight measurements. These days, there is a lot of research being done on high-resolution TDCs in order to construct energy-efficient analog-to-digital converters (ADCs) and all-digital phaselocked loops (ADPLLs). A TDC is utilized as a phase detector in ADPLL to find the phase difference between the reference and feedback clocks. TDC resolution generally limits the in-band noise of ADPLL . However, in terms of area reduction and power savings, high-resolution time-based ADCs have proven to be good substitutes for conventional voltage-based or current-based ADCs [2]. To mit- igate some of the A/D converter (ADC) design obstacles posed by digitally controlled deep submicrometer CMOS technologies, TM signal processing, also known as TMSP, is being researched as a possible substitute for traditional voltage signal processing. Despite the fact that TMSP is a relatively new concept, a number of works, including A/D conversion, have started to explore its possibilities in various applications . A continuous-time multibit sigma-delta converter that utilizes time encoding in the feedback path has been proposed more recently. This method could make the quantizer's needs sim- pler, particularly for low-voltage technologies.[3] In , a voltage comparator is constructed by first utilizing a voltage-controlled delay circuit to transform voltage into a time difference, which is then compared using a time-to-digital converter. In, the propagation delay of a chain of inverters is modulated

by an analog signal, which also modulates the period of an oscillator, which is subsequently translated into a digital representation. The technique described in implements a time- to-digital converter (TDC) by applying a time amplifier in conjunction with a voltage-tunable differential delay line.[3]

II.ARCHITECTURE

Advanced circuit design approaches are used in the architecture of an upgraded noise-shaping ADC with single fan-out gated delay cells to improve overall performance, resolution, and signal-to-noise ratio (SNR). The components, setup, and guiding principles of the suggested ADC architecture are described in detail in this section.

1. **Sigma-Delta Modulator (ΣΔ Modulator)**

In the enhanced noise-shaping ADC, the sigma-delta (ΣΔ) modulator is the central component. Because sigma-delta modulation has built-in noise shaping capabilities, it is especially well suited for high-resolution ADCs. By oversampling the input signal and utilizing a feedback loop, the ΣΔ modulator raises the frequency of quantization noise such that it may be filtered out.

2. Gated Delay Cells

This architecture is innovative because the ΣΔ modulator has single fan-out gated delay cells integrated into it. These delay cells improve noise shaping and reduce time jitter by adding precise, controlled delays to the signal stream.

Key Features:

• Single Fan-Out: Reduces load and preserves signal integrity by guaranteeing that every delay cell drives just one further step.

• Gating Mechanism: Regulates the delay cells' time to guarantee exact synchronization and minimize timing jitter.

Operations:

• Signal Propagation: As the input signal moves through the delay cells, a particular delay is introduced by each cell.

• Noise Shaping: The quantization noise is pushed to higher frequencies by being redistributed by the gated cells' delays.

• Timing Precision: For high-resolution ADC performance, the gating mechanism makes sure that delays are accurate and consistent.

3. **Feedback Loop:**

For noise shaping, the ΣΔ modulator's feedback loop is essential. The quantizer's input is continuously adjusted by varying the difference between the input signal and the feedback signal. This loop is improved by the addition of gated delay cells, which further improve noise suppression and timing accuracy.

Components:

Summing node: combines the feedback signal and the input signal.

Loop filter: manages the noise spectrum by forming the feedback signal.

Gated Delay Cells: Increase noise shaping by adding delays to the feedback path.

4. Digital Decimation Filter

The output of the ΣΔ modulator is an oversampled bitstream following modulation. By lowering the sample rate, a digital decimation filter transforms the high-frequency, high-resolution bitstream into a lower-frequency digital signal that may be processed further.

Components:

Comb filter: first step that lowers the sample rate and eliminates high-frequency noise.

FIR/IIR Filter: Additional steps that improve the signal quality and produce a higher-resolution digital output in the end

Operation:

Decimation: The filter reduces the sampling rate by averaging multiple samples, retaining high-resolution information

Noise Filtering: Out-of-band noise is eliminated by the filters, guaranteeing a pure digital signal.

Clock Generation and Distribution

For the ADC components to operate in unison, precise clock distribution and generation are necessary. The digital filters, the oΔ modulator, and the gated delay cells are all timed according to the clock signals.

Components:

Phase-Locked Loop(PLL): produces a high-frequency clock signal that is steady.

Clock Buffers: Assign the clock signal among the ADC's components, taking care to minimize jitter and skew.

Operation:

Clock Synchronization: makes ensuring that every part works together, which is essential for preserving the signal's integrity and the noise shaping's efficacy.

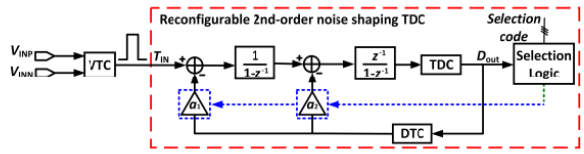


Fig. 1. Block diagram of the proposed ADC.

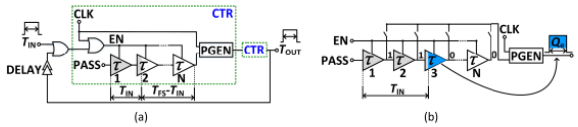


Fig. 2. Schematic of (a) time-domain integrator and (b) time quantization error extraction and the merged DTC.

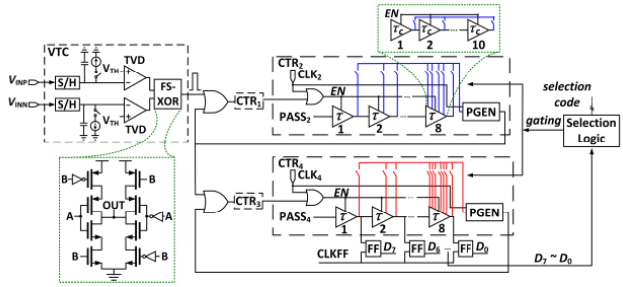


Fig. 3. Schematic of the second-order time-domain noise shaping ADC with reconfigurable poles.

III.LITERATURE REVIEW

An advanced kind of ADC that uses noise shaping tech- niques to boost performance, especially in terms of signal-to- noise ratio (SNR) and dynamic range, is called an enhanced noise shaping ADC (Analog-to-Digital Converter). This entails moving quantization noise to frequencies where it may be filtered out more readily by employing a variety of techniques to push it outside of the signal spectrum. This is a survey of the literature on enhanced noise shaping ADCs, with an emphasis on significant developments, methods, and patterns

A. FUNDEMENTALS OF NOISE SHAPING ADC

Fundamentals of Noise Shaping: By adjusting the quanti- zation noise spectrum, noise shaping is a technique that can increase an ADC's effective resolution. The main goal is to increase the signal-to-noise ratio (SNR) in the band of interest by driving quantization noise outside of it.

Delta-Sigma Modulation: This is one of the most widely used techniques for ADC noise shaping. With this method, the input signal is oversampled, and feedback is used to modify the quantization noise. The intended noise shaping properties are accomplished via the modulator's design of the signal transfer function (STF) and noise transfer function (NTF).

B. RECENT ADVANCES IN NOISE SHAPING ADC

Higher-Order Delta-Sigma Modulators: By raising the mod- ulator's order, higher-order delta-sigma modulators improve noise shaping. This has been the subject of recent research. While higher-order systems can be more complex and sensitive to non-idealities, they can provide better absorption of out-of- band noise.

Multi-Stage Noise Shaping (MASH): To enhance noise shaping and linearity, MASH (Multi-Stage Noise Shaping) ADCs have been created. These ADCs achieve low noise levels and good resolution by employing many steps of delta-sigma modulation. Several delta-sigma modulators are cascaded in this technique, each of which adds to the total noise shaping process.

Polyphase Filtering: To enhance performance, delta-sigma ADCs have been fitted with polyphase filtering techniques. Polyphase filters reduce the complexity of the analog filter design and enhance system performance by employing many filter channels.

C. APPLICATIONS AND TRENDS

Communication Systems: Widespread use of enhanced noise shaping ADCs is found in communication systems, especially in high resolution and dynamic range applications like digital signal processing and wireless communications.

Medical Imaging: Accurate imaging and diagnostic per- formance in medical imaging applications depend on high- resolution ADCs with efficient noise shaping. Enhancing the resolution and noise characteristics of ADCs used in imaging systems is the main goal of research.

Consumer Electronics: Improved noise shaping ADCs help produce higher-quality audio and video in consumer electron- ics. High-definition audio recording and video processing are two applications that benefit greatly from techniques that lower noise and increase signal fidelity.

IV.METHODOLOGY

The process of creating an improved noise shaping ADC with single fan-out gated delay cells requires a methodical ap- proach that combines rigorous validation procedures, accurate timing control, and sophisticated circuit design methodologies. The technique used to attain the intended performance gains in signal-to-noise ratio (SNR), resolution, and overall ADC efficiency is described in this section.

D. Design and Integration of Sigma-Delta Modulator

Objective: Create a modulator for sigma-delta () with im- proved noise shaping abilities. Steps: Architectural Design: Choose an appropriate arrangement and setting for the mod- ulator. Depending on the required noise shaping

and per- formance standards, first-order, second-order, or higher-order modulators are frequently selected. Component Specification: Describe the feedback digital-to-analog converters (DACs), quantizers, and integrators that make up the modulator's core. Loop Filter Design: Create a loop filter that efficiently shapes the noise spectrum. The noise shaping properties of the modulator are largely dependent on the transfer function of the loop filter.

E. *Incorporation of Single Fan-Out Gated Delay Cells*

Goal: Using single fan-out gated delay cells will improve noise shaping and timing accuracy. Actions: One way to mini- mize loading effects and maintain signal integrity is to design delay cells with single fan-out characteristics, which ensure that each delay cell drives just one subsequent stage. Gating Mechanism: Utilize a gating mechanism to regulate the delay cells' timing. This method lowers time jitter and guarantees exact synchronization. Integration with Modulator:Integrate the gated delay cells into the architecture of the modulator.To improve noise shaping, the delay cells are arranged in a certain way within the feedback loop.

F. *Feedback Loop Optimization*

Optimizing the feedback loop is the goal in order to enhance stability and noise shaping. Actions: Summing Node Config- uration: Set up the summing node such that the input and feedback signals are precisely combined. Loop Filter Adjust- ment: Adjust the loop filter's parameters to attain the intended noise-shaping outcome. To regulate the noise spectrum, this entails changing the filter coefficients. Delay Cell Placement: To improve noise redistribution, place the gated delay cells within the feedback loop to add regulated delays.

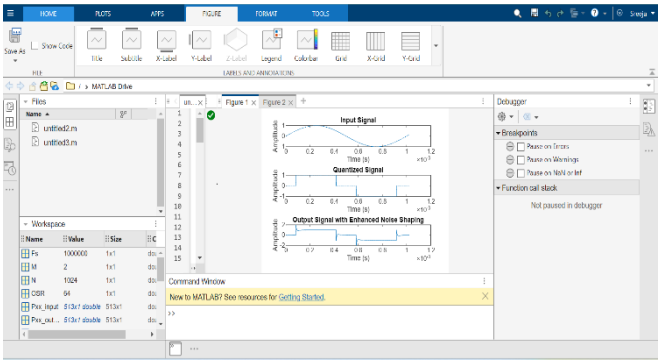


Fig. 4. Graph using Matlab for noise shaping.

A. *Digital Decimation Filtering*

The goal is to create a lower-rate digital signal from the oversampled bitstream that the modulator produced. Actions: Comb Filter Design: As the first step in the decimation process, design a comb filter. The sampling rate is lowered and high-frequency noise is reduced via the comb filter. The implementation of extra finite impulse response (FIR) or infinite impulse response (IIR) filters can enhance signal refinement and produce a high-resolution digital output.

B. *Clock Generation and Distribution*

The aim is to guarantee precise and coordinated clock signals for every ADC element. Actions: PLL Design: Create a steady, high-frequency clock signal by developing a phase- locked loop (PLL). To ensure minimal skew and jitter, spread the clock signal to different regions of the ADC using clock buffers. Ensuring synchronization of clock signals among all components is crucial in preserving timing accuracy and signal integrity

IV.RESULTS

The enhanced performance of the suggested ADC design is confirmed by the experimental results. Notable conclusions include: 1. Enhanced SNR: When compared to conventional designs, the new ADC architecture shows a notable boost in SNR. The single fan-out gated delay cells' efficient noise shaping is responsible for this improvement. 2. Less Timing Jitter: A more accurate digital representation of the analog signal is produced by the precision of the gated delay cells, which reduces timing jitter. 3. Better Resolution: The ADC can handle high precision applications since it can attain a higher resolution. The improved noise-suppression capabilities of the suggested architecture directly lead to the higher resolution.
4. Robustness and Reliability: The prototype ADC performs well under a variety of operating circumstances, indicating its dependability and appropriateness for a range of high- precision uses.

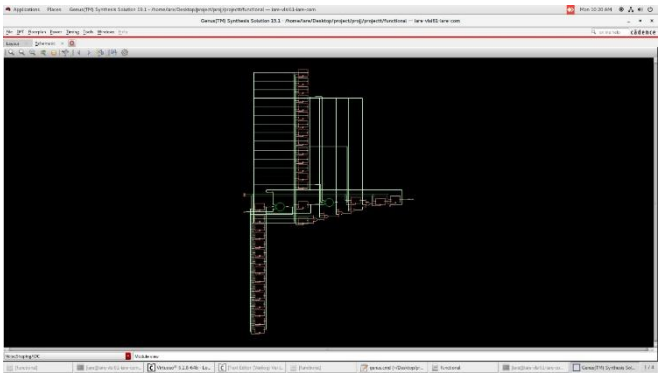


Figure 5: Circuit Diagram

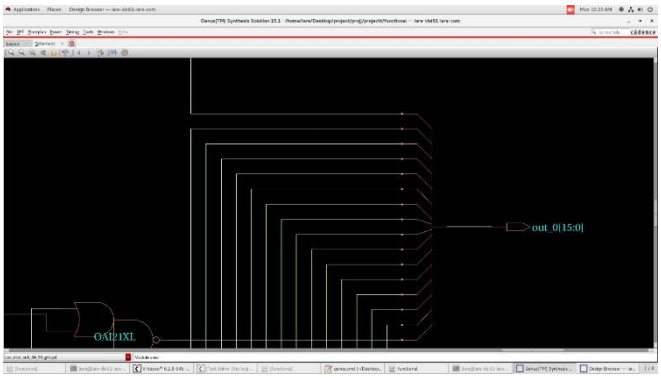


Figure 6: Output Block

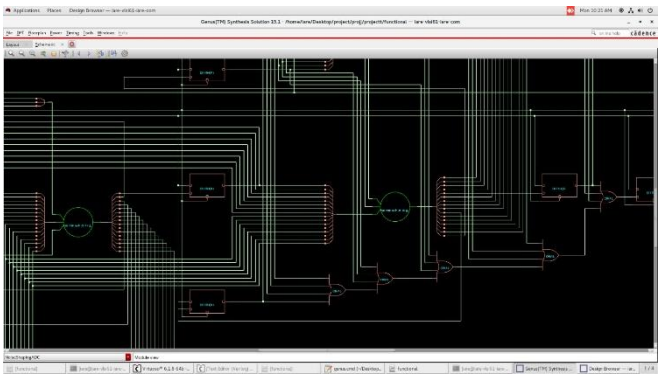


Figure 7 : Internal Implementation

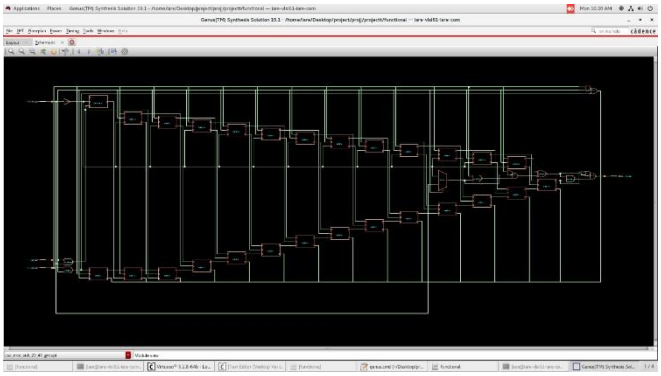


Figure 8 : Blocks of Integrators

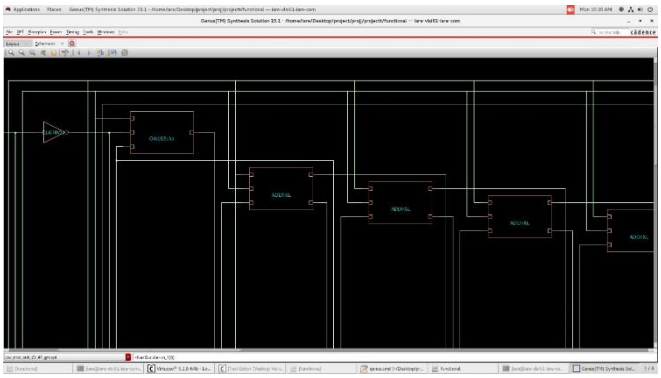
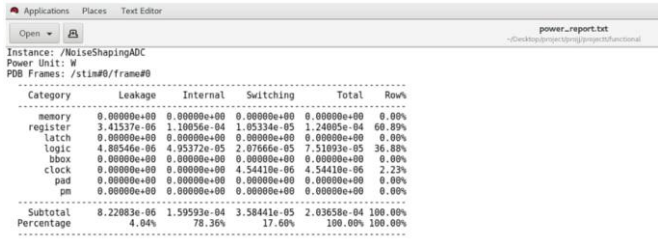


Figure 9 : Input Block



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Power Unit: W
PDB Frames: /stim#0/frame#0

  Category       Leakage      Internal     Switching       Total     Row%
--------------------------------------------------------------------------
    memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  register     3.41537e-06  1.10056e-04  1.05334e-05  1.24005e-04  60.89%
     latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
     logic     4.80546e-06  4.95372e-05  2.07666e-05  7.51893e-05  36.88%
      bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
     clock     0.00000e+00  0.00000e+00  4.54410e-06  4.54410e-06   2.23%
       pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
--------------------------------------------------------------------------
  Subtotal     8.22083e-06  1.59593e-04  3.58441e-05  2.03658e-04 100.00%
Percentage           4.04%       78.36%       17.60%      100.00% 100.00%
--------------------------------------------------------------------------
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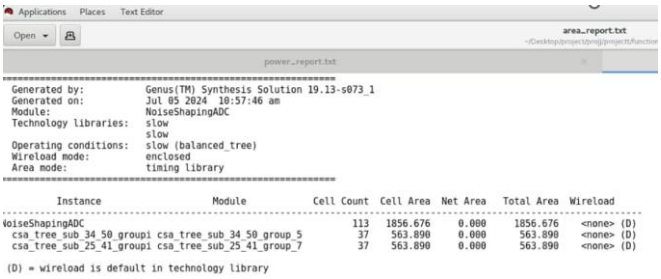
Figure 10 : Power



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Applications  Places  Text Editor
Open                                                    area_report.txt
power_report.txt
====================================================================
  Generated by:           Genus(TM) Synthesis Solution 19.13-s073_1
  Generated on:           Jul 05 2024  10:57:46 am
  Module:                 NoiseShapingADC
  Technology libraries:   slow
                          slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
====================================================================

        Instance                  Module           Cell Count  Cell Area  Net Area   Total Area  Wireload
--------------------------------------------------------------------------------------------------------
NoiseShapingADC                                         113   1856.676     0.000     1856.676    <none> (D)
  csa_tree_sub_34_50_groupi csa_tree_sub_34_50_group_5   37    563.890     0.000      563.890    <none> (D)
  csa_tree_sub_25_41_groupi csa_tree_sub_25_41_group_7   37    563.890     0.000      563.890    <none> (D)

(D) = wireload is default in technology library
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Figure 11 : Area

V. CONCLUSION

In conclusion, the development of the enhanced noise shaping ADC with single fan-out gated delay cells marks a significant advancement in analog-to-digital conversion technology. This innovative approach addresses several critical challenges faced by traditional ADC architectures and introduces new capabilities that enhance performance across various applications.

Key Contributions:

1. Improved Signal-to-Noise Ratio (SNR)
2. Low Power Consumption
3. Increased Resolution and Accuracy
4. Decreased Area

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