

FinFET Technology: Modeling and RF Characterization for 5nm Node Technology: A Review

N Sai Sriram and Dr. J.V. Suman,

¹ UG Student, Dept. of ECE, GMR Institute of Technology, Rajam

² Assist. Prof. Dept. of ECE, GMR Institute of Technology, Rajam

Abstract: The study offers new methods for understanding and simulating the radiofrequency, analog, and thermal characteristics of the FinFET at the 5nm CMOS technology node. The results of the thermal assessment show that changes in temperature have an effect on the threshold voltage and sub-threshold slope (SS). The maximum oscillation frequency and cut-off frequency of an n-FinFET RF device with a single gate contact are revealed by the RF investigation. Additionally, the study provides information about the device-level temperature sensitivity of the analog and RF Figures of Merit (FoMs) for the 5nm technology. The industry-standard BSIM-CMG model is adjusted to include the effects of self-heating (SH) and parasites in order to improve model accuracy. The updated BSIM-CMG model increases accuracy by taking self-heating and parasite effects into account. Effective heat pathways for lowering junction temperature are found by employing vias on silicon and stacks of conductive materials made of metal. It should be remembered, though, that using these heat pathways could raise parasitic capacitance and negatively impact the circuit's functionality.

Keywords: RF Characterization, Thermal Impact, Self-Heating, Figure of Merit, FinFET, Analog Characteristics.

INTRODUCTION:

Microelectronics Revolution: Rapid semiconductor advances are bringing about a transformative era in microelectronics, pushing the boundaries of devices to previously unheard-of heights. The FinFET architecture is dominant at the 5nm technology node, which is a significant turning point that promises improved scalability and power efficiency.

Developing FinFET Capabilities: A thorough comprehension of the complex behavior of FinFETs is necessary to realize their full potential within the 5nm node. This understanding, along with accurate modeling abilities, is essential for developing the next generation of integrated circuits that power a wide range of applications, including IoT devices and high-performance computing.

Theory and Application-Based RF Methodology: The methodology of RF characterization and modeling is essential for linking theoretical understanding to real-world applications in the context of 5nm FinFETs. With an emphasis on modeling and measurement techniques for radio frequency applications, this article examines the electrical characteristics, physical features, and RF performance issues of FinFETs.

Driving Wireless Communication Innovation: This research is essential for improving wireless communication systems, processing data quickly, and getting RF technologies widely used. By enabling scientists and engineers to fully utilize FinFETs in radiofrequency applications, the customized radiofrequency methodology for 5nm FinFETs advances semiconductor research and influences the direction of electronics in the future.

METHODOLOGY:

Modeling RF Signals for 5nm FinFETs: A methodology for the characterization of radio frequency (RF) signals is presented, with particular attention to n-type FinFETs in the 5nm technology node. This method accurately captures both DC and RF performance, simplifying parameter extraction, by using a modified BSIM-CMG model.

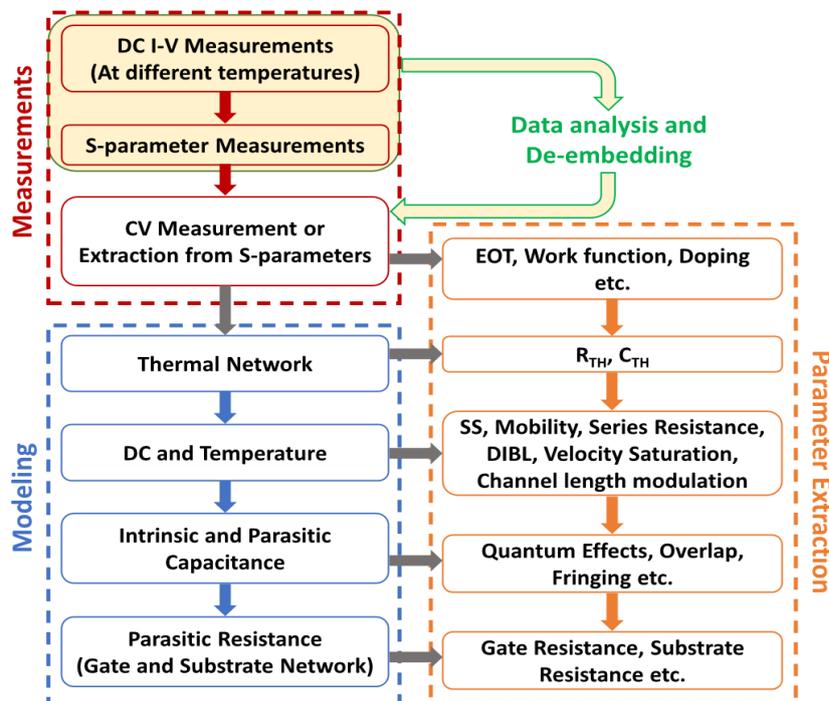


Figure 1: Flowchart For Modeling

2. Validation and Suitability of PDK Development: Demonstrating strong agreement between modeled and measured data to demonstrate the approach's validity through rigorous validation. Its high accuracy makes it an effective tool for expediting the creation of process development kits (PDKs).

3. Complex RF Models and Layout Effect Evaluation: Introducing a novel small-signal model for RF bulk FinFETs that has been effectively verified in cutting-edge technologies. Investigating the effect of layout dimensions on FinFET RF performance yields knowledge that advances and improves RF circuit design.

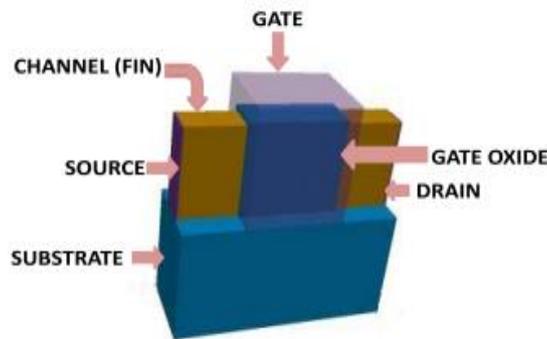


Figure 2: Structure of FinFET used

4. Innovation in Parameter Extraction and SG JL FinFET Design:

A creative approach to parameter extraction handles FinFET technology process variations and provides flexibility in a variety of experimental setups. The SG JL FinFET’s design is also presented in this paper, with its behaviour and performance characteristics precisely portrayed through the use of calibrated simulation techniques.

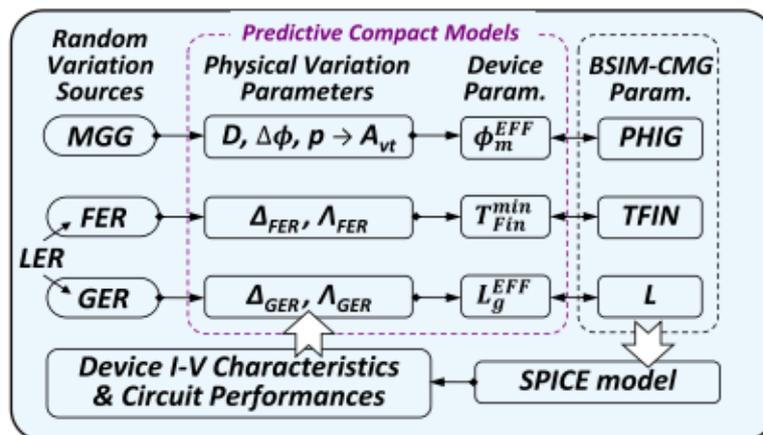


Figure 3: Parameters used

RESULTS:

1. Thermal Impact: A few critical parameters are greatly influenced by the 5nm FinFET technology node's behaviour and thermal characteristics. Temperature changes have an impact on both the threshold voltage and the sub-threshold slope. When exposed to temperature variations, these properties fluctuate. The threshold voltage varies by 70 millivolts, whereas the sub-threshold slope varies by 69%. When evaluating the stability and dependability of FinFET devices, thermal effects are crucial. Variations in temperature can lead to changes in the behaviour and performance of electrical systems.

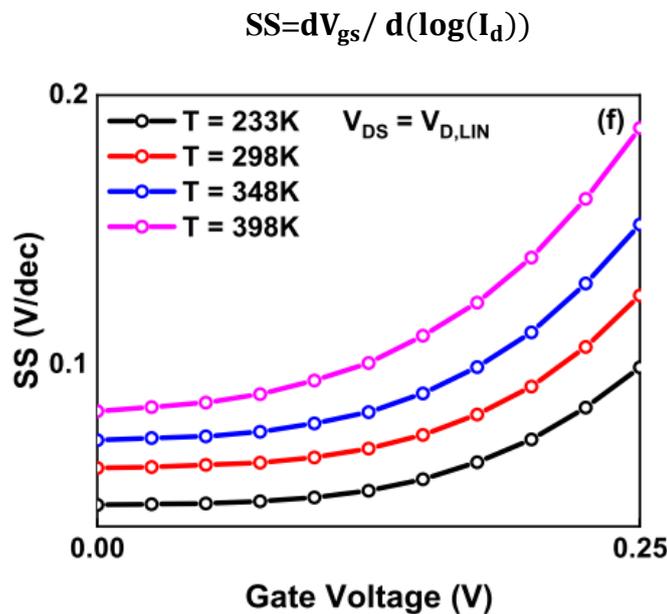


Figure 4: voltage vs sub-threshold Slope

2. RF Device Characteristics: The RF characterization of n-FinFET RF devices at the 5nm node is investigated in this exploration. The maximum oscillation frequency and cutoff frequency are its main concerns. Maximum oscillation frequency represents the upper bound of the device, whereas cutoff frequency affects power gain and bandwidth. The study's conclusions apply to the state of technology today. Analyzing RF characteristics yields useful insights for design optimization and performance enhancement. The results have implications for RF devices and wireless communication systems.

$$F_t = g_m / 2\pi C_{gs}$$

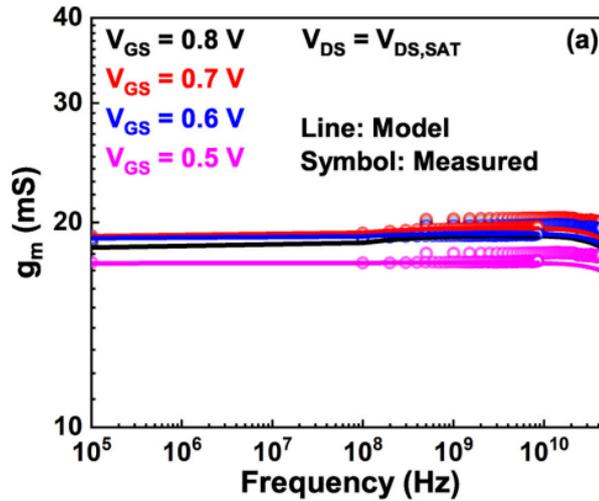


Figure 5: Frequency vs gm

Analog and RF Figures of Merit:

Important Figures of Merit (FoMs) like current gain, gain frequency, power gain, and oscillation frequency are revealed by a study on semiconductor devices at the 5nm technology node. These metrics provide designers and engineers with insightful information. For evaluating and fine-tuning analog and radio frequency devices at 5 nm, parameters such as gain frequency, power gain, and oscillation frequency are essential. The study's conclusions set standards for assessing semiconductor devices and propel advancements in 5nm technology. This facilitates developments in the RF and analog domains, enabling engineers to improve applications and maximize performance in these fields.

$$g_m = \Delta I_{ds} / \Delta V_{gs}$$

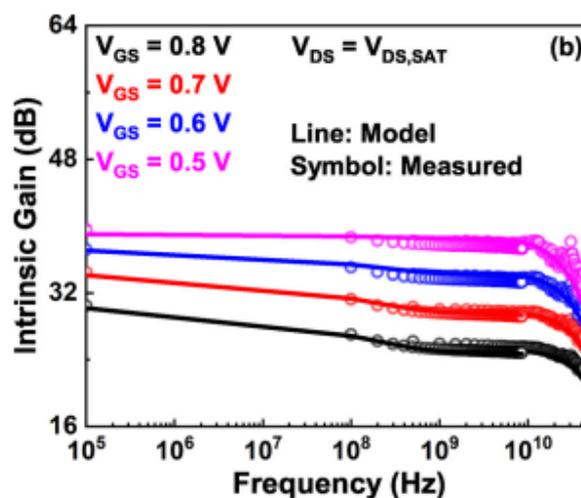


Figure 6: Frequency vs Intrinsic Gain

CONCLUSION:

This paper presents a thorough characterization and modeling approach for 5nm FinFETs with an emphasis on their thermal, analog, and radio frequency characteristics. When compared to measured data, the modified BSIM-CMG model shows accuracy in predicting device behaviour, taking parasitics and self-heating into account. Process Design Kit (PDK) development may be sped up by the methodology, as evidenced by the successful alignment of simulated and measured results. The study comes to the conclusion that this methodology is precise and essential for advancing the development of RF Systems-on-Chip (SoCs) at the 5nm node. In conclusion, the paper lays a solid basis for the accurate and effective development of radio frequency applications in cutting edge semiconductor technologies.

REFERENCES:

- [1] Parihar, S. S., Pampori, A., Dwivedi, P., Huang, J., Et al. ,“A Comprehensive RF Characterization and Modeling Methodology for the 5nm Technology Node FinFETs”, IEEE Journal of the Electron Devices Society, vol. 11,pp. 444-445,2023.
- [2] Zhang, W., Yin, S., Hu, W., & Wang, Y. (2021). “Novel physics-based small-signal modeling and characterization for advanced RF bulk FinFETs”. IEEE Transactions on Electron Devices, vol 68(5),pp 2160-2166,2021.
- [3] Tinoco, J. C., Rodriguez, S. S., Martinez-Lopez, A. G., Et al., “Impact of extrinsic capacitances on FinFET RF performance”. IEEE transactions on microwave theory and techniques, vol 61(2),pp 833-840,2013.
- [4] Zhang, Z., Jiang, X., Wang, R., Guo, S., Wang, Y., & Huang, R. “Extraction of process variation parameters in FinFET technology based on compact modeling and characterization”. IEEE Transactions on Electron Devices, vol 65(3), pp-847-854, 2018.
- [5] Sehgal, H. D., Pratap, Y., & Kabra, S. “Designing and Reliability analysis of radiation hardened Stacked gate Junction less FinFET and CMOS Inverter”. IEEE Transactions on Device and Materials Reliability, Vol 23(2),pp 249-256,2023.