

FPGA-Based Design and Implementation of DDR SDRAM Controller

Aditi Yadav¹ & Prof. Prashant Goyal²

¹M.Tech Scholar, ECE Dept., Patel College of Science & Technology, Indore

²Assistant Professor, ECE dept., Patel College of Science & Technology, Indore

Abstract: Double Data Rate Synchronous DRAM (DDR SDRAM) has become a mainstream memory of choice in design due to its speed, burst access and pipeline features. The DDR SDRAM is an enhancement to the conventional SDRAM running at bus speed over 75MHz. The DDR SDRAM (referred to as DDR) doubles the bandwidth of the memory by transferring data twice per cycle on both the rising and falling edges of the clock signal. The designed DDR Controller supports data width of 64 bits, Burst Length of 4 and CAS (Column Address Strobe) latency of 2. DDR Controller provides a synchronous command interface to the DDR SDRAM Memory along with several control signals. In this paper, the implementation has been done in Verilog HDL by using Xilinx ISE 9.2i and Model-SIM 64b.

Key Words: Double Data Rate, Column Address Strobe (CAS), Synchronous Dynamic RAM.

1. INTRODUCTION

The motivation behind designing the processor is to increase its speed so that our task becomes too fast. In this research we tried to find some of the techniques to reduce the processing time of the processor. A processor is something which processes the given task. It is developed to make human task easy, and when it processes micro things it is called as a microprocessor. It contains basically two things. One is the CPU and second is the memory. CPU stands for central processing unit [1]. It controls the whole processor; we can also call it a human brain. The design of processor needs the designing of CPU and memory. The memory can be static or random. Design of

CPU can be done in different ways but its fundamental operation remains the same. CPU is designed on small scale and large scale integration. Processors are designed with enhancements like decreasing power consumption, increasing more pipeline stages, increasing speed and minimizing the chip area. The basic operation performed by a processor is fetching, decoding and executing the given instruction. After that the output will store in memory. For storing the results in memory some mechanism is applied. With the rapid development in the processor's family, speed and capacity of a memory device is a major concern. The DDR is an enhancement to the traditional synchronous DRAM. The DDR is able to transfer the data on both the edges of each clock cycle. Thus doubling the data transfer rate of the memory device. The DDR is available in a very low cost that's why it is widely used in personal computers where they are basically used to provide the functions of storage and buffers. The DDR SDRAM supports the data widths of 16, 32 and 64 bits. It automatic refresh during the normal and power down modes.

1.1 Processor architecture and its fundamentals

A processor takes input information, processes that input and produces output result which gets stored inside the memory [2]. This is the fundamental operation of a processor. The functional units of a processor are input output, memory storage, arithmetic logic unit and control unit. Information in a processor is in the form of data. In terms of technical language we can define this data in bits or bytes. The memory of the processor can be increased as per need. Information in a

processor is known as instruction which is given by an human operator. There is a particular language for the understanding of processor called as assembly language. It contains the instruction sets. A sequence of instruction is called as program.

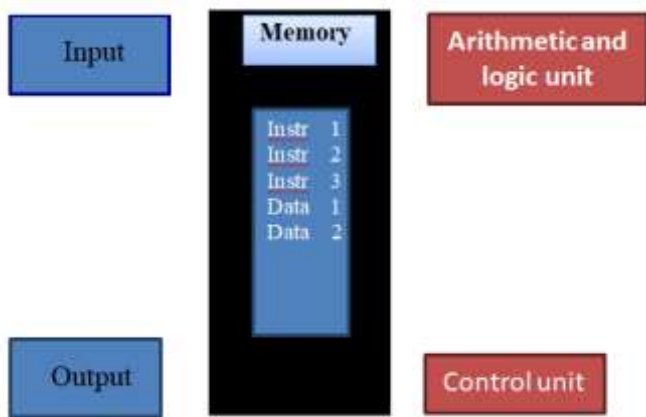


Fig 1.1 Overview of the RISC processor

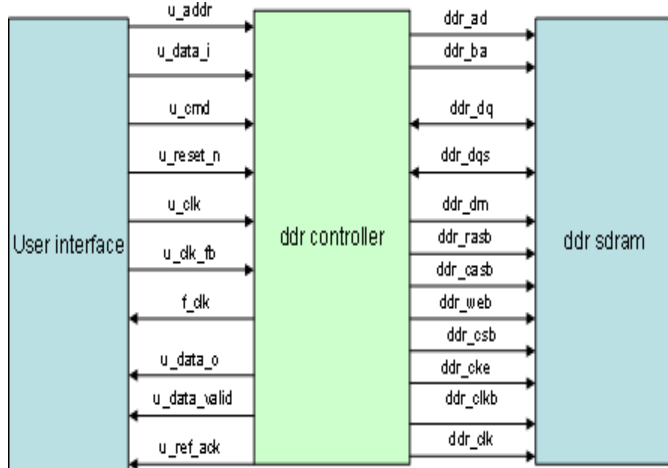
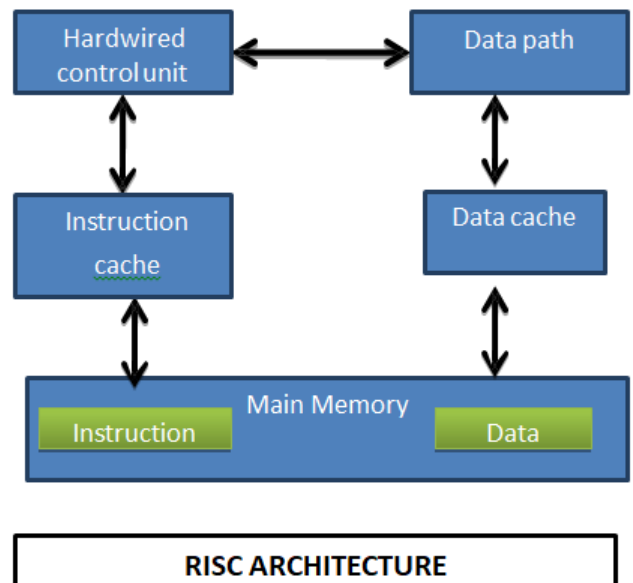


Fig 1.2 Top Level block diagram

The rules are made to check whether the design is correct or not. After full verification of each rule the design goes to the fabrication lab for fabrication. This process is called as Electronic design Automation. These rules basically check layout not the schematic [12]. There are lambda based rules, Meta rules and micro based rules. Amongst them most popular is lambda based rules. These rules play an important role because they are an interface between design engineers and fabrication engineers. There are design rules checking software. There are basic three rules for width, length and masks. Some of the lambda rules are as follows-

- Well to well spacing should be 2λ

- Well to poly spacing should be 2λ
- Well to metal spacing should be 3λ
- Poly-active minimum spacing should be 1λ
- Poly overlap spacing should be 2λ



2. Problem statement -

Multiprocessor systems can solve problems many times faster than a single processor alone. However, these processors must communicate in order to efficiently divide and solve a problem. Fast volatile memory is designed for use with a single processing system. In order for multiprocessor systems to access a common resource such as a memory, there must be some facilitation between the processing systems and the memory, in order to avoid any data corruption or malfunctioning of the system. [1] This is where the arbiter comes into play. An arbiter can be considered as a controlling system, which can be incorporated in between the multiprocessor systems and the shared memory. The arbiter follows a set of rules to pass the communication between the various processing systems.

3. LITERATURE SURVEY

VHDL is used to write text models that describe a logic circuit. There is a simulation program for test the logic design using simulation models to represent the logic circuits that interface to the design. This collection of simulation models is commonly called a test bench. VHDL has filed input and output capabilities, and can be used as a general-purpose language for text processing, but files are more commonly used by a simulation test bench for stimulus or verification data. In this case, it might be possible to use VHDL to write a test bench to verify the functionality of the design using files on the host computer to define stimuli, to interact with the user, and to compare results with those expected.

Sharda P. Katke, G.P. Jain et al. 2024 [1] title: “Design &Implementation of 5 stages pipelined architecture in32 bit RISC processors using Pipelining SDRAM”: The proposed work has improved the speed of the processor with 5 different cycles.

Nupur Gupta1, PragatiGupta2, Himanshi Bajpai3, Richa Singh4, Shilpa Saxena5 2023 [2] title: “Analysis of 16 Bit Microprocessor Architecture on FPGA Using VHDL DDR”. This paper involves the design and Simulation of 16 bit microprocessor architecture on FPGA using VHDL. Significant features such as the , increased speed ,minimal implementation real-estate, reduction in power and maximum configurability are provided by several FPGAs.

R. Uma et al. [3] title: “Design and Performance Analysis of 8-bit RISC Processor using Xilinx Tool”. In the present work, the design of an 8-bit data width Reduced Instruction Set Computer (RISC) processor is presented; it was developed with simplicity and implementation efficiency in mind.

4. Methodology

MICROWIND is truly integrated EDA software encompassing IC designs from concept to completion, enabling chip designers to design beyond their imagination. MICROWIND integrates traditionally separated front-end and back-end chip design into an integrated flow, accelerating the design cycle and reduced design complexities. Microwind thus facilitates to vary the parameters of MOSFET’s etc so that our study becomes easy [11]. The functional block diagram of the DDR Controlling is shown in fig 3.1. It consists of three modules, the main control module, the signal generation module and the data path module. The main control modules has two state machines and are fresh counter, which generates proper I state and cstate outputs according to the system interface control signals. The signal generation module generates the address and command signals required for DDR based on I state and cstate.

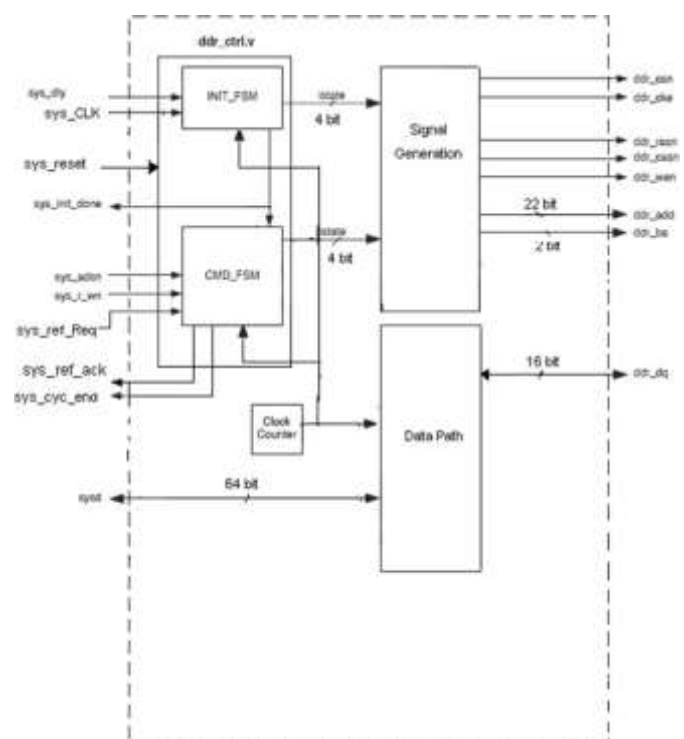


Fig 4.1 Functional Block Diagram

Width to length ratio (w/l Ratio) for any transistor is an important parameter because it affects the current or we can say that switching of the circuit. There is a direction relation between channel width and the output current. This will affect the overall function of the processor.

The **material** plays an important role in changing the **speed of the processor**. Increasing the speed is major concern. The main idea for this is decreasing the channel length so that the switching of current increases. Since, the drive current requirement to switch the load devices depends upon not only the physical channel length but also upon total capacitance. Scaling down the device dimensions can also be a factor for increasing the speed.

Pipelining (pipelined architecture) is a process where a microprocessor involves several stages of execution one after another in different segments. It is developed to reduce the total time for processing. These will in turn improve the speed of the processor. A pipelined architecture is little more complex than non-pipelined. As we know that complexity always increase when design becomes small and speed becomes a major issue. We have to add some mechanism here, like some registers. Now in case of pipelining, in the first cycle t1 fetching is done and then its data is stored in register R1, thus the fetch register is free to fetch new bit.

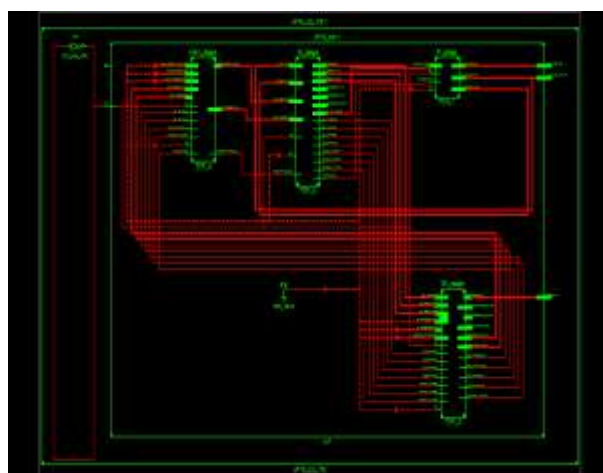
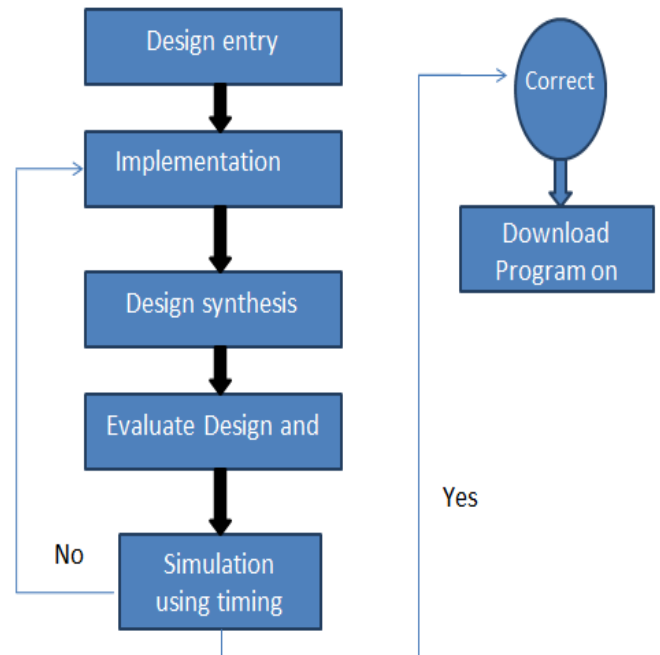


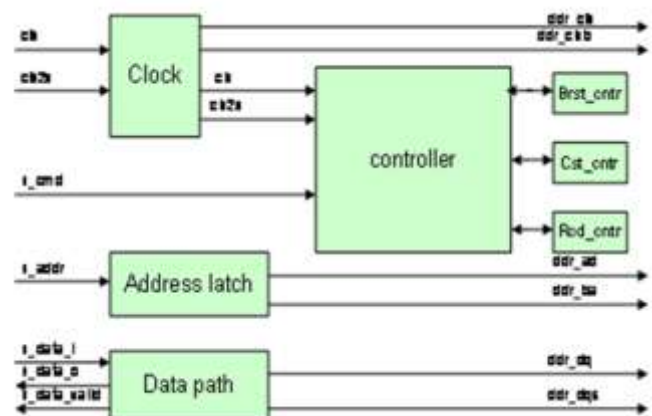
Fig 4.2: Architecture of 16 bit RISC processor on

Microwind

5. FPGA design flow chart



6. DDR Controller Architecture



The basic function of **address latch module** is to gets its control signals from the controller and generates row, column and bank addresses for the DDR SDRAM. The address latch also generates different control signals like burst_max, cas_lat_max for the burst counter and cas latency counter.

One of the most difficult aspects of DDR SDRAM controller design is to transmit and capture data at

double data rate. This module transmits data to the memories. The basic function of **data path module** is storing the write data and calculates the value for read data path.

6. RESULTS:

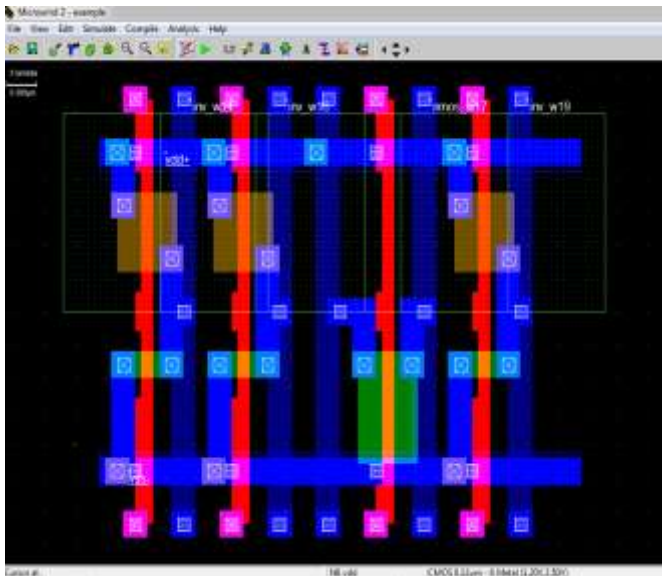


Fig 6.1: Layout design 16 sense

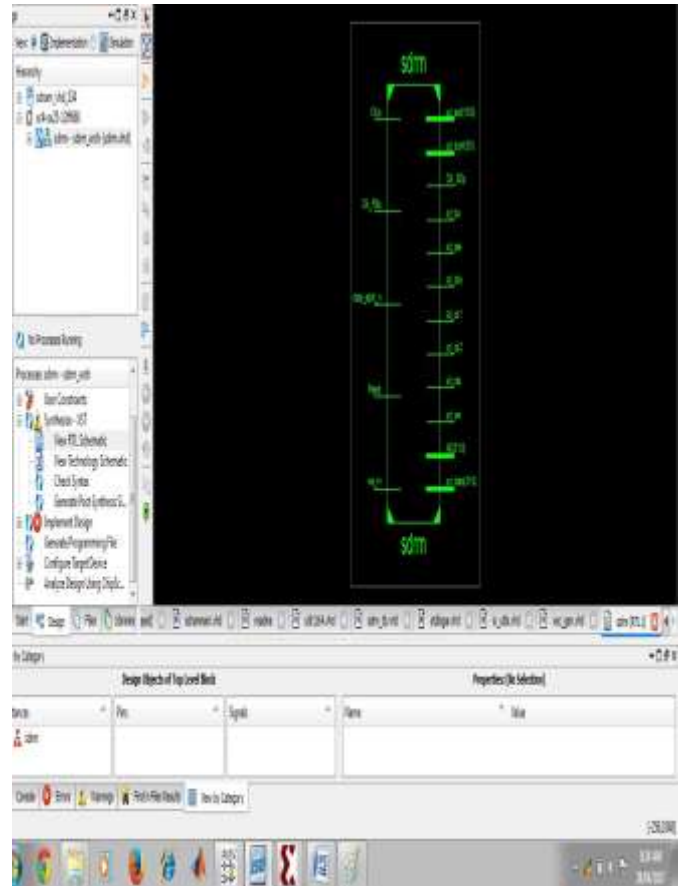


Fig 6.3: SDRAM Xilinx Design

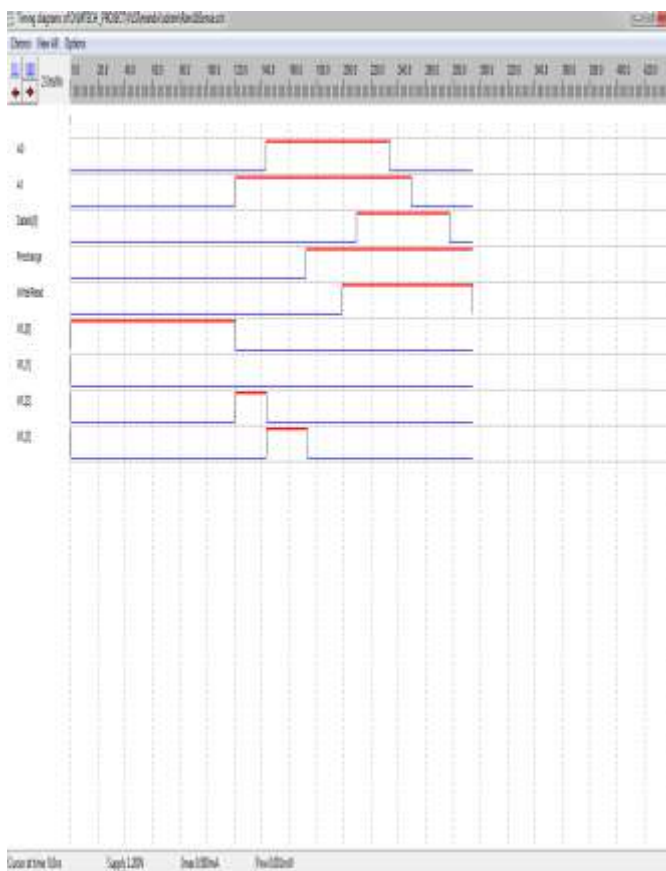


Fig 6.2: Timing waveform16 sense

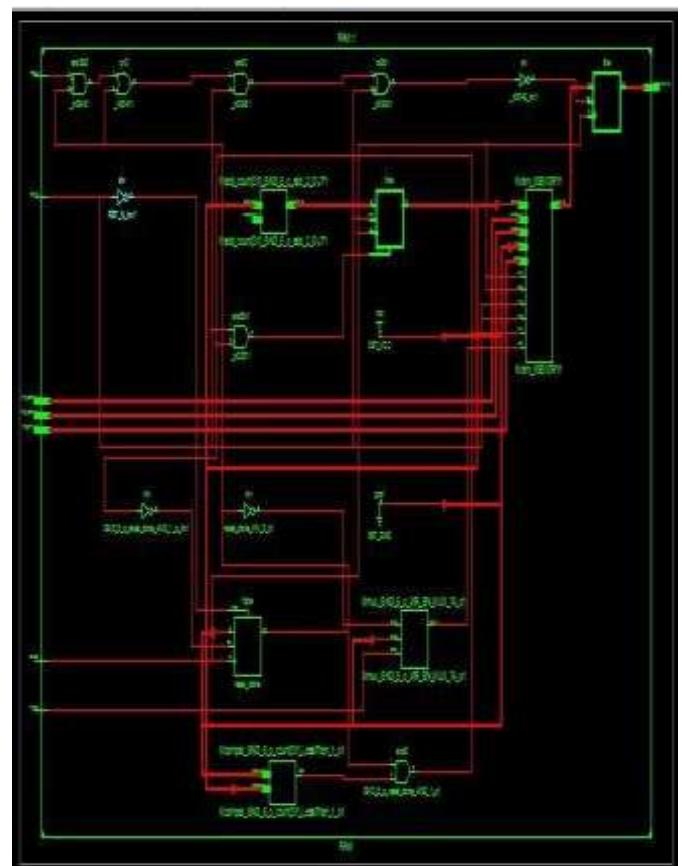


Fig 6.4: RTL logic design



Fig 6.5: Enhancement report

7. CONCLUSION

Conventional 6T SRAM and MESFET 6T SRAM are analyzed through cadence virtuoso tool in 45 nm technology. It is seen that sub-threshold and gate leakage, both effects the operation of the SRAM cell. In this paper MESFET is used to simulate the 6T SRAM cell and it is concluded that MESFET increases the performance of SRAM cell. The considerable change in the sub-threshold leakage is observed in comparison with the gate leakage. Total leakage in the SRAM cell can be reduced to 10 % using MESFET. Further SVL technique is applied in MESFET SRAM cell in which LSVL provides increased ground voltage and USVL provides reduced supply voltage during standby mode which reduces the leakage by 34 %. Therefore, results in reduced power dissipation and increased performance.

REFERENCES

1. J.L. Hennessy, D.A.Patterson, "Computer Organization and Design: The Hardware / Software Interface", Second Edition, Morgan Kaufmann, 2023.
2. M. Shand, "Flexible Image Acquisition using reconfigurable hardware" In Proc. of the IEEE Workshop on Field Programmable Custom Computing Machines, April 2022.
3. Jen-Shiun Chiang and Jun-Yao Liao, "A novel asynchronous control unit and the application to a pipelined multiplier", IEEE, pp. II 169-172, 2022.
4. Design and implementation of 5 stage pipelined 32 bit RISC processor Sharda P. Katke1,
5. G.P. Jain2 ISSN 2250-2459, Volume 2, Issue 4, April 2023.
6. R. Uma ,Pondicherry University, Pondicherry (IJERA), "Design and performance analysis of 8 bit RISC processor using Xilinx tool", Vol. 2, Issue 2, pp.053-058 Mar-Apr 2022.
7. Anand Nandakumar Shardul, "16-Bit RISC Processor Design for Convolution Application", International Journal of Advancements in Research & Technology, Volume 2, Issue 9, ISSN 2278-7763, September-2022.
8. Seung Pyo Jung, Jingzhe Xu, Donghoon Lee, "Design & Verification of 16 Bit RISC Processor",
9. Dimitris Mandalidis1 , Panagiotis Kenterlis2 , John N. Ellinas3,"A Computer Architecture Educational System based on a 32-bit RISC Processor", International Review on Computers and Software (I.RE.CO.S.), Vol.

xx, n. x, 2021.

10. T. S. Hall and J. O. Hamblen, "System-on-a-programmable chip development platforms in the classroom," IEEE Trans. Educ., vol. 47, no. 4, pp. 502–507, Nov. 2021.
11. R. Uma, "Design and Performance Analysis of 8-bit RISC Processor using Xilinx tool", International Journal of Engineering Research and Applications (IJERA), ISSN: 2248- 9622, Vol. 2, Issue 2,, pp.053-058 Mar-Apr 2020.
12. Sruthi.V1, Akhila.Raj.K.M2, Madhulika.A.R3, Ajin.A.S4 , "Design of a 3-T Half Adder", SSRG International Journal of Electronics and Communication Engineering, Volume 3 Issue 6 , June 2020.
13. J. Bhasker, "A VHDL Primer", Third Edition, Pearson, 2019.