

FPGA Implementation of the Advanced Encryption Standard Algorithm Using VERILOG-HDL

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Abstract – This paper presents the hardware design and functional verification of an Advanced Encryption Standard (AES-128) encryption system optimized for real-time security applications. The primary objective is to implement a high-speed cryptographic engine on hardware to overcome the processing latency bottlenecks inherent in software-based encryption. Utilizing a modular design methodology in Verilog HDL, each core algorithmic stage—SubBytes, ShiftRows, MixColumns, AddRoundKey, and Key Expansion—was individually engineered and integrated into a unified 10-round pipeline architecture. Stage-specific verification was executed using standalone testbenches, and functional accuracy was validated through behavioral simulation waveform analysis. The experimental results confirm flawless logical transformation of plaintext inputs into secure ciphertext across all modules without any runtime computational errors. By exploiting hardware-level parallel processing frameworks, this architecture successfully minimizes execution times while improving throughput efficiency and cryptographic data diffusion. This modular accelerator design provides a high-performance hardware baseline suited for physical deployment in FPGA and VLSI environments, including secure telecommunication networks, banking transactions, wireless infrastructures, IoT devices, and real-time embedded systems.

Key Words: AES-128, Verilog HDL, VLSI, IOT, FPGA, Cryptographic hardware, Parallel processing, Waveform simulation.

1. Introduction

In today's digital world, secure data transmission has become very important due to the rapid growth of communication networks, cloud computing, and online services. Sensitive information such as banking details, personal data, and confidential documents must be protected from unauthorized access and cyber attacks. Cryptography plays a major role in ensuring data security by converting readable information into an encrypted format that can only be accessed using a secret key. Among various encryption techniques, the Advanced Encryption Standard (AES) is widely used because of its high security, reliability, and fast processing speed.

AES is a symmetric key encryption algorithm developed by the National Institute of Standards and Technology (NIST). It operates on fixed-size data blocks of 128 bits and supports key sizes of 128, 192, and 256 bits. In AES-128, the encryption process is completed in 10 rounds consisting of operations such as SubBytes, ShiftRows, MixColumns, and AddRoundKey. These transformations provide strong confusion and diffusion, making the encrypted data highly secure. Due to its strong resistance against attacks, AES is extensively used in wireless communication, banking systems, military applications, embedded systems, and secure internet communication.

This project focuses on the hardware implementation of AES-128 encryption using Verilog HDL. The design is developed using modular architecture where each AES stage is implemented separately and verified through simulation. Hardware implementation provides faster execution and better performance compared to software-based encryption methods, making it suitable for FPGA and VLSI applications. The project demonstrates secure and efficient encryption of plaintext into ciphertext using

a 128-bit secret key and highlights the importance of digital hardware design in modern cryptographic systems.

2. Literature Review

Here is the formatted literature comparison table tailored for this project manuscript. Extensive academic literature emphasizes the value of hardware-based cryptographic accelerators over general-purpose computing platforms:

- **Kouser et al. (2022)** validated an FPGA-centered implementation of AES focused on minimizing area and maximizing hardware logic utilization efficiency. Their architecture leveraged parallel structures to boost overall processing speed.
- **Srinivas & Akramuddin (2023)** developed a unified FPGA configuration supporting both encryption and decryption pipelines inside a shared hardware floorplan, establishing notable throughput gains.
- **Shastry et al. (2023)** introduced an Application-Specific Integrated Circuit (ASIC) approach to AES ciphers. Although ASIC implementations reduce active power budgets compared to programmable FPGAs, they suffer from high engineering costs and zero post-fabrication versatility.
- **Hoang & Nguyen (2024)** focused on structural optimization for real-time applications. Their implementation utilized highly optimized pipeline stages to lower processing latency within standard FPGA fabrics.
- **Katkade & Phade (2025)** combined an AES engine directly with serial interfaces (such as UART) to secure active streams of point-to-point data. This design highlights the real-world demand for inline, hardware-level encryption modules.

Table -1: Literature Survey

Research Author(s)	Platform	Core Practical Contributions	Primary Foundational Limitations
Kouser et al. (2022)	FPGA	Optimized multi-channel resource distribution frameworks.	Logic dependencies restricted cross-platform

			scaling.
Sai Srinivas & Akramuddin (2023)	FPGA	Shared logic blocks execute dual enc/dec operations.	Complex routing raised overall latency metrics.
Shastry et al. (2023)	ASIC	Drastically cut power demands via cellular tuning.	Upfront prototyping costs remain extremely restrictive.
Hoang & Nguyen (2024)	FPGA	Mitigated delay times inside critical path pathways.	Routing complexity spikes under larger key sizes.
Katkade & Phade (2025)	Serial	Successfully fortified low-bandwidth serial line transmissions.	Protocol translation injects additional interface overhead.

3. Proposed AES Architecture and Methodology

The AES-128 processing module handles a state matrix composed of a 4×4 array of bytes. The execution pipeline maps plaintext into a series of modular matrix transformations.

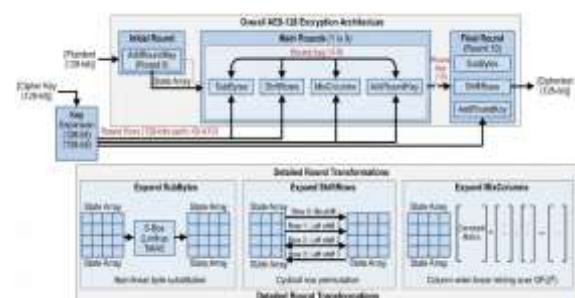


Fig -1: Hierarchical block diagram of AES-128 bit process.

3.1 Initial AddRoundKey

The encryption cycle initiates with a standalone AddRoundKey block. The 128-bit original plaintext is blended with the primary 128-bit secret key through bitwise exclusive-OR (XOR) operations. This step

introduces initial entropy before entering the main iteration loops.

3.2 SubBytes Transformation

The SubBytes stage represents the primary source of non-linear confusion within the cipher. Each individual byte in the state matrix is structurally swapped with an independent byte from a static (16×16) lookup configuration called the Substitution Box (S-Box). The replacement maps the upper nibble of the state byte to the S-Box row index (x) and the lower nibble to the column index (y) . For instance, a state byte containing 0x53 points directly to row 5, column 3, yielding an output value of 0xED.

3.3 ShiftRows Transformation

The ShiftRows block provides structural permutation across the matrix rows to establish linear diffusion. It performs cyclical left shifts on the state array rows as follows:

1. Row 0 is kept static.
2. Row 1 is cyclically shifted left by 1 byte.
3. Row 2 is cyclically shifted left by 2 bytes.
4. Row 3 is cyclically shifted left by 3 bytes.

3.4 MixColumns Transformation

The MixColumns operation processes the state array column-by-column, treating each as a polynomial over Galois Field $(GF(2^8))$. Each column is multiplied against a fixed polynomial matrix to distribute individual byte information across the entire column. The matrix equations are computed via the following linear combinations:

$$\begin{aligned}b_0 &= (02 \cdot a_0) \oplus (03 \cdot a_1) \oplus a_2 \oplus a_3 \\b_1 &= a_0 \oplus (02 \cdot a_1) \oplus (03 \cdot a_2) \oplus a_3 \\b_2 &= a_0 \oplus a_1 \oplus (02 \cdot a_2) \oplus (03 \cdot a_3) \\b_3 &= (03 \cdot a_0) \oplus a_1 \oplus a_2 \oplus (02 \cdot a_3)\end{aligned}$$

Note: * indicates finite field multiplication in GF(2^8) @ indicates XOR

3.5 Key Expansion and Round Additions

The Key Expansion module takes the primary 128-bit key and generates 10 independent round keys. During the AddRoundKey step of rounds 1 through 10, the updated state matrix is XORed with the corresponding round key block. This creates a high degree of key-dependent diffusion across the ciphertext output. Notably, the final round (Round 10) omits the MixColumns transformation entirely, in strict accordance with the NIST AES specification.

4. Hardware Implementation & Simulation Results

AES ciphers operate over fixed block widths of 128 bits, dynamically supporting cryptographic key lengths of 128, 192, and 256 bits. AES-128 relies on a mathematical architecture consisting of 10 structured rounds. While software solutions are popular, they are inherently prone to execution latency overheads and side-channel vulnerabilities. Hardware implementation using Hardware Description Languages (HDLs) offloads cryptographic computing to dedicated logical fabric, enabling highly parallel configurations that achieve high throughput and deterministic latency. This study outlines a modular Verilog HDL design targeting FPGA implementation of an AES-128 encryption algorithm.

Table -2: input and output status

Processing Module	Testbench State (Hexadecimal)	Input Data	Simulated Vector Output Data (Hexadecimal)	Verification Status
SubBytes	0011223344556677 8899aabbccddeeff		638293c31 bfc33f5c4e eacea4bc12 816	Functional Match
ShiftRows	63fca161bee28c3c4 c1193f5b8233ea0		63e293a0be 113e614c23 a13cb8fc8c f5	Functional Match
MixColumns	d4bf5d30d4bf5d30d 4bf5d30d4bf5d30		046681e50 46681e504 6681e5046 681e5	Functional Match
AddRoundKey	State: 1234567890abcdef1 234567890abcdef Key: 0f0f0f0f0f0f0f0f f0f0f0f0f0f0f		1d3b59779f a4c2e01d3b 59779fa4c2 e0	Functional Match

The behavioral verification waveforms confirm strict adherence to standard test vectors. Stable signal states during simulation verify that the modular hardware blocks maintain consistent data pipelines without logic hazards or execution faults.

4. RESULTS

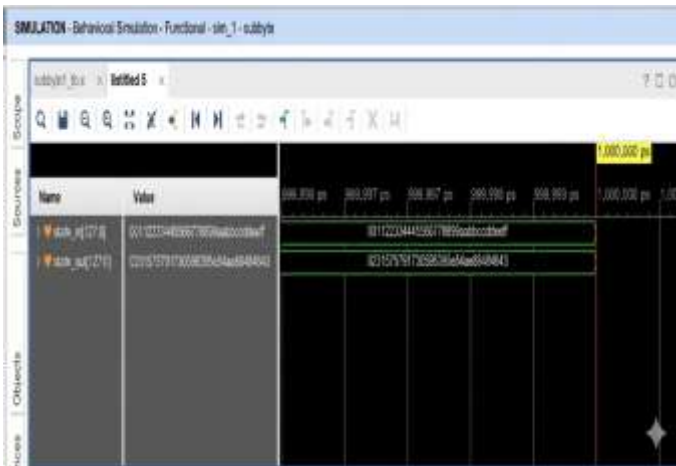


Fig -2: subbyte waveform

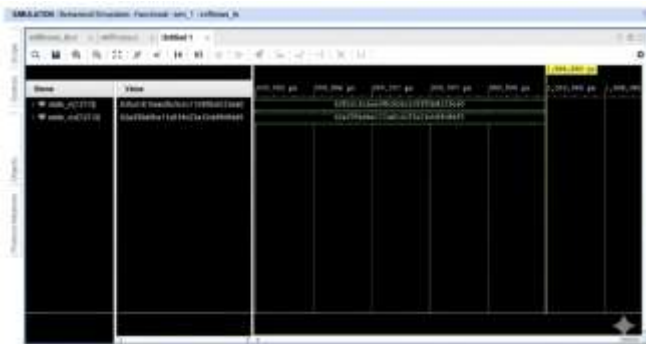


Fig -3: AddRoundKey waveform

The waveform confirms the correct Verilog implementation of the AES AddRoundKey module by demonstrating that the 128-bit input plaintext (1234567890abcdef1234567890abcdef) and round key (0f0f0f0f0f0f0f0f0f0f0f0f0f0f0f0f) successfully perform a bitwise XOR operation to produce the expected output state (1d3b59779fa4c2e01d3b59779fa4c2e0).

5. CONCLUSIONS

AES (Advanced Encryption Standard) is a secure and efficient symmetric key encryption algorithm widely used for protecting digital information. It operates on 128-bit data blocks and uses secret keys of 128, 192, or 256 bits for encryption and decryption. In this project, the AES encryption algorithm was implemented and analyzed using Verilog HDL. The main operations of AES such as SubBytes, ShiftRows, MixColumns, and AddRoundKey were designed and simulated successfully. SubBytes provides substitution using an S-box, ShiftRows performs cyclic shifting of rows,

MixColumns increases diffusion through matrix multiplication, and AddRoundKey combines the data with the round key using XOR operation. The simulation waveforms confirmed the correct functionality of each module. The project provided a clear understanding of cryptographic techniques, digital hardware implementation, and functional verification using simulation tools.

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