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Full Adder Circuit Design with CMOS Technology Implementing with Artificial Neural Network with Verilog HDL Code for Output

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Abstract:

The goal of this research is to create Full-Adder gate using a Complementary Metal Oxide Semiconductor (CMOS) and an Artificial Neural Network.We constantly bear in mind that any COMS circuit we design should be as inexpensive as possible.Multilayer ANN was employed in this work to create the circuit. Weights are employed to modify the value in our study, treating neurons as transistors and treating negative values as inverters.We are also designing Verilog-HdL Code to simply apply the full adder for experimenting an artificial neural network assigning weights to get appropriate results.

Keywords: Full Adder, CMOS,ANN,Verilog-HDL

Introduction:

The term "full adder" refers to an adder that takes three inputs and outputs two. A and B are the initial two inputs, while an input carry designated as C-IN is the third input. The normal output, denoted as S, is SUM, while the output carry is indicated as C-OUT. The majority 1's detector, or C-OUT for short, is a device whose output rises when several inputs are high. The architecture of a full adder logic allows it to cascade the carry bit from one adder to another and accept eight inputs collectively to form a byte-wide adder. We utilize a full adder since a 1-bit half-adder does not work when a carry-in bit is present, thus we also need to use another 1-bit adder.

A complete snake is more adaptable than a half viper because it can add three information bits. By connecting several complete adders, it can also be used to add multi-bit values. Because the complete viper has a convey input, it may chain many adders together and achieve multi-bit number expansion.

Multi-bit paired numbers can be added by various complete adders when they are connected in a chain. Data handling: Applications involving information handling, such as advanced signal processing, information encryption, and error correction, need full adders..Counters: To increase or decrease the count by one, counters use full adders..Multiplexers and demultiplexers: To select and route information, multiplexers and demultiplexers use full adders.

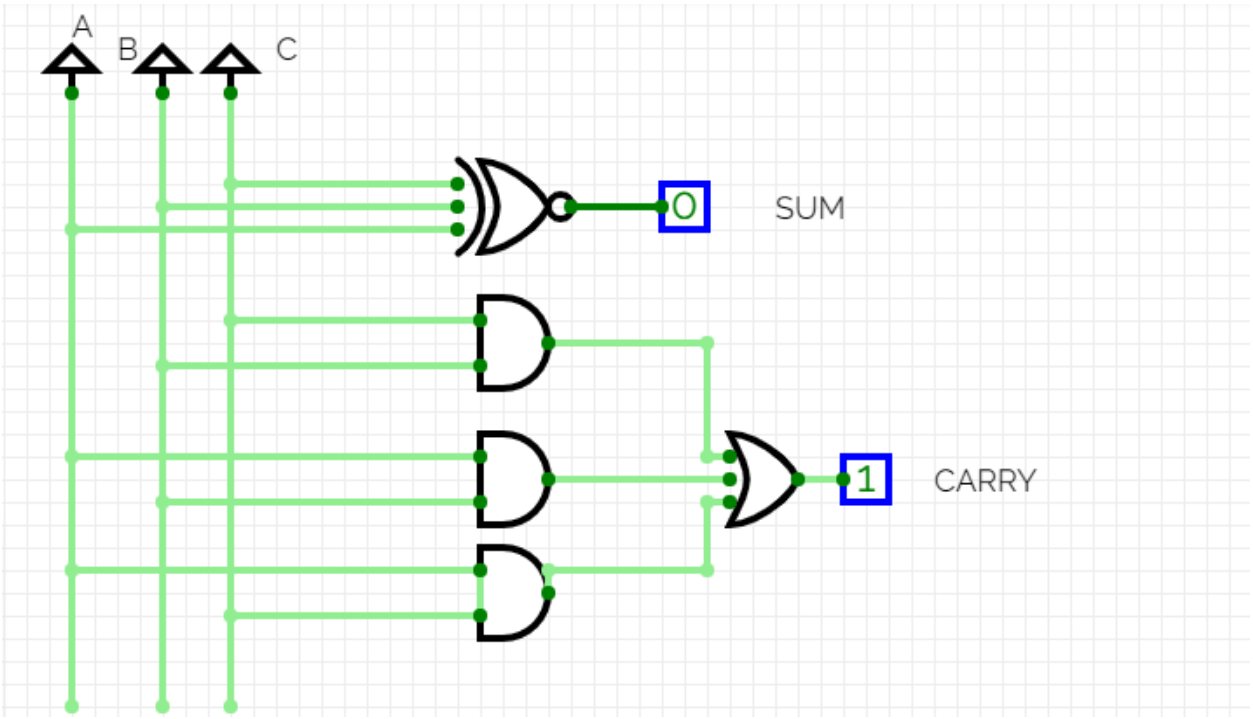

Figure 1: Circuit Diagram of Full Adder with Sum and Carry

Truth Table of SUM and CARRY:

INPUT			OUTPUT	
A	B	Cin	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

A Karnaugh map, often known as a K-map, is a visual technique used to minimize different Boolean expressions without the need for equation manipulation and the Boolean algebra theorems. One variant of the truth table that can be used is the Karnaugh map.

Karnaugh Map for SUM:

AB \ CD				
	0	1	0	1
	1	0	1	0

Equation for SUM=

A (EXOR)B (EXOR) C.----------(1)

Karnaugh Map for CARRY:

AB \ CD				
	0	0	1	0
	0	1	1	1

Equation for for CARRY=

AB+BC+CA----------(2)

Methodology for CMOS Design:

Massive scaling of a range of semiconductor devices has been made possible by CMOS (complementary metal-oxide-semiconductor) VLSI (very-large-scale integration) design. VLSI and the CMOS process together have pushed packages down to smaller sizes while maintaining affordable prices. CMOS technology is still important in older technology nodes, which are not anticipated to be phased out anytime soon, despite not being as compact and dense as FinFET technology. A new integrated circuit, SoC, or other component you're building will probably need to be made with CMOS VLSI design.

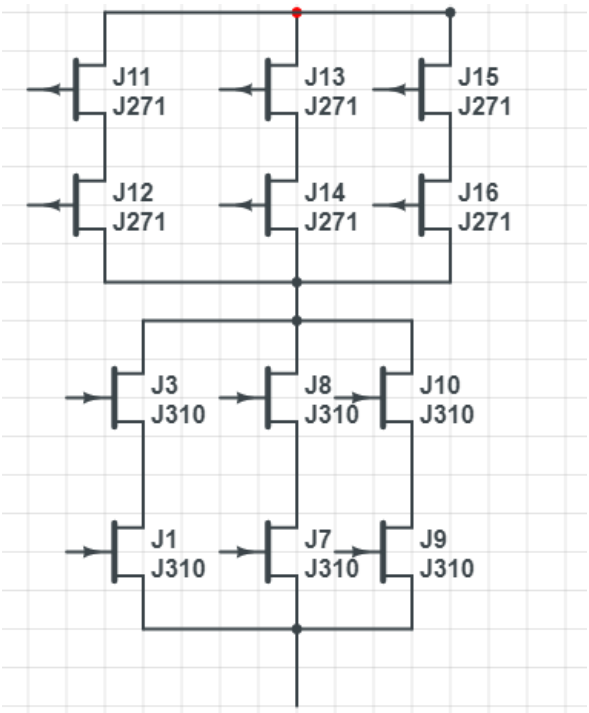

Fig:2:Pull up and Pull Down Circuit For Carry

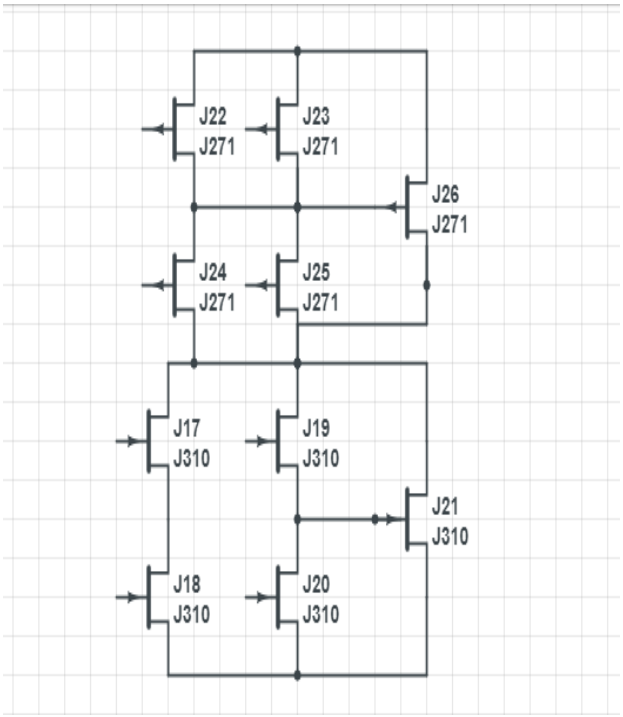

Fig:3: Pull Up and Pull Down Circuit for Sum

Artificial Neural Network Design for CMOS of SUM and Carry:

Units, or artificial neurons, are components of artificial neural networks. The Artificial Neural Network of a system is made up of these units grouped in a sequence of layers. The number of units in a layer can range from a few dozen to millions, depending on how many complicated neural networks are needed to uncover the dataset's hidden patterns. Artificial neural networks typically consist of hidden layers, output layers, and input layers. The input layer is where external data is fed into the neural network for analysis or education. After that, the data goes via one or more hidden layers, which convert the input into useful data for the output layer.

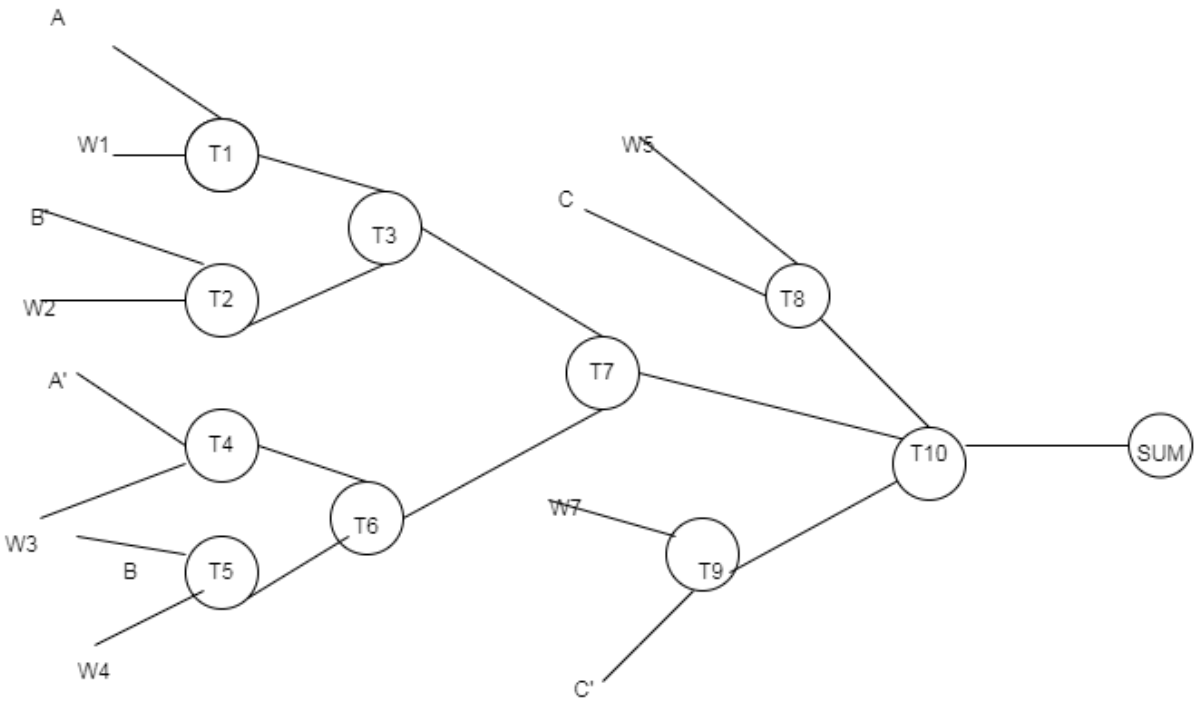

Fig :4: ANN Design for SUM

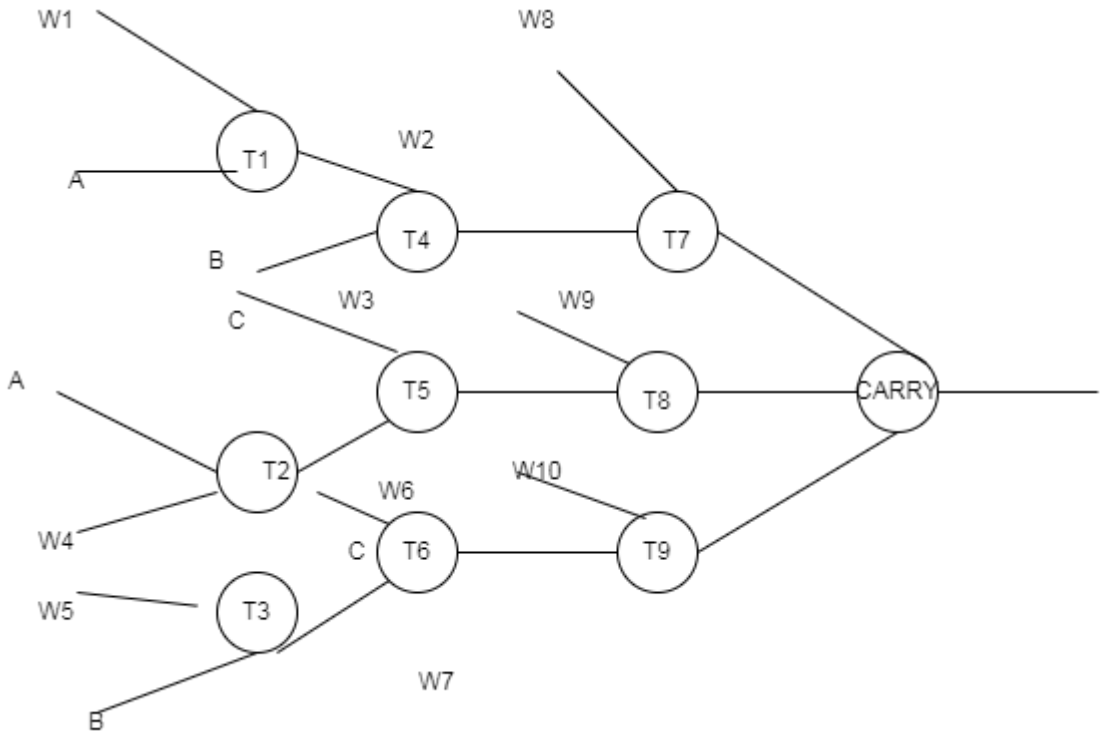

Fig :5: ANN Design for carry

Result in Verilog-HDL and Weight Calculation.

The term "full adder" refers to an adder that takes three inputs and outputs two. A and B are the initial two inputs, while an input carry designated as C-IN is the third input. The normal output, denoted as S, is SUM, while the output carry is indicated as C-OUT.

Since the complete adder is a combinational circuit, Verilog can be used to simulate it. Below is the logical expression for the two outputs, sum and carry. For two-bit binary values, A and B are the input variables, Cin is the carry input, and Cout is the output variable for sum and carry.

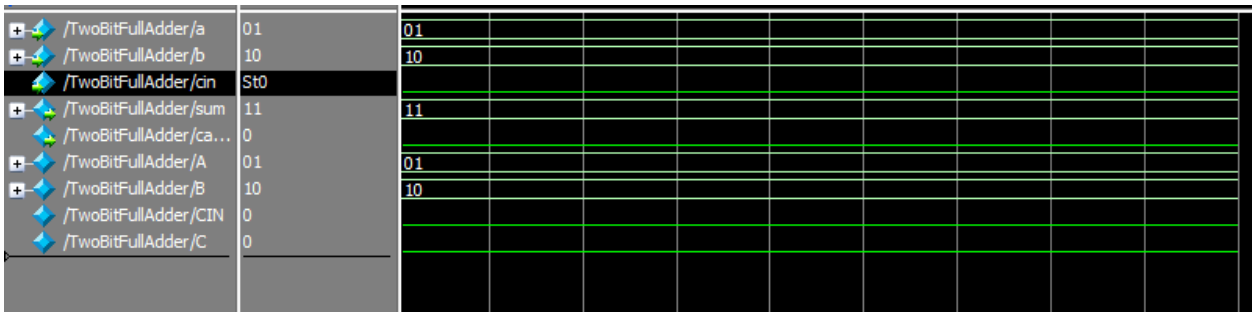

Fig6:Verilog Output for Full Adder

Weight Calculation for SUM:

T1=W1*A----------(3)

T2=W2*B'----------(4)

T3=T1*T2……..(5)

T4=W3*A'---------(6)

T5=W4*B--------(7)

T6=T4*T5-------(8)

T7=T3+T6-----(9)

T8=C*W5----(10)

T9=C'*W6------(11)

T10=T8*T9---(12)

Weight Calculation for CARRY

T1=A*W1-----(13)

T2=B*W2------(14)

T3=A*W3-----(15):

T4=C*W4-------(16)

T5=B*W5---(17)

T6=C*W6---(18)

T7=1*T2---(19)

T8=T3*T4-----(20)

T9=T5*T6----(21)

Carry=T7+T8+T9-----(22)

Conclusion:

The purpose of this project is to use an artificial neural network with a complementary metal oxide semiconductor (CMOS) to develop a full-adder gate.We always keep in mind that the lowest feasible cost should be the goal while designing any COMS circuit.This work used a multilayer artificial neural network to design the circuit. In our work, we treat neurons as transistors and negative values as inverters, and we use weights to adjust the value.Additionally, we are creating Verilog-HdL code that can be used to apply the entire adder for experimenting with artificial neural networks and allocating weights to provide relevant results.

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