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GDI based Area Delay and Power Efficient Braun Multiplier

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Abstract *— Multipliers are the most commonly used elements in today's digital devices. Multiplications are very expensive and slow the overall operation. As multipliers are complex circuits and must operate at a high system clock rate, reducing the delay of a multiplier is an essential part of satisfying the overall design. Today the requirements for minimizing the delay, area and power of multiplier circuit improve the efficiency of whole system which drives the technology to the next level. To accomplish the needs of today's digital devices, various types of low power and high performance multipliers have been designed. To achieve such requirements high performance multipliers are always preferable. The proposed technique provides low power dissipation and less propagation delay. By using this GDI based multiplier the number of transistors required for the circuit is also minimized. So an efficient multiplier design can be achieved through this technique.*

Keywords — *multiplier, low power, less area, GDI*

I. INTRODUCTION

Design of low power and high speed circuits is the main aim of processor designers. The operation that occurs frequently in digital signal processing and many other applications is multiplication. Multipliers consume more delay when compared to adders as they occupy large area. Generally the computational performance of a DSP processor is affected by the performance of its multipliers. Therefore several techniques are being proposed to speed up the computation while maintaining less area. The need for low power multipliers has increased as well.

The process of multiplication can be divided into three stages:1) Partial products generation stage, 2) partial products addition stage, 3) addition stage. In the first stage, the multiplier and the multiplicand are multiplied bit by bit to generate the partial products. In the second stage adders are used to add the partial products generated by the previous stage. This stage determines the speed of the overall multiplier and is more complicated.

Area, delay and power are the three most widely accepted metrics to measure the quality of a circuit or to compare various circuit styles. Now-a-days, the requirement of portability and the improvement in battery performance indicate that the power dissipation is one of the most critical design parameters. Some of the multipliers like Braun multipliers and Wallace Tree multipliers are efficient and easy to design when compared to other multipliers. In order to reduce the power dissipation in the adders, compressors and multipliers, a new technique called Gate Diffusion Input (GDI) can be used instead of Complementary Metal Oxide Semiconductor (CMOS).

II. BRAUN MULTIPLIER

Braun multipliers are widely used in order to achieve high speed and low power demand in DSP applications. It is a simple parallel multiplier which is generally called as carry save array multiplier. The structure consists of array of AND gates and adders arranged in an iterative manner and there is no need of logic registers. The standard form of an n-bit Braun Multiplier has n^2 AND gates for generating partial products, (n-1) Carry Save Adder stages and one Ripple Carry Adder stage which give final 4 MSB Product Bits as shown in figure 1. All the partial products are computed in parallel, and then collected through a cascade of adders. The adders may be a half adder or a full adder which generates two outputs i.e., sum and carry.

Adding numbers with minimal carry propagation can enhance the speed of the circuit. The completion time is limited by the depth of the carry save array, and by the carry propagation in the adder. The basic idea is that three numbers can be reduced to two, in a 3:2 compressor, by doing the addition while keeping the carries and the sum separate. This means that all of the columns can be added in parallel without relying on the result of the previous column, creating a two output "adder" with a time delay that is independent of the size of its inputs. The sum and carry can then be recombined in a normal addition to form the correct result. It is only the final

recombination of the final carry and sum that requires a carry propagating addition.

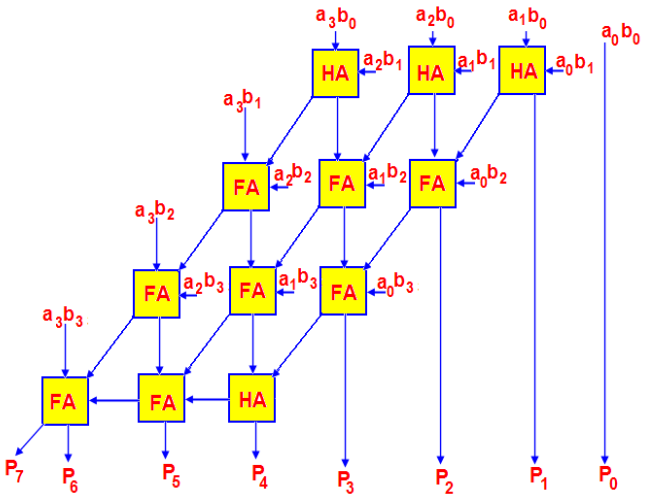

Fig. 1 Architecture of Braun multiplier

The partial products can be generated in parallel using the AND gates. Each partial product is added with the sum which has previously been produced by the row of adders. The carry out will be shifted one bit to the left or right and then it will be added to the sum which is generated by the first adder and the newly generated partial product. The shifting would carry out with the help of Carry Save Adder (CSA) and the Ripple carry adder should be used for the final stage of the output. Braun multiplier performs well for the unsigned operands that are less than 16 bits in terms of speed, power and area. But it has simple structure when compared to the other multipliers.

III. PROPOSED DESIGN

An alternative method for designing a high speed multiplier which occupies less area is proposed in this paper.

A. GDI

Gate diffusion Input is a new low-power design technique that allows solving most of the problems that occur while designing high performance logic circuits. This technique allows implementation of a wide range of logic functions using only two transistors as shown in table I. This is a new technique to cut back propagation delay, space and power dissipation. The main feature of GDI cell is that the VDD supply won't hook up with the supply of PMOS junction transistor and the GND won't hook up with the supply of NMOS transistor. Within the place of VDD and GND pins input signals are connected to build additional versatile than CMOS style.

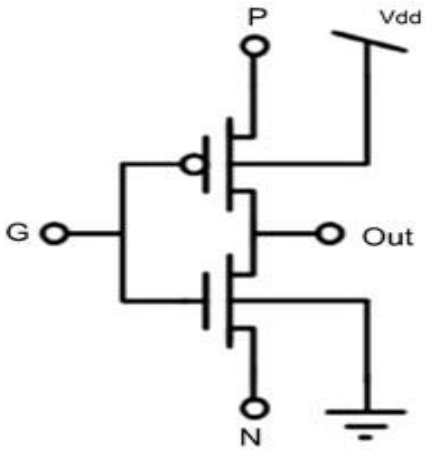

Fig. 2 Basic GDI cell

The basic GDI cell is shown in fig. 2. At first glance, the basic cell reminds one of the standard CMOS inverter, but there are some important differences.

1) The GDI cell contains three inputs : G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS).

2) Bulks of both nMOS and pMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter.

The GDI cell with four ports will be recognized as a replacement Multi-functional device, which may attain six functions with simply totally different combos of inputs G, P and N.

TABLE I
BASIC FUNCTIONS USING GDI

N	P	G	OUTPUT	FUNCTION
0	1	A	A′	INVERTER
0	B	A	A’B	F1
B	1	A	A’+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A’B+AC	MUX
B’	B	A	A’B+AB’	XOR
B	B’	A	AB+A’B’	XNOR

Table I shows how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions. Most of these functions are complex (6–12 transistors) in CMOS, as well as in standard PTL

implementations, but very simple (only two transistors per function) in the GDI design method.

B. Braun multiplier using GDI technique

The architecture of Braun multiplier consists of AND gates and adders. The adders may be half adders or full adders based on the number of inputs to be added. So the GDI based multiplier can be designed using GDI based AND gates, half adders and full adders.

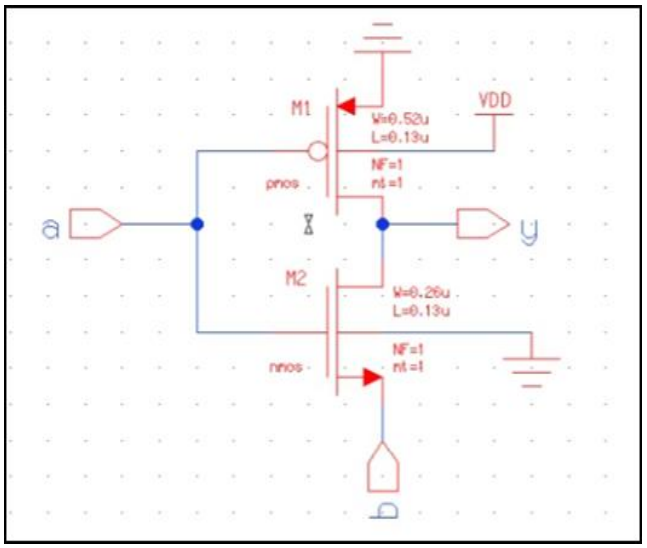

Fig. 3 AND circuit using GDI

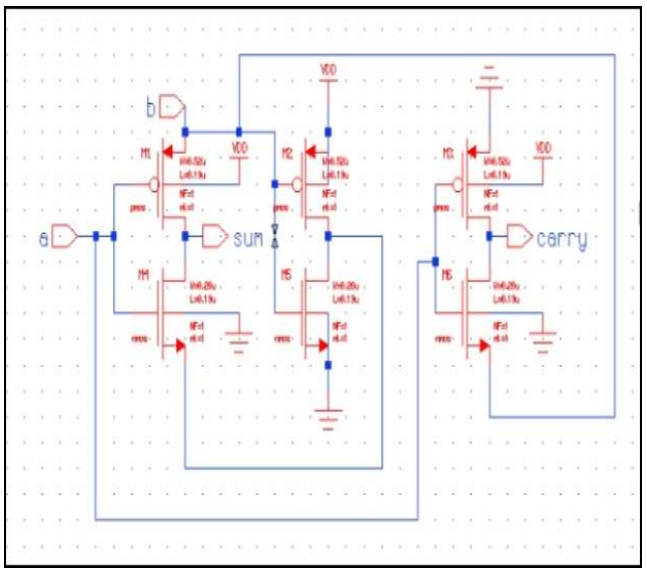

Fig. 4 Half adder circuit using GDI

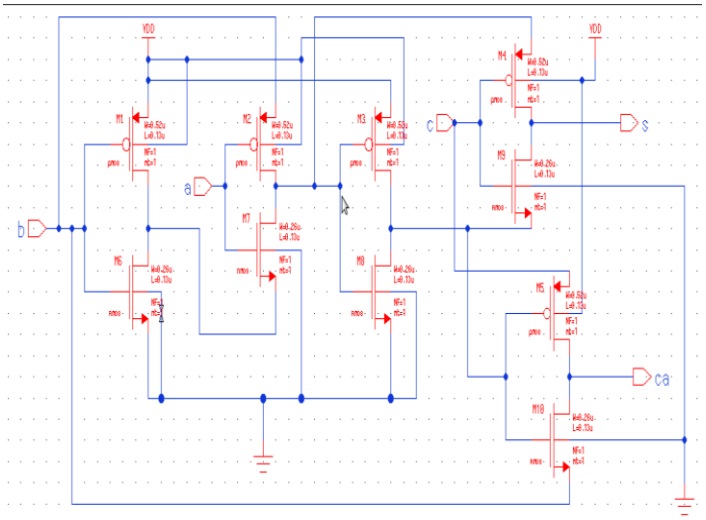

Fig. 5 Full adder circuit using GDI

IV. Performance Comparison

A. Number of transistors

The comparison of number of transistors required for implementing a logical function in CMOS and GDI techniques is shown in table II. It can be observed that the transistor count is less in the case of GDI circuit compared to CMOS thereby, reducing the area occupied by the circuit and also reducing the complexity of the circuit.

TABLE III
Comparison of Transistor Count

FUNCTION	GDI	CMOS
INVERTER	2	2
F1	2	6
F2	2	6
0R	2	6
AND	2	6
MUX	2	14
XOR	4	12
NAND	4	4
NOR	4	4

B. Power dissipation

Table III shows the comparison of power dissipation in both the logics (CMOS and GDI) where the power dissipated by GDI circuit is less than the power dissipated by CMOS circuit.

TABLE IIIII
COMPARISON OF POWER DISSIPATION

FUNCTION	GDI	CMOS
OR	40.8692pW	30.7108nW
AND	21.7801pW	9.7247nW
XOR	14.8807nW	31.2268nW
MUX	1.0306nW	45.6667nW
HALF ADDER	14.9025nW	33.9515nW
FULL ADDER	29.8440nW	98.6144nW

C. Delay

It is evident from the above table (table IV) that the GDI circuit always produces less delay when compared to CMOS circuit. So the propagation speed of the circuit can be increased by designing the circuit in GDI technique.

TABLE IVV
COMPARISON OF DELAY

FUNCTION	GDI	CMOS
OR	40.004ns	40.031ns
AND	20.002ns	40.013ns
XOR	20.010ns	25.050ns
MUX	20.007ns	25.050ns
HALF ADDER	20.010ns	20.013ns
FULL ADDER	12.027ps	72.681ps

V. CONCLUSIONS

The area and delay of 4 bit Braun multiplier using CMOS and GDI logics are evaluated. It is clear from the results that, the proposed multiplier takes less delay and area when compared with CMOS multiplier. It is also observed that in the proposed multiplier the reduction in area is very high with insignificant penalty in the delay when compared with CMOS multiplier.

By implementing Braun multiplier using GDI technology, we can reduce the number of transistors that are used in the design of the multiplier. Thus we can reduce the area of the multiplier. We can also reduce the delay as the number of transistors is less in the proposed multiplier when compared with CMOS multiplier. The power dissipation can also be reduced by implementing the multiplier in GDI technique.

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