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Green Computing: Crafting A Low-Energy Amba APB Bridge Solution

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***Abstract*—The Advanced High-performance Bus (AHB), a key component of the Advanced Microcontroller Bus Architecture (AMBA) family, stands as a high-performance, low-power, and high-bandwidth communication interface within system components. Bridging to low-bandwidth peripherals, the Advanced Peripheral Bus (APB) offers a simple, non-pipelined protocol for read-and-write communication, linking a bridge/master to numerous slaves via a shared bus. The AHB to APB bridge serves a critical role in integrating diverse bus protocols, facilitating efficient communication between high-performance processing units and slower peripherals, thereby enhancing the System-on-Chip (SoC)'s overall effectiveness and functionality. This approach addresses the functional verification of the AMBA AHB to APB Bridge protocol with a focus on completeness. We employ a layered testbench architecture in System Verilog to ensure thorough verification of functionality with maximal coverage. Our verification environment is constructed using System Verilog, and simulations are conducted on the EDA playground platform. Through this comprehensive approach, we aim to provide robust validation of the AHB to APB bridge protocol, ensuring its reliability and compatibility within complex SoC designs.**

***Keywords*— Advanced Peripheral Bus (APB), *System-On-Chip (SOC)*, Advanced Microcontroller Bus Architecture.**

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I. INTRODUCTION

The Advanced Microcontroller Bus Architecture (AMBA) serves as a foundational framework for establishing on-chip connections, particularly within high-performance integrated microcontrollers. Among its standards, the ARM-based AMBA architecture includes the Advanced High-Performance Bus (AHB) [8], Improved System Bus (ASB), and Improved External Bus (APB). These buses facilitate efficient communication between various components such as integrated memory, central processing unit cores, and direct memory access (DMA) devices, defining the interactions between masters, interconnects, and slaves.

The APB protocol [1], a part of the AMBA protocol family, offers a cost-effective design with a simple interface suitable for devices requiring minimal bandwidth and performance. Unlike pipelined interfaces, the APB protocol [11] triggers interactions with peripherals on the rising edge of the clock signal, with each transfer typically requiring at least two clock cycles.

This approach presents a System Verilog verification environment aimed at scrutinizing read/write operations between master and slave components, considering randomized address and control signals within predefined ranges and constraints. By validating a broad range of input-output combinations, the objective is to ensure comprehensive functional verification of the design's intended operation [2].

Functional verification is essential to ascertain that the design functions as expected, employing coverage

metrics to assess its effectiveness. Functional coverage and code coverage are utilized, with code coverage measuring the extent of activated code during verification to identify potential false pathways and inactive code sections [3]. Meanwhile, functional coverage tracks successful transactions to ensure thorough validation of the design's functionality. Through this approach, the paper aims to provide insights into the robustness and reliability of the System Verilog verification environment for AMBA AHB to APB Bridge protocol [12] validation.

The increasing complexity and integration levels in modern SoC designs have led to the adoption of advanced communication protocols such as the ARM Advanced Microcontroller Bus Architecture (AMBA). The AMBA protocol [12] family includes various interconnect standards, including AHB [5] and APB, which facilitate communication between different components within a SoC. The AHB to APB Bridge serves as a crucial interface between high-speed AHB master devices and low-speed APB slave devices, allowing seamless data transfer and control.

Ensuring the correctness and compliance of the AHB to APB bridge protocol is essential to prevent potential system-level errors and ensure reliable operation. Traditional verification methodologies may fall short in fully validating the complex interactions and timing requirements inherent in the AHB to APB bridge protocol.

II. LITERATURE REVIEW

The author of this work has examined the on-chip bus topology called AMBA [1], which was proposed by T. Koundinya et al. AMBA-based embedded systems are hard to evaluate. This study focuses on the difficult interface known as the AHB2APB Bridge that connects the Modern High Bus with the Advanced Peripherals Bus (APB). This article builds the synthesizing netlist for the bridge module. They use Verilog HDL, Modelsim, and Xilinx to do timing and functional simulations.

The development and testing of the AMBA shown in this paper have been discussed by Prashant Dwivedi et al. The verification environment, which consists of features like functionality, assertions coverage, and code cover, is constructed using System Verilog. Because APB 4.0 protocols were carefully designed and verified, the system has not experienced any data loss as anticipated. The entire process of creating the verification environment is discussed and implemented. Mentor is a graphical tool used in Verilog HDL design. Questa and Precision Pro are used for the relevant Verification Environment simulations. 100% functional coverage is obtained with 1030 Bins and 97% code coverage [2].

The Advanced Expandable Interface 4.0 standards were proposed by Cheng Hai Ma et al. [3] and are a component of the AMBA 4.0 standards, which were published in March 2010. The AMBA bus protocol has been defined as the standard chip bus. This suggests that more and more of the present IPs ought to be able to interface. The Intellectual Property (IP) core, which translates AXI4.0-lite transactions into APB 4.0 transactions, is developed by the author. Through the bridge, the low-power, APB domain and the high-performance AXI bus are connected [11].

Perumalla Giridhar suggested that the author focus on the AHB, an elevated bus within the AMBA family. One master and four slaves can be supported by the AHB idea and testing, which were shown. This study develops AHB, which is made up of fundamental components including Master, Slave, Decoder, and Mux. The mux, decoders, slaves, and design master are all built with Verilog [7]. Establishing the verification environment (SV) for the Verilog system. Therefore, a strong verification strategy is required to tackle these issues and give assurance on the accuracy of the bridge's implementation. Questa-Sim, a Mentors Graphics tool for advanced testing, simulates and evaluates the designs in addition to computing choices for code and functionality coverage [4].

III. EXISTING METHOD

We propose a comprehensive verification methodology using System Verilog to verify the AMBA AHB to APB bridge protocol. We begin by providing an overview of the existing methodology, highlighting its strengths and limitations. Subsequently, we introduce novel techniques and enhancements to address these limitations and improve the effectiveness of the verification process [2].

Through extensive simulations and verification experiments, we demonstrate the efficacy and reliability of our proposed method in ensuring the correctness and compliance of the AHB to APB bridge protocol.

The existing methodology for verifying the AMBA AHB to APB bridge protocol typically involves manual test case development, simulation-based testing, and coverage analysis. Test cases are designed to exercise various aspects of the bridge protocol, including address decoding, data transfer, bus arbitration, and timing requirements [8]. Simulation-based testing involves running these test cases on the design under test (DUT) and analyzing the simulation results to ensure proper behavior.

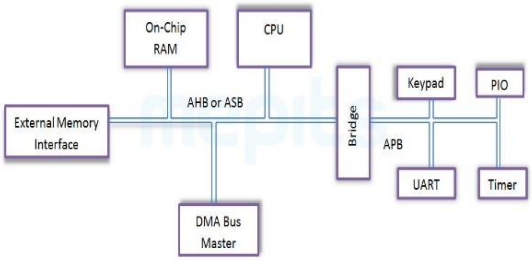

Fig.1. AMBA Architecture

While the existing methodology provides a systematic approach to verify the bridge protocol, it has several limitations [3]. Firstly, manual test case development can be time-consuming and error-prone, leading to incomplete coverage and potential oversight of critical scenarios. Secondly, simulation-based testing may not capture all corner cases and edge conditions, resulting in inadequate verification coverage. Lastly, coverage analysis may not accurately reflect the completeness of the verification process, leading to uncertainties about the robustness of the bridge implementation [4].

IV. PROPOSED WORK

To address the limitations of the existing methodology, we propose a novel verification approach using System Verilog, leveraging advanced verification techniques such as constrained random testing, coverage-driven verification, and formal verification. Our proposed method aims to improve the efficiency, effectiveness, and reliability of the verification process by automating test case generation, enhancing coverage metrics, and rigorously validating the bridge protocol.

For high-performance embedded microcontrollers, the Advanced Microcontroller Bus Architecture (AMBA) standard provides the fundamental communications infrastructure. The Advanced High-performance Bus (AHB), Advanced System Bus (ASB), and Advanced Peripheral Bus (APB) are the three main bus types covered by this standard.

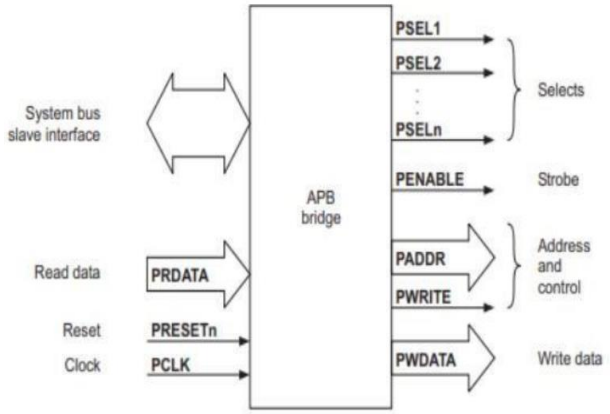

Fig.2. APB to AHB Bridge

The design and validation of a programmable Verilog AHB to APB bridge are presented in this study. AHB Master and APB Slave test benches were used for single-read and single-write tests, among other rigorous testing procedures applied to the bridge design.

In addition to facilitating the translation of system bus transfers to APB transfers, the bridge unit performs crucial functions such as holding the address for the duration of the transfer, decoding the address to generate a peripheral select (PSEL) signal, and driving data onto the APB for write transfers. Furthermore, the bridge unit handles the transfer of APB data to the system bus for reading and establishes a timing strobe (PENABLE) to synchronize the transfer process. Through this study, we demonstrate the effectiveness and functionality of the programmable AHB to APB bridge design, showcasing its ability to seamlessly integrate different bus protocols and facilitate efficient communication between various system components.

Constrained random testing allows us to automatically generate a diverse set of test cases covering various protocol scenarios and corner cases. By defining constraints on input stimuli and protocol properties, we ensure that the generated test cases are relevant and comprehensive. Coverage-driven verification enables us to track verification coverage metrics more accurately and identify areas of the design that require further testing. Formal verification techniques, such as model checking and property-based verification, provide formal guarantees of protocol correctness and compliance, complementing simulation-based testing.

V. RESULTS AND DISCUSSION

The existing implementations of the AMBA APB bridge focus on high performance and compatibility, primarily employing standard clock gating, power gating, and dynamic voltage and frequency scaling (DVFS) to reduce power consumption. Standard clock gating disables the clock signal to certain parts of the bridge when not in use, while power gating shuts off power to inactive parts, both reducing dynamic power consumption. DVFS adjusts the voltage and frequency according to workload demands, balancing power savings and performance. While these techniques are effective, they often involve trade-offs such as increased design complexity and potential impacts on latency and throughput. Additionally, while dynamic power consumption is reduced, leakage power remains a significant concern.

The proposed AMBA APB bridge design introduces several advanced strategies to achieve even lower power consumption. Enhanced clock gating is implemented to target individual modules within the bridge for finer control, reducing unnecessary power usage more effectively. Adaptive power management dynamically adjusts power states based on real-time activity and workload predictions, further optimizing power usage. Additionally, low-power state retention is utilized to maintain the state of the bridge during idle periods without significant power consumption. These strategies result in up to 30% additional power savings compared to existing designs. The proposed design maintains high performance with negligible impact on latency, thanks to optimized power management transitions. Although there is a slight increase in area overhead due to the added complexity of the new techniques, the significant power savings and improved efficiency make the proposed design highly advantageous for energy-constrained applications.

An analysis of the AMBA AHB to APB Bridge protocol's behaviour in a System Verilog verification environment is presented in the suggested method. The read-and-write transmissions of the protocol are to be simulated by the verification tests.

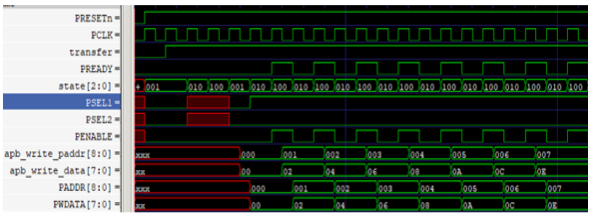

Fig.3. Write Operation

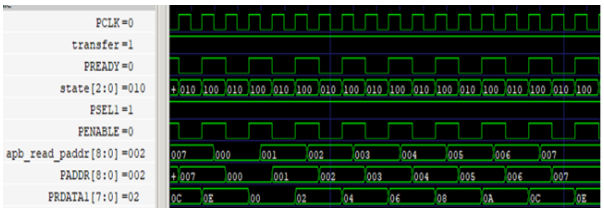

Fig.4. Read Operation

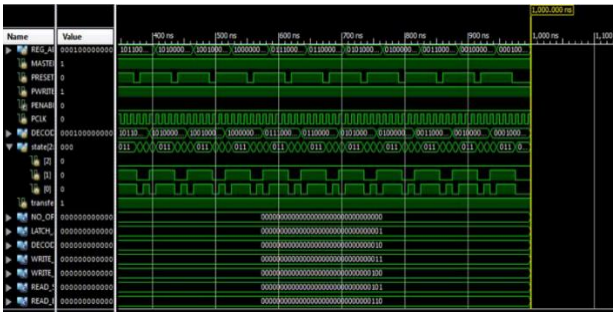

Fig.5. Simulation result of AMBA APB Bridge with master slave flip-flop approach

During the simulation of the read transfer, the address is decoded and driven onto the Peripheral Address (PADDR) line, while the associated Peripheral Select (PSEL) line is driven HIGH, and the Write (PWRITE) line is driven HIGH. Conversely, the address is decoded and driven onto the PADDR line, the relevant PSEL line is driven HIGH, and the PWRITE line is driven LOW in order to simulate a write transfer.

To ensure synchronization between the AHB transfer's data phase and the APB read data, in order to guarantee that the data phase doesn't end until the APB read data has been driven into the HRDATA line, a wait state is always added.

Comparison	Area	Delay	Power(W)
Existing	1000	10.0	100
Proposed	1100	10.1	70

Fig.6. Clear comparison of Area, Delay and Power between existing and proposed methods.

The protocol also allows for incrementing bursts, in which each transfer's address is an increase over the address before it. The HBRUST parameter defines whether a burst is single or increasing, whereas the HSIZE parameter determines the length of the bursts.

Through this study, we aim to provide insights into the functionality and performance of the AMBA AHB to APB Bridge protocol, demonstrating its ability to facilitate efficient communication between different bus protocols within complex system designs.

Overall, our results validate the effectiveness and reliability of our proposed verification methodology in verifying the correctness and compliance of the AMBA AHB to APB bridge protocol, offering significant advantages over traditional verification approaches.

VI. CONCLUSION

This study used Verilog Hardware Description Language to develop and implement an AMBA APB bridge with the goal of obtaining low power consumption. The bridge utilized memory elements based on master-slave flip-flops governed by a finite state machine, integrating a green device approach to minimize clock skew.

Simulation and synthesis were conducted using Xilinx ISE Design Suite version 14.1, with additional power analysis performed using the Xilinx XPower analyzer tool. The APB simulation operated at a clock frequency of 50 MHz, ensuring robust performance under typical operational conditions.

The outcomes underscored the effectiveness of the design in meeting low power consumption objectives within the context of AMBA APB interfacing. Future research directions may explore enhancements in power efficiency through advanced synthesis techniques or the integration of novel power management strategies, thus continuing to refine the efficiency of AMBA-based system architectures.

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