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Grid Power Reduced-Component Multilevel Inverter Modelling and Simulation Improvement of Quality

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Abstract: Compact, efficient, and high-performance power conversion systems that can produce high-quality output power with little harmonic distortion are in high demand due to the growing integration of renewable energy resources into current electrical networks. Although traditional MLI topologies can produce high-quality voltage waveforms, they are notoriously expensive, physically large, control-complicated, and lossy due to the abundance of passive components, isolated DC sources, and semiconductor switches needed. This study models and simulates a reduced-component switched-capacitor multilevel inverter for grid-connected solar applications in order to circumvent these restrictions. In order to synthesise numerous voltage levels with a single DC source and a switched-capacitor voltage boosting network, the suggested topology drastically reduces the number of components without compromising voltage gain or output performance. To simplify the control architecture, we produce the gating signals using a Level-Shifted Pulse Width Modulation (LS-PWM) technique, which allows for stable capacitor voltage balancing and smooth multilevel voltage generation. In addition, an algorithm called Incremental Conductance Maximum Power Point Tracking (IC-MPPT) is used to improve the total conversion efficiency by extracting the most energy possible from the solar source in different climatic conditions.

To study the output voltage properties, quality of the current waveform, stability of the capacitor voltage, dynamic responsiveness, and harmonic performance, the whole system is modelled and tested in the MATLAB/Simulink environment under grid-connected working circumstances. Simulation results show that compared to traditional multilevel inverter structures, the suggested inverter uses fewer power electronic components, improves power quality, boosts voltage more effectively, reduces switching stress, and produces a high-resolution stepped output waveform with reduced Total Harmonic Distortion (THD). Photovoltaic energy conversion and future smart-grid power conditioning applications will benefit greatly from the suggested inverter's simpler control method, enhanced conversion performance, and decreased hardware demand.

Key Words: Switched-capacitor, low components, inrush current limitation, ripple reduction, simple control.

1.INTRODUCTION

The demand for efficient DC-to-AC power conversion technology has skyrocketed due to the rapid expansion of current power electronic systems. Many electrical and electronic devices rely on inverters for various functions. These include renewable energy installations that use photovoltaic modules, battery storage, and fuel-cell technology, air conditioning units, electric vehicle propulsion systems, induction heating equipment, and uninterruptible power supply (UPS) systems. The requirement for inverter topologies that can provide efficient, dependable, high-quality AC power with low harmonic distortion is growing in importance due to the rising penetration of distributed energy resources. Due to its capacity to produce stepped output voltage waveforms that nearly resemble a sinusoidal signal, multilevel inverters (MLIs) have garnered significant interest from researchers and industrial designers among the several power conversion methods. Less total harmonic distortion (THD), less voltage stress on semiconductor devices, better electromagnetic compatibility, and smaller output filter needs are all results of this property. Typical topologies for conventional multilevel inverters, such as Cascaded H-Bridge (CHB), Neutral Point Clamped (NPC), and Flying Capacitor (FC), have proven to be highly effective in applications requiring medium to high power. Nevertheless, the need for multiple power switches, passive components, isolated DC sources, and complex control approaches frequently hinders their practical implementation. This leads to more complicated hardware, higher manufacturing costs, and less reliable systems.

In response to these difficulties, current studies have concentrated on creating more sophisticated multilevel inverter architectures that can simplify the control method, reduce the number of components, and attain high voltage gain. The capacity to generate various voltage levels with a smaller number of independent DC sources and fewer semiconductor devices has led to the rise of hybrid multilevel inverters, modular U-cell (MUC) designs, and switched-capacitor multilevel inverters (SCMLIs) as viable alternatives.

These state-of-the-art topologies are ideal for smart-grid and next-generation renewable energy applications due to their balanced combination of circuit simplicity, voltage

boosting capability, power quality, and overall conversion efficiency.

Because they combine multilevel inverter designs with switched-capacitor networks to provide voltage boosting without using cumbersome magnetic components, switched-capacitor multilevel inverters (SCMLIs) have become a popular choice for high-gain power conversion. By controlling the charging and discharging of capacitors, SCMLIs increase the output voltage without sacrificing circuit compactness, in contrast to traditional boost converters that necessitate big inductors and incur significant switching losses at high operating frequencies. Because of its reduced physical size and improved power density, SCMLIs are well-suited for use in photovoltaic production systems, battery-powered applications, and distributed energy resources thanks to their magnetic-less voltage boosting capacity. In addition, having different voltage levels allows for better voltage self-balancing in the capacitors, which in turn reduces output harmonic distortion and voltage stress on semiconductor devices. This leads to better power quality and more efficient conversions [3,4].

Although subsequent designs decreased the number of components and improved the charging properties of capacitors, the voltage gain was still low—usually approximately twice the input voltage—and the maximum blocking voltage of a number of switches was still very high [6]. There was a marked increase in the number of power switches, leading to greater hardware complexity and higher implementation cost, but higher-level inverter configurations, such as thirteen-level structures, accomplished substantial voltage boosting and lower device stress [7].

To improve device reliability and converter lifetime, the suggested topology meticulously limits the maximum blocking voltage to a small number of switches, reducing voltage stress across semiconductor devices. The necessary switching signals are generated using a modified version of Level-Shifted Pulse Width Modulation (LS-PWM). This method guarantees stable capacitor voltage balancing during steady-state operation and greatly simplifies the gate-driver. In addition, the switched capacitors' charging and discharging sequence is fine-tuned to minimise inrush current, keep voltage levels consistent during the switching cycle, and suppress voltage variations in the capacitors. The power quality, total standing voltage (TSV), harmonic performance, and switching losses are all improved as a result of these upgrades.

2. Proposed Multilevel Converter Topology

The goal of developing the suggested multilayer converter was to simplify the converter construction and achieve high voltage gain with a minimum number of power semiconductor devices. The suggested topology uses an optimised circuit configuration that decreases hardware complexity without sacrificing output performance, in contrast to traditional switched-capacitor multilevel inverters that typically necessitate a multitude of switches, capacitors, and isolated DC sources to produce multiple voltage levels. Renewable energy conversion systems and medium-power applications are ideal for this converter's improved voltage boosting capability, switching efficiency, and capacitor voltage balancing. Figure 5.1 shows the whole circuit configuration of the multilevel converter that has been suggested. Included in the topology are a single DC input source, ten controlled power switches, three power diodes, and four capacitors. The switched-capacitor network's charging current is regulated by connecting an input inductor in series with the DC supply. This inductive element improves converter dependability and reduces electrical stress on the switching devices by efficiently suppressing the inrush current that ordinarily occurs during capacitor charging. This makes the converter more secure to use during startup and other brief periods of operation.

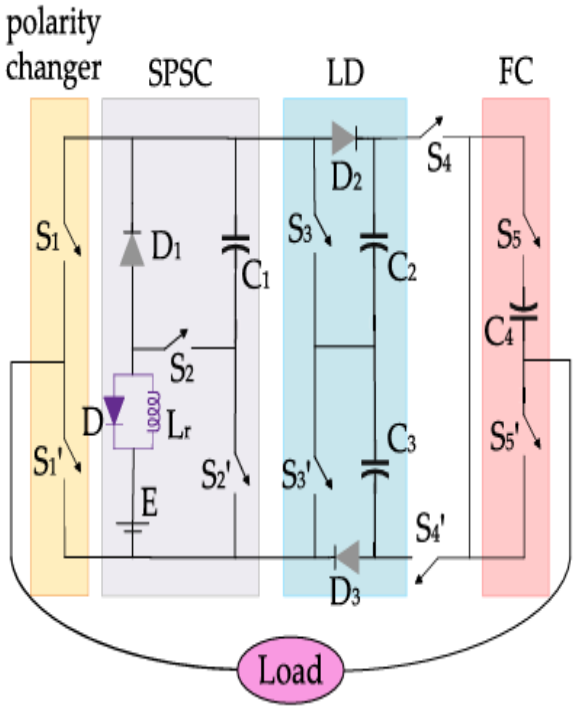


Fig.1 Proposed Multilevel Converter Topology

The Proposed Multilevel Converter's Switching Strategy In order to keep the capacitor voltages steady and produce seventeen different output voltage levels, the suggested multilevel converter makes use of a meticulously planned switching method. The operational sequence is designed such that every switching state helps with controlled charging and discharging of the switched-capacitor network and also contributes to generating voltage levels. The converter is able to accomplish significant voltage gain with fewer semiconductor devices and no extra voltage-balancing circuits because to its coordinated operation.

As shown in Table.1, the suggested topology incorporates a comprehensive switching sequence. The matching capacitor states dictate whether the individual capacitors are charging, discharging, or electrically isolated during that switching interval, while a precise combination of semiconductor switches is used to generate each output voltage level. On the switching table, the letters C, D, and N stand for the three different operating conditions of the capacitors:

charging, discharging, and neutral. In this schematic, the energy transfer process inside the converter's switched-capacitor network is shown clearly.

Table.1 Switching States of the Proposed 17-Level Multilevel Converter

Level	u_o	S_1	S_2	S_3	S_4	S_5	C_1	C_2	C_3	C_4
+8	+4E	1	1	0	0	0	D	C	D	N
+7	+3.5E	1	1	0	0	1	D	C	D	D
+6	+3E	1	0	0	0	0	C	N	D	N
+5	+2.5E	1	0	0	0	1	C	N	D	D
+4	+2E	1	1	1	0	0	D	N	C	N
+4	+2E	0	0	0	0	0	D	C	D	N
+3	+1.5E	1	1	1	0	1	D	N	C	D
+3	+1.5E	0	0	0	0	1	D	C	D	D
+2	+E	0	0	1	0	0	C	N	D	N
+1	+0.5E	0	0	1	0	1	C	N	D	D
0	0	0	1	1	0	0	D	N	C	N
0	0	1	1	0	1	0	D	C	N	N
-1	-0.5E	0	1	1	0	1	D	N	C	C
-2	-E	1	0	0	1	0	C	D	N	N
-3	-1.5E	1	0	0	1	1	C	D	N	C
-4	-2E	0	0	0	1	0	D	C	N	N
-5	-2.5E	0	1	0	1	1	D	C	N	C
-6	-3E	0	0	1	1	0	C	D	N	N
-7	-3.5E	0	0	1	1	1	C	D	N	C
-8	-4E	0	1	1	1	0	D	D	C	N

In order to ensure that the charging and discharging periods of the capacitors are evenly distributed throughout one basic cycle, the switching sequence has been carefully developed. Capacitor voltage ripple is greatly reduced and excessive continuous discharge of any one capacitor is prevented by such a design. So, there's no need for complex closed-loop control algorithms or external balancing circuits, and the capacitor voltages stay near to their intended working values. One notable aspect of the converter that has been suggested is that it can flip between different states for different amounts of output voltage, specifically for +2E, +1.5E, and 0 V. You may achieve the same output voltage by combining multiple switching combinations, which will create different routes for the current to flow through the capacitor. Additional flexibility during converter operation is provided by this redundancy. To improve voltage balance and minimise the longest continuous capacitor discharge interval, the controller can choose the most appropriate switching state based on the capacitor voltage condition.

The operational reliability of the converter is further improved by the availability of redundant switching states. It is possible to select a different switching combination that will produce the same level of output voltage in the event that one switching device becomes inoperable due to a malfunction or unusual operating situation. The suggested architecture is better suited for real-world applications involving the conversion of industrial power and renewable energy sources because of this feature, which enhances converter fault tolerance and increases system availability.

The mitigation of voltage stress across semiconductor devices is an additional critical design factor. Instead of concentrating the blocking voltage on a few devices, the suggested converter uses an optimized switched-capacitor configuration, which means that the voltage is spread out across various switches, diodes, and capacitors. As a result, the majority of the converter switches can be made using semiconductor devices with lower voltage ratings, which improves efficiency, decreases the overall cost of implementation, and reduces switching losses. Table.2 summarises the Maximum Blocking Voltage (MBV) that each component of the proposed converter has experienced. According to the data in the table, the maximum blocking voltage of 4E is applied to just two semiconductor switches, which correspond to the converter's maximum output voltage. There is one set of passive components and switches that function under a blocking voltage of only E, and another set of components that run with a blocking voltage of 2E, including four switches, two power diodes, and two capacitors. The voltage stress applied to the remaining capacitor and switches is 0.5E, which is relatively modest. Improved semiconductor utilisation and increased converter dependability are the result of this uneven blocking voltage distribution.

Table.2 Maximum Blocking Voltage (MBV) Across the Converter Components

C Components	Maximum Blocking Voltage (MBV)
S_4, S_4'	4E
S_1, S_1', S_3, S_3', D_2, D_3, C_2, C_3	2E
S_2, S_2', D_1, C_1	E
S_5, S_5', C_4	0.5E

The operational modes of the proposed converter for both positive and negative half cycles are illustrated in the subsequent Figures. In these operating diagrams, the load current path and the capacitor charging path are represented separately to simplify the understanding of energy transfer within the converter. During every switching interval, electrical energy is simultaneously delivered to the load and redistributed among the switched capacitors according to the selected switching state. This coordinated charging and discharging mechanism enables continuous multilevel voltage generation while maintaining balanced capacitor voltages.

Another important performance parameter used to evaluate multilevel converters is the Average Total Conducting Devices (TCD(_{av})), which represents the average number of semiconductor devices conducting current during one fundamental cycle. Lower values of TCD(*{av}) generally correspond to reduced conduction losses and higher converter efficiency. For the proposed seventeen-level converter, the average number of conducting devices is 8.65, indicating that the topology achieves high-quality multilevel voltage generation while maintaining comparatively low conduction losses.

3.Approach to Modulation

Because of its simplicity, superior harmonic performance, and suitability for multilevel voltage generation, the Level-Shifted Pulse Width Modulation (LS-PWM) technology is used to regulate the seventeen-level multilevel converter that is proposed. With LS-PWM, the available DC-link voltage is better utilised than with traditional sinusoidal PWM methods, and all semiconductor devices are able to maintain balanced switching.

In addition, digital controllers based on FPGAs and DSPs can benefit from the method's accuracy in generating numerous voltage levels while requiring very little processing resources. A low-frequency sinusoidal reference signal and a set of high-frequency triangle carrier signals arranged in a level-shifted configuration are compared in the proposed converter to generate the switching pulses. All seventeen of the output voltage levels are generated by utilising the full modulation range, which is covered by each carrier in their own voltage band. In order to activate the necessary semiconductor switches, the corresponding switching logic changes its working state whenever the reference signal's instantaneous value intersects a specific carrier waveform.

This suggested converter makes use of a full Level-Shifted Pulse Width Modulation (LS-PWM) scheme, as shown in Figure 3. A sinusoidal reference waveform, several carrier signals that have been level-shifted, and the unit that generates the gate signals make up the modulation block. Each power switch receives its own unique set of instructions based on how well they compare to the reference waveform and the carrier signals. To further guarantee safe converter operation and prevent shoot-through scenarios, complementary control signals are automatically generated for the complementary switch pairs in addition to the primary gate pulses.

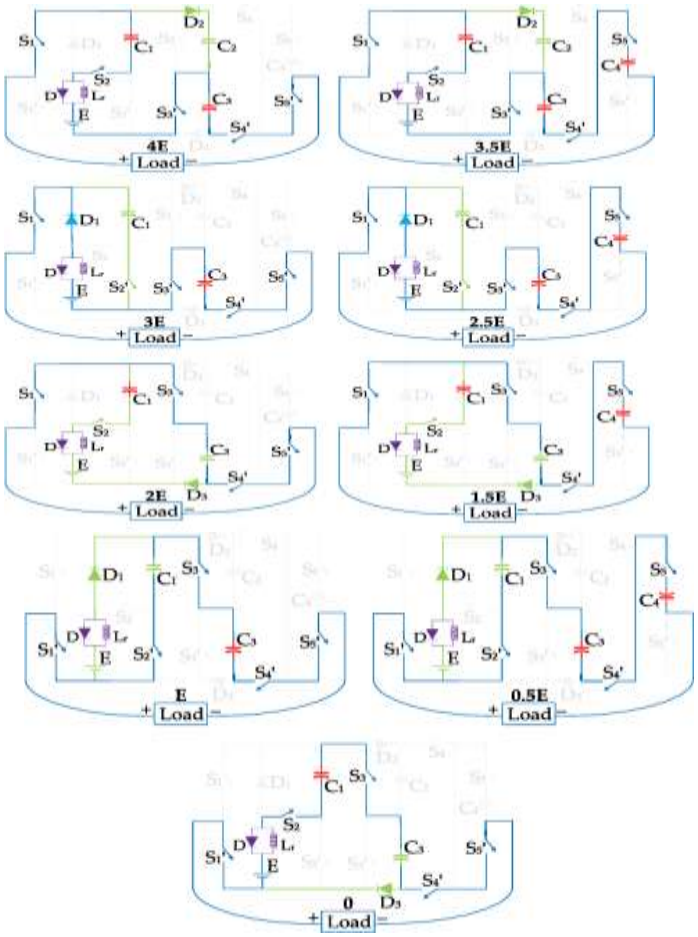


Fig.2 Level-Shifted PWM Technique for the Proposed Multilevel Converter

4.An inrush current limiting inductor

The inrush current that occurs when the capacitors are charging is one of the biggest problems with switched-capacitor multilevel inverters. Whenever the switching state changes or the converter starts up, there can be a big voltage gap between the input and the switched capacitors. At first, the charging route of an uncharged capacitor can carry a very significant transient current because it acts almost like a short circuit. Reduced converter dependability and shortened operational lifetime of the power conversion system can result from improper regulation of this current, which can put undue electrical and thermal stress on semiconductor switches, diodes, capacitors, and PCB interconnections. The suggested converter gets around this issue by charging the switched-capacitor circuit in series with an inrush current limiting inductor. This inductor's principal use is to introduce inductive reactance during capacitor charging in order to control the charging current's rate of change. An inductor's magnetic field momentarily stores energy, which it then transmits to the capacitor network rather than permitting an instantaneous spike of current. As a result, the converter components experience less electrical stress and the charging current grows gradually.

The suggested multilevel converter with the inrush current

limiting circuit illustrated in Figure 5.7 shows the changed configuration. The inductor is linked in series with the switched-capacitor charging loop, ensuring that it is passed through with each capacitor charging period. The regular voltage boosting action of the switched-capacitor network is unaffected by this setup, which successfully restricts the charging current. The outcome is a converter that uses a single passive component to safely charge capacitors while achieving significant voltage gain.

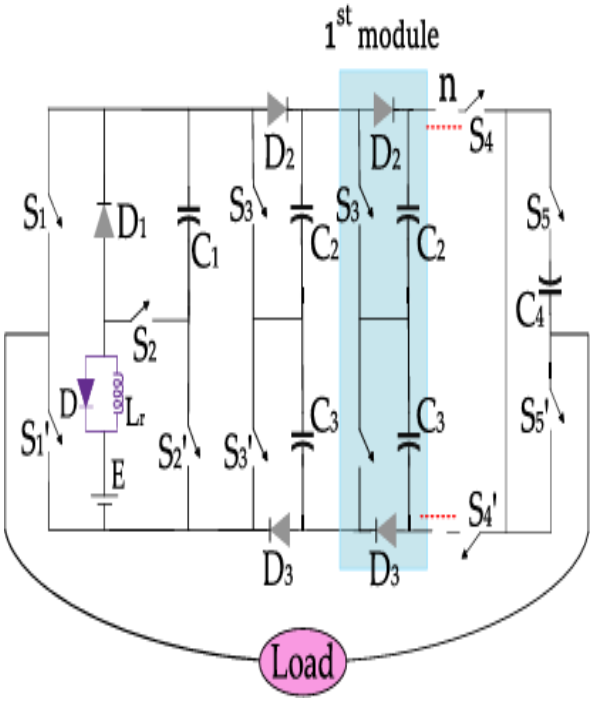


Fig.3.Proposed Multilevel Converter with Inrush Current Limiting Inductor

A reverse-parallel freewheeling diode is placed across the inductor to guarantee that current continues to flow even after the capacitor charging interval. Under typical conditions, this diode's polarity is in opposition to the charging current. The inductor's magnetic energy storage must be securely released when the switching state changes and the capacitor reach the desired voltage. In order to dissipate all of the energy held in the inductor, the current can circulate via an alternate current path provided by the freewheeling diode. To protect semiconductor devices and reduce switching losses, this technique stops high-voltage transients from being generated. The converter's dynamic performance is greatly enhanced when the series inductor and freewheeling diode work together. The inductor counteracts fast current changes during each charging interval, while the diode keeps the current constant during the transition time. Hence, there is less current overshoot and electromagnetic interference caused by fast switching transitions, and the charging process of the capacitor is more consistent.

5.Simulation And Results

5.1 Scenario Model with 17 Levels A comprehensive simulation model was created using the MATLAB/Simulink platform to confirm that the suggested 17-level switched-capacitor multilevel inverter with a single DC source was effective. Power electronic converters' electrical behaviour under varied operating situations can be studied with the help of this simulation environment's adaptable framework. You can test the proposed inverter design's steady-state characteristics, switching performance, voltage boosting capability, and overall operational behaviour with this model before you put it into practice. It faithfully depicts the topology.

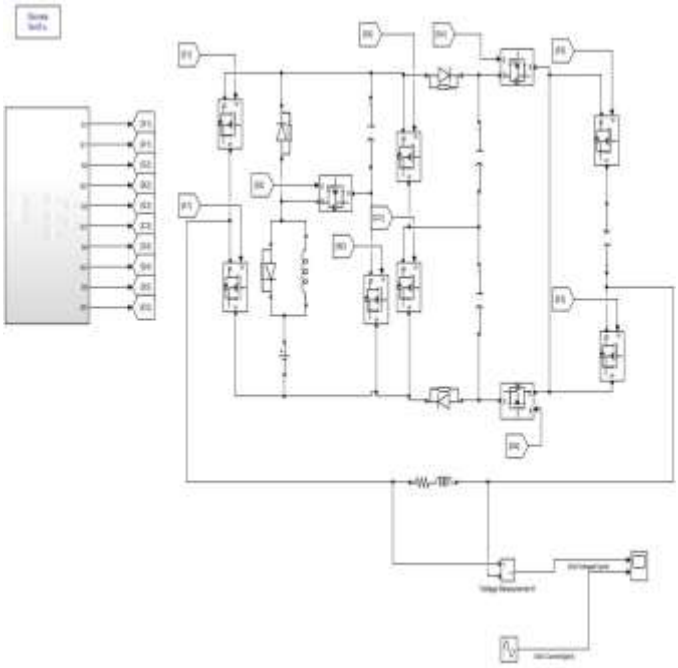


Fig.4.Existing simulation model

A single DC input source, a network of switched-capacitor units, power semiconductor switches, gate-driver circuits, modulation blocks, control logic, and the output load make up the whole simulation model. The interconnections between the subsystems allow for a detailed analysis of the proposed converter's operation, including the switching sequence, multilayer voltage production mechanism, and the charging and discharging behaviour of the capacitors. The proposed multilayer inverter was created for simulation investigations, and its entire MATLAB/Simulink model is shown in Figure 4.

The suggested converter stands out because it can produce seventeen separate voltage levels at the output from a single DC input. The coordinated operation of the switched-capacitor network accomplishes this by charging and discharging the capacitors in accordance with a preset switching sequence. The input source is efficiently coupled with the stored energy in the capacitors to generate a boosted output voltage, doing away with the need for numerous separate DC supply or cumbersome step-up transformers. As a result, the suggested setup keeps the converter's outstanding voltage boosting capacity while reducing circuit complexity, installation cost, and overall size.

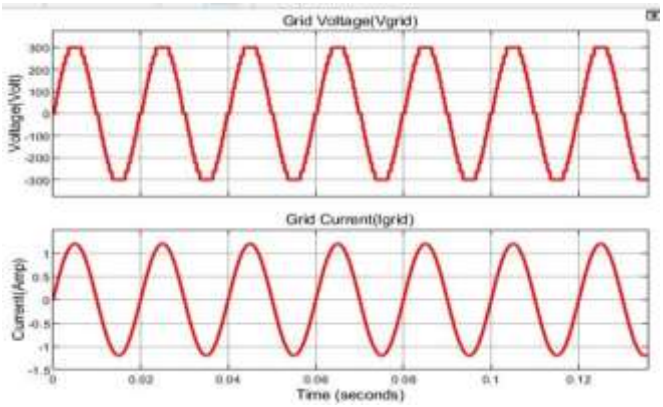
The suggested architecture has fewer semiconductor devices than many traditional multilevel inverter topologies, which is a major benefit. The reduced number of power switches and related gate-driver circuits allows for a smaller and simpler converter design. Reduced manufacturing cost, greater reliability, and decreased switching losses are all benefits of the simpler hardware architecture that do not compromise the quality of the produced multilayer output voltage. The suggested converter uses the Level-Shifted Pulse Width Modulation (LS-PWM) method to guarantee accurate operation of the semiconductor switches.

This method of modulation involves continually comparing a sinusoidal reference waveform with a number of vertically shifted high-frequency carrier signals. In order to generate voltage levels accurately throughout the positive and negative half cycles of the output waveform, these comparisons are used to generate the appropriate gate pulses for each semiconductor switch. The suggested inverter gains numerous performance benefits by using the LS-PWM approach. It allows the semiconductor devices to distribute switching operations uniformly, greatly minimises output voltage harmonic distortion, and helps keep capacitor voltages balanced during continuous operation. In addition to enhancing waveform quality and decreasing switching stress on power devices, the modulation technique guarantees smooth transitions between neighbouring voltage levels. Consequently, the suggested converter is ideal for medium-power applications and renewable energy conversion due to its increased conversion efficiency, less switching losses, better voltage regulation, and stable performance under steady-state conditions.

In contrast, the proposed converter achieves seventeen output voltage levels using only a single DC voltage source, ten power semiconductor switches, and four switched capacitors, thereby providing a simpler and more compact hardware implementation. Despite the reduced number of components, the converter maintains excellent output voltage quality and achieves a Total Harmonic Distortion (THD) of only 2.81%, indicating a significant improvement over many conventional multilevel inverter configurations. These results confirm that the proposed topology successfully combines high voltage boosting capability with efficient component utilization while maintaining low harmonic distortion and reduced converter complexity. Consequently, the proposed design represents an effective solution for renewable energy conversion systems where compact size, high efficiency, and low implementation cost are essential design requirements.

As shown in Figure 6, the suggested inverter's simulated waveforms for output voltage and load current are displayed. The output voltage has seventeen separate levels, giving it a staircase waveform that is very similar to a perfect sinusoidal waveform. Reducing the voltage step size between consecutive levels, the increasing number of voltage levels greatly enhances the waveform quality. Consequently, the power quality that is given to the load is improved, and the harmonic content of the output voltage is significantly lower compared to traditional two-level and lower-level multilevel inverters. The inductive properties of the linked load cause the matching load current waveform to take on a nearly sinusoidal shape. Because the load impedance efficiently attenuates the high-frequency harmonic components in the stepped output voltage, the current waveform is smooth. Level-Shifted Pulse Width Modulation (LS-PWM) and the switched-capacitor network work together to keep capacitor voltages balanced and guarantee constant voltage generation during the whole operating cycle. So, the simulation results show that the suggested converter can produce high-quality AC output with less harmonic distortion, better voltage regulation, and dependable capacitor voltage balancing, and they also confirm that it operates steadily under steady-state settings.

Fig. 5. Existing 17-Level load voltage and current



Level-Shifted Pulse Width Modulation (LS-PWM) is the method used to generate the switching pulses needed by the current 17-level switched-capacitor multilevel inverter. This method of modulation makes use of a sinusoidal reference waveform at a low frequency (V_{ref}) in conjunction with several triangular carrier signals at a high frequency (V_{car}) that are vertically shifted. In order to find the right switching intervals for the semiconductor devices, the reference waveform is constantly compared with each carrier signal.

The final gate-driving pulses for the power switches M_1-M_5 and their corresponding complementary switches M_1'-M_5' are generated from a series of intermediate logic signals that are produced by the comparison process. These signals are then processed using OR logic gates. To avoid shoot-through situations and increase the inverter's overall reliability, the complementary switching design makes sure that only the necessary semiconductor components conduct throughout each working interval. The switched-capacitor charging and discharging processes are also precisely coordinated by the applied LS-PWM control scheme. The converter is able to produce the necessary multilayer output voltage while keeping the capacitor voltages steady because the switching sequence is synchronised with the modulation signals. This ensures that the capacitor network functions in a controlled manner during each fundamental cycle. Overall, the gate-drive circuitry is simplified, switching losses are reduced, and the number of needless switching transitions is reduced by this coordinated switching technique. The inverter's output voltage, seen in Figure 6 as a well-defined 17-level staircase, is very near to a sinusoidal waveform. The smooth profile of the corresponding load current is due to the fact that the inductive nature of the load effectively filters out the components involved in high-frequency switching. So, the inverter guarantees stable functioning of the switched-capacitor network and improves the quality of the output voltage with reduced harmonic

distortion. These findings demonstrate that the LS-PWM method is capable of producing efficient switching control with a minimum of effort required for implementation.

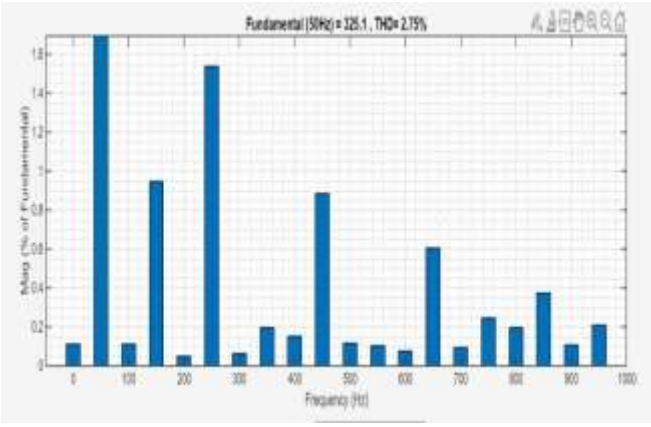


Figure 6. Total Harmonic Distortion (THD) Analysis of the 17-Level Proposed Inverter

A Total Harmonic Distortion (THD) study was performed using the Fast Fourier Transform (FFT) tool available in the MATLAB/Simulink environment to evaluate the output power quality of the proposed multilevel inverter. Analysing the inverter's output voltage using fast Fourier transform (FFT) allows one to quantify waveform distortion by separating it into its fundamental and harmonic frequency components. Figure.7. displays the matching harmonic spectrum that was derived from the simulation. As a measure of the proportion of harmonic components in the output waveform compared to the fundamental frequency component, Total Harmonic Distortion is a commonly used performance metric for power electronic converters. Power quality, electrical losses, electromagnetic interference, and compatibility with sensitive electrical equipment are all improved when the THD value is low, meaning the output voltage is closer to an ideal sinusoidal waveform. For this reason, reducing total harmonic distortion (THD) is a primary goal of contemporary multilevel inverter systems, especially for use with renewable energy sources and in conjunction with the grid. Confirming the converter's outstanding harmonic performance, the FFT study of the suggested inverter shows that the output voltage attains a THD value of just 2.81%. Producing an output waveform that closely resembles a sinusoidal waveform and generating seventeen separate voltage levels are the primary factors responsible for the low distortion level. In addition, the Level-Shifted Pulse Width Modulation (LS-PWM) method is used to accurately switch the semiconductor devices, which reduces the presence of lower-order harmonic components and improves the quality of the waveform as a whole.

There are a number of real-world benefits to the suggested topology's lower harmonic content. Convertor size, cost, and power losses are all reduced since there are less harmonic components in the output voltage, which means that bulky output filters aren't needed as much. Better waveform quality also improves converter efficiency, reduces heating impacts on linked electrical equipment, and makes it easier to comply with harmonic criteria that renewable energy systems that are connected to the grid must meet.

High voltage gain, low harmonic distortion, decreased component count, and outstanding output voltage quality are all achieved by the suggested switched-capacitor multilevel inverter, as shown in the simulation results. The efficiency of the switched-capacitor voltage boosting mechanism and the LS-PWM control approach are both confirmed by the achieved THD value of 2.81%. These findings validate the proposed inverter's ability to provide consistent, high-quality AC power under steady-state circumstances while keeping operations efficient and dependable.

The obtained simulation results show that the proposed converter is suitable for grid-connected power electronic applications, distributed generation networks, photovoltaic energy conversion systems, and battery energy storage units. These applications require compact converter architecture, high conversion efficiency, and superior power quality

6. CONCLUSION

This study detailed the planning, modelling, and testing of a 17-level switched-capacitor multilevel inverter for use in PV energy conversion systems that are connected to the grid. The goal of developing this converter was to reduce the number of power electronic components needed for conventional multilevel inverter topologies while still generating a high-quality AC output. A single DC input source and an optimised switched-capacitor network allowed the converter to produce seventeen different voltage levels from a small circuit. Hardware implementation was simplified without sacrificing efficiency in voltage boosting due to the reduced number of semiconductor switches, capacitors, and gate-driving signals. In addition, the Level-Shifted Pulse Width Modulation (LS-PWM) technique was used to achieve accurate switching control and inherent capacitor voltage balancing without the need for extra balancing circuits. An inrush current limiting inductor was also included to reduce charging current to a minimum and improve the converter's overall reliability.

The steady-state operational properties of the proposed converter were verified by analysis in the MATLAB/Simulink environment, which was used for effective implementation. The simulation results showed that the system was stable, with an output voltage that followed a well-defined 17-level staircase and a waveform for the load current that was almost sinusoidal. With a straightforward circuit design, the converter increased the input voltage from 75 V to about 300 V, a voltage gain of four. A Total Harmonic Distortion (THD) of 2.81% was verified by the FFT analysis, which means that the output waveform is of outstanding quality and meets the power quality criteria of renewable energy applications. Furthermore, the converter demonstrated little power loss during switching, decreased voltage stress on semiconductor devices, and effective balancing of capacitor voltages during operation. Based on these findings, the suggested

topology is an attractive option for small and inexpensive grid-connected photovoltaic power conversion systems since it strikes a good balance between high voltage gain, low harmonic distortion, reduced component count, and simplified control.

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