

Hybrid Logic Circuit-based one-bit Full-Adder for Energy-Efficient DSP Applications

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Abstract— This study offers revolutionary 24-transistors (24T), 1-bit 'full-adder' (FA) for energy-efficient DSP applications. A hybrid XNOR circuit is used to create the proposed 1-bit FA. The hybrid XNOR circuit is built utilising the GDI (gate-diffusion-input) technology, TG (transmission gate), and SCMOS (static CMOS) logic. To evaluate the proposed FA's performance, 'Design Metrics' (DMs) such as power, delay, 'power-delay-product' (PDP), and area are compared to state-of-the-art FAs. All of the FAs under examination were built and simulated under common 'process-voltage-temperature' (PVT) conditions for a fair comparison.

The Cadences' Spectre software was used to run the simulations. Using a 45 nm 'predictive-technology-model' as a simulator (PTM). At an input signal frequency of 200 MHz and a supply voltage of 1 V, simulations show that the suggested FA wastes an average power of 1.284 W. It has a power-delay-product (PDP) of 0.156 fJ and a worst-case delay of 122 ps..

Keywords—full adder, PDP, low power, static CMOS, gate-diffusion-input, transmission-gate-logic

I. INTRODUCTION

The next generation of battery-powered portable electronic devices will have to process a massive amount of computationally intensive data for multimedia applications [1]. These apps cover a wide range of topics, including audio, video, and image processing. All of these technologies have the same requirement: to extend battery life by lowering power dissipation per bit of action executed. This necessitates the development of low-power, high-speed arithmetic systems. The 'Digital-Signal-Processing' (DSP) blocks are commonly used as a core in arithmetic systems that handle these multimedia applications [2], [3], [7]. In these systems, the most basic arithmetic operation is addition, and the adder circuit, as a vital part, plays an important role in determining the overall correctness and performance of the system. As a result, many academics are interested in the design and improvement of adder circuits with improved performance in the context of DSP.

Figure 1 depicts a generic block diagram of FA. It features three inputs: A, B, and Cin, as well as two outputs: Sum and Cout. Table I shows the truth table for 1-bit FA. The logic equations for Figure 1's output are as follows: [21].

$$Sum = A \oplus B \oplus C_{in} \quad (1a)$$

$$C_{out} = A \cdot B + B \cdot C_{in} + A \cdot C_{in} \quad (1b)$$

The outputs *Sum* and *C_{out}* of FA can also be expressed in different forms. Based on how the output *Sum* is expressed, the

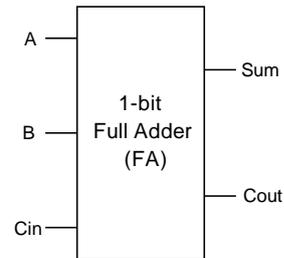


Fig. 1. Block Diagram of 1-bit FA

Inputs			Outputs	
A	B	C _{in}	Sum	C _{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

TABLE I
TRUTH TABLE OF 1-BIT FA

architectures are classified into XOR-XOR, XNOR-XNOR, XOR-XNOR, and Alternative-Logic (AL) based FAs. The block diagram and their respective output equations are listed as below.

- XOR-XOR based FA [13]: Here the *Sum* is implemented using two XOR gates and *C_{out}* using a single a 2 × 1 Mux herein called as *C_{out}*-Mux (C-Mux). The logic expressions of outputs of Figure 2 is listed in the Equation 2.

$$Sum = H \oplus C_{in} \quad (2a)$$

$$C_{out} = A \cdot H + C_{in} \cdot H \quad (2b)$$

- XNOR-XNOR based FA [13]: The diagram of this Full Adder architecture is shown in the Figure 3, here the *Sum* is implemented using two XNOR gates and *C_{out}* using a C-Mux. The logic expressions of outputs are listed in the Equation 3.

$$Sum = \overline{H \oplus C_{in}} \quad (3a)$$

$$C_{out} = A \cdot H + C_{in} \cdot H \quad (3b)$$

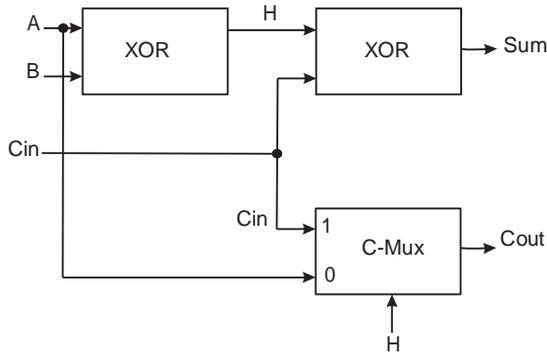


Fig. 2. Block diagram of XOR-XOR based FA

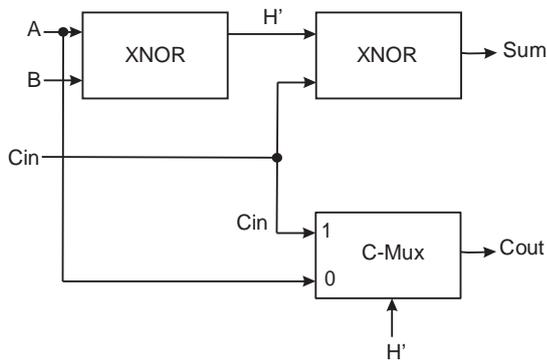


Fig. 3. Block diagram of XNOR-XNOR based FA

- XOR-XNOR based FA [13]: The diagrammatic representation of this Full Adder architecture is shown in the Figure 4, here the sum is obtained using XOR/XNOR gates and using a Sum Mux (S-Mux). The C_{out} is obtained using XOR/XNOR gates and using a C-Mux. The logic expressions of outputs are listed in the Equation 4.

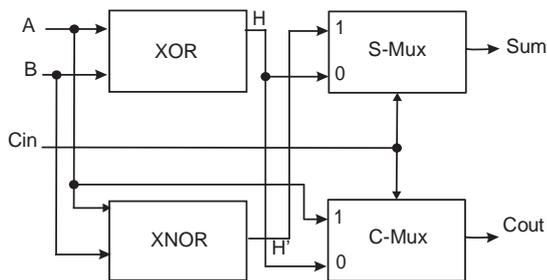


Fig. 4. Block diagram of XOR-XNOR based FA

$$Sum = H \cdot \overline{C_{in}} + C_{in} \cdot \overline{H} \quad (4a)$$

$$C_{out} = A \cdot \overline{H} + C_{in} \cdot H \quad (4b)$$

- AL based FA [10]: The diagrammatic representation of AL FA architecture is given in the Figure 5, here the Sum is realized using XOR/XNOR gates and SMux. The C_{out} is realized using AND/OR gates and CMux. The logic expressions of outputs are shown in the Equation 5. Where $G=A \cdot B$ and $P= A + B$.

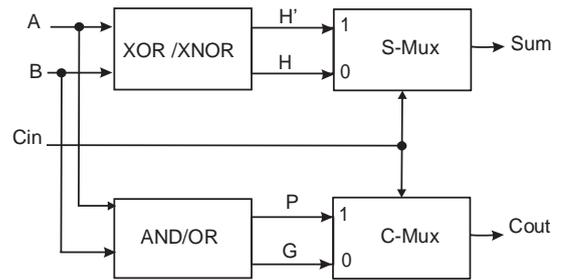


Fig. 5. Block diagram of AL based FA

$$Sum = H \cdot \overline{C_{in}} + C_{in} \cdot \overline{H} \quad (5a)$$

$$C_{out} = G \cdot C_{in} + C_{in} \cdot P \quad (5b)$$

The state-of-the-art is aimed on optimization of Power Delay Product and circuit complexity of Full Adder in terms of 'transistor count' (TC). The optimization of Full Adder in the Power Delay Product and TC space can be achieved through the exploration of best features of various types of logic structures. Most of the energy-efficient FAs have been designed by combining the best features of conventional logic styles such as static complementary metal oxide semiconductor (SCMOS), transmission gate (TG), and pass-transistor (PT) [21], [22]. The conventional 28-T CMOS SCMOS [21] is used to develop the adder. TG logic is used to design the TG [14] and 'transmission function' [11], [12] FAs. TG and TF FAs each require 20 and 16 transistors, respectively. The PT-based FA described in [20] uses a total of 38-T and is built with 'complementary PT logic' (CPL). All of the other adders mentioned [3], [5]–[16], [19] were created with a mix of SCMOS, TG, and PT logic. Rest of this paper is organized as follows. Section-II details about proposed FA circuit. Section-III presents about the test bench and simulation environment. Section-IV discusses about simulation results and discussion. Section-V concludes this paper.

II. PROPOSED 1-BIT FULL ADDER CIRCUIT

The schematic of proposed novel 1-bit FA is shown in Figure 7. It is derived based on the Equation 1 and Table I. The Sum and C_{out} are given by $Sum = H \cdot \overline{C_{in}} + \overline{H} \cdot C_{in}$ and $C_{out} = A \cdot \overline{H} + C_{in} \cdot H$. Where $H = A \oplus B$ and $\overline{H} = A \oplus \overline{B}$ represents XOR and XNOR logical operations respectively. A unique XNOR circuit is the critical component of the suggested FA. Figure 6 shows the suggested XNOR circuit, which was created utilising the GDI approach [4], SCMOS, and TG logic. The full swing rail-to-rail outputs are a unique characteristic of this XNOR gate. When B=1, H =Strong '0' if A=0' and Strong '1' if A=1', as shown in Figure 6. H =Strong '0' if A=1' and Strong '1' if A=0' when B=0'. Table II summarises the same information. As a result, depending on the input signal circumstances, the XNOR circuit always passes either a strong '0' or a strong '1'. After that, the H signal is inverted to get the \overline{H} (XOR operation). We simply need 14T to implement XNOR and XOR using GDI, SCMOS, and TG topologies. Further, an additional two multiplexers are required

B	A	\overline{H}	H
0	0	1	0
0	1	0	1
1	0	0	1
1	1	1	0

TABLE II
FUNCTIONAL TABLE OF PROPOSED HYBRID XNOR CIRCUIT

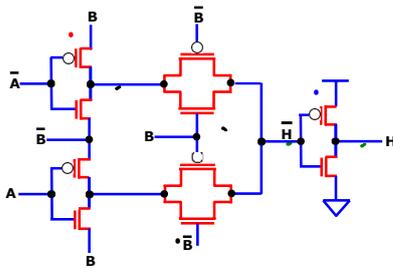


Fig. 6. Schematic of Proposed XNOR circuit

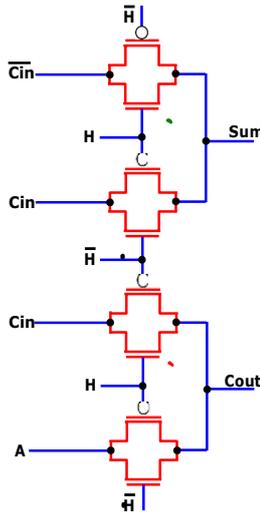


Fig. 7. Schematic of Proposed 1-bit FA circuit

to implement the Sum and C_{out} . These multiplexers need only 10T using TG logic. Thus a total of 24T are required to implement the proposed novel 1-bit FA.

A. Transistor Sizing

For a fair comparison of proposed FA along with other reported adders, all FA schematics under consideration was designed using PTM 45 nm technology node [23] with minimal transistor channel length, $L_{min} = 45 \text{ nm}$ and width, $W_{min} = 90 \text{ nm}$. Accordingly the ‘aspect ratio’ (AR) for n-channel MOSFET (NMOS) is chosen as $(\frac{W}{L})_n = \frac{90 \text{ nm}}{45 \text{ nm}}$ and p-channel MOSFET (PMOS) as $(\frac{W}{L})_p = 2 \times (\frac{W}{L})_n = \frac{180 \text{ nm}}{45 \text{ nm}}$.

III. TEST BENCH AND SIMULATION ENVIRONMENT

To evaluate and comparing the DMs of the proposed Full Adder with respect to other adders, a common test bench shown in the Figure 8 [5], [6], [13] is used. The figure has ‘circuit-under- test’ (CUT), input buffers and output load capacitance. The

CUT is the Full Adder under test, for which the DMs need to be extracted. At the input side of CUT, the buffers with the specified AR are used. With this buffers the CUT undergoes the required signal distortion. Thus mimicking the real situation, while operating in a system. At the output, a load capacitance of 6 fF, equivalent to four ‘fan-out inverters’ (FO4) is used.

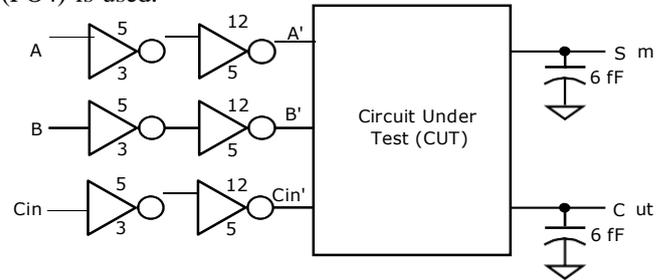


Fig. 8. Test bench to extract DMs of Proposed and reported FAs

To extract the average power and worst case delay the standard test input patterns as suggested in [18] are used. The average power, P_{avg} , is the sum of two components, given as:

$$P_{avg} = P_{static} + P_{dynamic} \quad (6a)$$

$$P_{dynamic} = P_{switching} + P_{short\ circuit} \quad (6b)$$

P_{static} refers to the static power loss caused by reverse bias leakage between diffusion zones and the substrate. When the input switches from logic-0 (or logic-1) to logic-1, the $P_{dynamic}$ is the power loss (or logic-0). $P_{dynamic}$ also includes two components: $P_{switching}$ and $P_{short\ circuit}$. The power loss caused by switching all of the node capacitances is known as $P_{switching}$. The $P_{short\ circuit}$ is the power loss over the entire circuit caused by n-channel and p-channel MOSFETs linked between the power supply rails conducting at the same time.

To extract the P_{avg} , the input signals with variable frequency combinations are applied at the three inputs of a CUT. The frequency patterns or combinations (f_{in}) for input signals are selected in such a way that it should include high frequency (f_h), medium frequency (f_m), and low frequency (f_l) signals. The P_{avg} of all the 12, 1-bit FAs under consideration is determined as the average power dissipated over 9 input frequency patterns (see Table III), applied at the 3 inputs resulting in a valid logic levels at the outputs. The frequencies for the inputs A, B, and C_{in} , are labeled as f_A , f_B , and f_{Cin} respectively. In Table III the first 6 frequency patterns are combinations of three frequencies: f_l , f_m , and f_h . And the last 3 rows of this table are combinations of frequencies: f_l , f_m , f_{md} and f_h . The f_{md} is the delayed version of input signal frequency f_m . The worst-case power loss owing to glitches will be effectively simulated by the last three rows of frequency patterns. The waveform of Figure 9 shows the worst-case glitches that result. Figure 9 shows all nine frequency patterns applied to the test bench's three inputs, as well as the corresponding waveforms at the Sum and Cout outputs. The Piece Wise Linear (PWL) feature in Cadences' Virtuoso tool is used to automatically produce all of these frequency combinations.

Frequency Patterns			
Sl. No	f_A	f_B	f_{Cin}
1	f_h	f_m	f_l
2	f_h	f_l	f_m
3	f_m	f_l	f_h
4	f_m	f_h	f_l
5	f_l	f_h	f_m
6	f_l	f_m	f_h
7	f_m	f_{md}	f_l
8	f_m	f_{md}	f_m
9	f_m	f_{md}	f_h

TABLE III

STANDARD INPUT PATTERNS USED TO MEASURE THE AVERAGE POWER

The f_{in} is thus, a concatenation of three different frequencies, where f_{in} represents the input signal frequency of either ‘A’ or ‘B’ or ‘ C_{in} ’ inputs. The number of frequency combinations used is 9 as suggested in [18]. In this research the values of f_h , f_m , and f_l are chosen as 200 MHz, 100 MHz, and 50 MHz respectively with $V_{dd}=1$ V. Thus the average power of a CUT is, the power dissipated over aforementioned combinations of frequencies. The simulated waveforms to extract the average power of the proposed 1-bit FA is shown in the Figure 9.

The propagation delay (tpd) is defined as the period between a 50% change in input signal while switching from 0 to 1 or 1 to 0 logic levels, and a corresponding 50% change in output signals, again moving from 0 to 1 or 1 to 0 logic levels. There are $2^3 = 8$ potential input vectors for a 1-bit FA with three inputs: A, B, and C_{in} . We must consider all possible input vector to vector transitions for an exhaustive delay analysis for Sum or C_{out} . For $k=3$ inputs, there are $2^k \times 2^k = 64$ possible input vector transitions, presented in the form of a $2^k \times 2^k$ matrix herein referred to as a delay matrix; the template of the output-Sum delay matrix is shown in the diagram. Table IV. The extracted delays for a 1-bit FA at its output-Sum is entered as an element in this matrix consisting 64 cells. The 8 diagonal cells out of 64 in the delay matrix, correspond to transition within the same input states for e.g., 000 → 000, 001 → 001, ..., 111 → 111 transitions (where the arrow indicating the direction of state transition), have no physical significance and are indicated by a *. Further 24 out of remaining 56 (64-8) state transitions will not cause any state change at Sum output and are labeled as Not Applicable (NA). All the 56 input vector transitions are defined as standard input test patterns to determine the worst case delay in Sum as shown in waveforms of Figure 10. These input vector transitions are generated automatically using PWL function to generate 200 MHz signal for transient simulation. Collectively, these waveforms on A, B, and C_{in} inputs have all the 56 input vector-to-vector transitions implicit in them. The delay extracted at the output—Sum constitutes the critical path (in an adder chain). Further, a total of $32 (= 56 - 24)$ delays (t_{pd1} to t_{pd32}) at Sum, corresponding to the 32 significant transitions on 3 input vector A, B, C_{in} have been simulated, extracted, and tabulated in the respective cell in Table V. Similarly the

A B C_{in}	000	001	010	011	100	101	110	111
0 0 0	*	t_{pd1}	t_{pd2}	NA	t_{pd3}	NA	NA	t_{pd4}
0 0 1	t_{pd5}	*	NA	t_{pd6}	NA	t_{pd7}	t_{pd8}	NA
0 1 0	t_{pd9}	NA	*	t_{pd10}	NA	t_{pd11}	t_{pd12}	NA
0 1 1	NA	t_{pd13}	t_{pd14}	*	t_{pd15}	NA	NA	t_{pd16}
1 0 0	t_{pd17}	NA	NA	t_{pd18}	*	t_{pd19}	t_{pd20}	NA
1 0 1	NA	t_{pd21}	t_{pd22}	NA	t_{pd23}	*	NA	t_{pd24}
1 1 0	NA	t_{pd25}	t_{pd26}	NA	t_{pd27}	NA	*	t_{pd28}
1 1 1	t_{pd29}	NA	NA	t_{pd30}	NA	t_{pd31}	t_{pd32}	*

TABLE IV

EXTRACTED DELAY OF PROPOSED ADDER AT OUTPUT, Sum

A B C_{in}	000	001	010	011	100	101	110	111
0 0 0	*	30	107	NA	97	NA	NA	28
0 0 1	30	*	NA	92	NA	80	31	NA
0 1 0	89	NA	*	62	NA	111	71	NA
0 1 1	NA	97	79	*	97	NA	NA	76
1 0 0	81	NA	NA	122	*	62	65	NA
1 0 1	NA	89	117	NA	80	*	NA	70
1 1 0	NA	79	110	NA	100	NA	*	32
1 1 1	40	NA	NA	88	NA	77	30	*

TABLE V

EXTRACTED DELAY OF PROPOSED ADDER AT OUTPUT, Sum

effective 32-delays at the output- C_{out} is also extracted and tabulated in the Table VI. The maximum delays in each of the delay matrix is highlighted with larger and bold font. The worst case delay is then considered as the maximum delay among Sum and C_{out} .

Using the input patterns depicted in Figures 9 and 10, the product of average power and worst case delay is extracted to obtain the power delay product (PDP). This section has already covered the extraction of the worst case delay and the average power. Traditionally, the PDP has been seen to be a good performance parameter for optimising power and delay at the same time. The power dissipation in long channel transistors is primarily due to the switching of node capacitances in the circuits, where the leakage power dissipation was rather high. The overall leakage power dissipation due to all leakage mechanisms, such as subthreshold, junction, and carrier tunnelling through oxide, becomes equivalent with dynamic power dissipation in sub-45 nm gate lengths.

A B C_{in}	000	001	010	011	100	101	110	111
0 0 0	*	NA	NA	78	NA	40	30	28
0 0 1	NA	*	NA	79	NA	41	77	31
0 1 0	NA	NA	*	34	NA	91	76	57
0 1 1	29	92	30	*	32	NA	NA	NA
1 0 0	NA	NA	NA	109	*	34	70	57
1 0 1	31	83	34	NA	30	*	NA	NA
1 1 0	37	39	51	NA	60	NA	*	NA
1 1 1	40	38	51	NA	60	NA	NA	*

TABLE VI

EXTRACTED DELAY OF PROPOSED ADDER AT OUTPUT, C_{out}

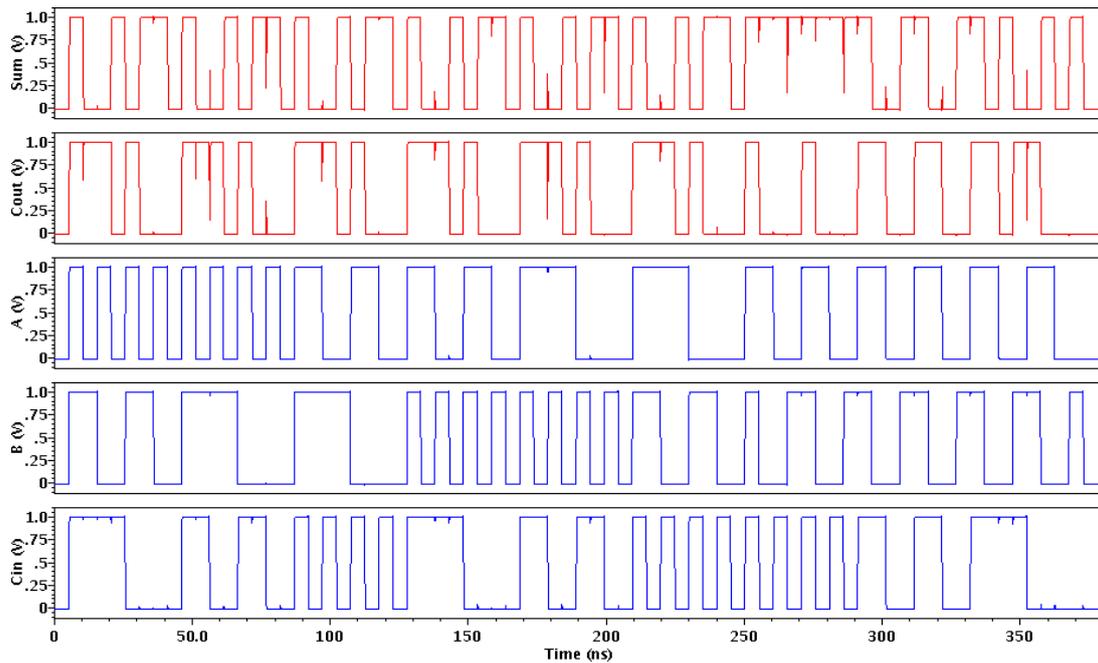


Fig. 9. Simulation Waveforms of Proposed 1-bit FA circuit to extract Power

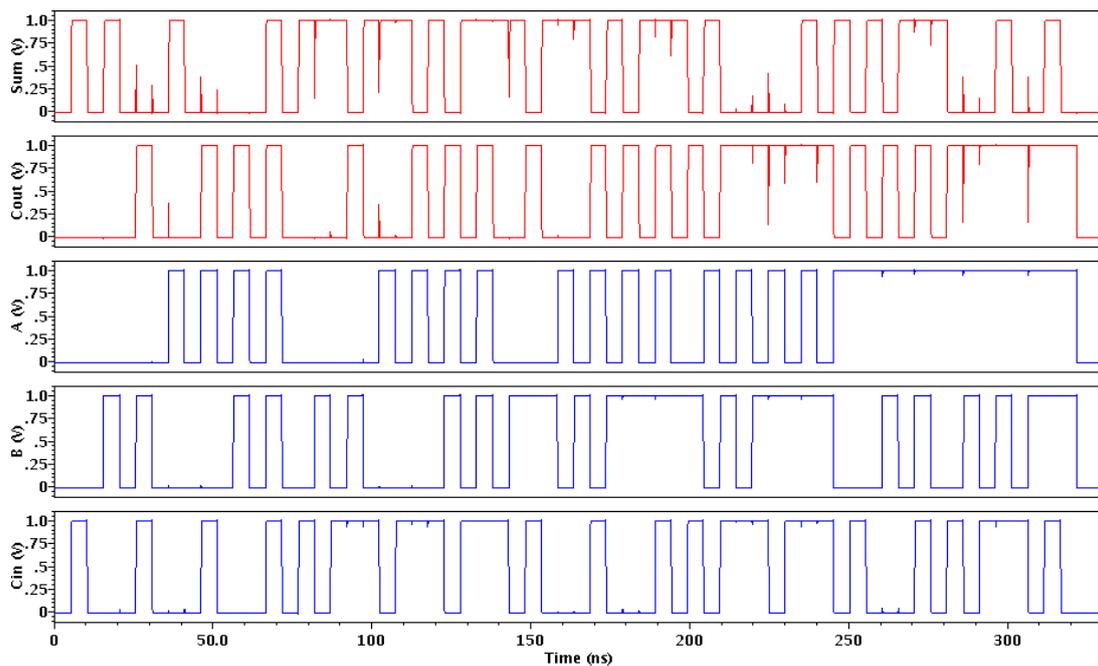


Fig. 10. Simulation Waveforms of Proposed 1-bit FA circuit to extract Delay

IV. SIMULATION RESULTS AND DISCUSSION

The results of the suggested FA and other reported adders in terms of their DMs are shown in this section. In terms of TC, the DMs under consideration are power, delay, PDP, and area. All of the FAs under consideration were created using Cadence's Virtuoso tool for a fair comparison. Spectre simulator is used to simulate circuits based on the PTM 45 nm technology node. The DMs were retrieved under common PVT settings to analyse the performance of all FAs under consideration.

In Table VII, the related values are tabulated. Figures 9 and 10 demonstrate the simulated waveforms used to extract the power and delay of a proposed FA, respectively. The following conclusions can be reached from Table VII:

- The planned FA's average power is 1.23 W, which is the 4th lowest among the 12 reported FAs, according to the 'Avg. Power' column. This power advantage can be attributed to the suggested adder's underlying architecture. The highest power is dissipated by the CPL (3.05 W) and Hybrid3 (3.66 W) FAs.

Full Adder Circuit	Avg. Power (μW)	Delay (ps)	PDP (fJ)	Area (TC)	Ref.
C-CMOS	1.16	111	0.129	28	[21]
CPL	3.05	173	0.530	38	[20]
TGA	1.28	138	0.177	20	[14]
TFA	1.14	155	0.177	16	[12]
HPSC1	1.32	123	0.162	22	[16]
HPSC2	1.44	124	0.178	26	[13]
DPL	1.31	149	0.195	28	[10]
SRCPL	1.40	138	0.193	26	[10]
Hybrid1	1.08	143	0.154	16	[7]
Hybrid2	1.51	165	0.250	16	[3]
Hybrid3	3.66	238	0.871	24	[5]
Proposed	1.23	122	0.156	24	This work

TABLE VII

PERFORMANCE COMPARISON OF PROPOSED AND OTHER REPORTED FAS IN TERMS OF DMS

The output of CPL has more TC, while the output of Hybrid3 has more glitches. The suggested FA's latency is '122 ps,' which is the 2nd lowest among other reported high-speed FAs, according to the 'Delay' column. The crucial path between the input signal 'A' and the output signal 'Sum' causes this delay. When the input signal vector ABCin changes from '100' to '011', there is a delay. The suggested FA has a PDP metric of 0.156 fJ, which is the third lowest among all other FAs examined for comparison, according to the PDP column. This PDP adder has a little higher PDP value than the other lowest PDP adders. The shortest PDP is due to a shorter time delay.

Considering the overall inferences, the PDP and TC of proposed adder is found to be best and comparable with other reported FAs. Thus, the proposed FA can be considered as an alternative choice for energy efficient and area efficient DSP applications.

V. CONCLUSION

A unique 24T 1-bit FA circuit was introduced in this research study. The suggested FA is based on a unique hybrid XNOR circuit that employs GDI, TG, and SCMOS logic. The proposed FA's performance has also been compared to those of previously reported FAs. Power, latency, PDP, and TC were all used to make the comparison. The DMs of all 12 FAs under study were retrieved utilising a same test bench under the identical PVT settings. The average PDP and TC of a proposed FA are best and comparable to other reported FAs, according to the comparative results. As a result, the suggested FA circuit can be thought of as an alternative for energy-efficient DSP applications.

CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

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